Fully Differential mm/sub-mm Wave CMOS Amplifiers

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Abstract: This paper presents an effective design methodology and flow, which is validated through three mm-wave/sub-mm-wave amplifiers: including W-band LNA with NF=7dB, W-band PA with PAE >11% and D-band amplifier with gain>20dB. The CMOS based amplifiers can be integrated with III-V materials to form heterogeneous integration, such as COSMOS, to achieve the best performance for various applications.

Keywords: *Amplifier; CMOS; COSMOS; Low Noise Amplifier; Power Amplifier.*

Introduction

Millimeter wave and sub-millimeter wave systems have drawn substantial interests due to their unique capabilities in various radar, radio and sensing applications. The continuous aggressive scaling of CMOS begins to find its ground in mm-wave/sub-mm-wave systems through its high speed devices. CMOS based integrated solutions, offering high integration, small form factor and low power consumption, may increase the system accessibility and open new application fields. In addition, the unparalleled integration with on-chip digital processing and calibration enables system re-configurability and high reliability. To achieve single chip integration solution in CMOS or COSMOS, one of the most challenging blocks is the amplifier, which includes low noise amplifier at receiver side, high power and high efficiency power amplifier at transmitter side.

The design challenges are: first, the inherent drawbacks of CMOS process, such as lossy substrate, large parasitics, shrinking supply and device breakdown voltages, etc.; second, the inaccurate device model, for both active and passive components, at such high frequency to guide high performance circuit design. This paper presents an effective design and verification flow that may overcome CMOS process drawbacks and modeling insufficiency to push CMOS into mm-wave/sub-mm-wave frequencies and beyond. The proposed methodology has been validated in several mm/sub-mm wave CMOS amplifier designs: W-band and D-band Power Amplifiers (PAs), W-band Low Noise Amplifier (LNA). The design methodology can also be applied in other high frequencies to guide accurate circuit design for high performance and design fidelity.

Design Methodology

Existing mm/sub-mm wave amplifiers are based on single ended circuit structure [1-4]. This structure renders the circuit sensitive to environmental and process variations such that any circuit parasitic, including L, C and R, mutual coupling and device performance deviation may dramatically degrade circuit performance. Single ended structure is also vulnerable to common mode and supply noises. Consequently, differential circuit structure, with slight power overhead, is more integration friendly, which simplifies the design by only focusing on local parameter optimization. On the other hand, differential structure desensitizes the common mode and supply noises which are inevitable in integrated circuits/systems; it also annihilates other common mode parasitic effects and doubles the amplifier dynamic range. Therefore, we adopt differential architecture in all the amplifier designs for high robustness.

To increase amplifier stability by reducing parasitic capacitance induced by Miller effect, we utilize cascode amplifier structure, shown in Fig. 1. The inner node between bottom and cascode devices has large stray capacitance, which degrades amplifier gain and efficiency by shunting large portion of signal current to ground. The added series transmission line forms as π network to achieve wideband operation and tune out the parasitic capacitance; it also alleviates Miller effect at the same time by introducing smaller voltage gain from the bottom device gate to drain. Planar transformers are used as inter-stage coupling and matching [5] to realize compact, efficient and symmetrical amplifiers. Transformer coupling based structure provides several key advantages to benefit high frequency amplifier design over traditional capacitor based AC coupling: (1) it has higher coupling efficiency than capacitor based approach at high operation frequencies, such as mm-wave/sub-mm-wave frequencies; (2) it naturally supports individual bias optimization for each stage; (3) designers have more freedom to optimize circuit performance by choosing voltage amplification or current amplification through different turn ratios; (4) the physical layout is compact and symmetrical, which facilitates EM simulation and supports well-matched circuit parameters; (5) this signal-driven scheme minimizes traveling loss for high gain and high power efficiency.

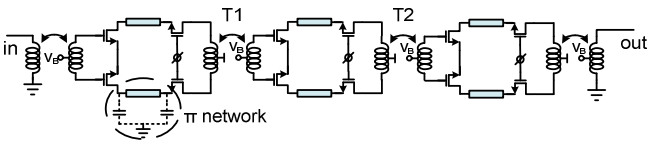

Figure 1 Integration friendly, fully differential CMOS amplifier circuit topology

In mm/sub-mm wave frequencies, active device model is vastly layout dependent. The extrinsic parasitics, such as gate/source/drain resistance, substrate resistance and coupling capacitors, ultimately determine the maximum achievable

gain and/or minimum noise figure. The RF models provided by foundries are typically not optimized for mm/sub-mm wave frequency design, which is only used to build the initial circuit schematic. We then customize the active device layout for amplifier performance optimization: minimize gate/source resistance and gate parasitic capacitance for best noise performance in LNA; increasing power handling and distributing current evenly are additional layout concerns for PA. Afterwards, a realistic device model is established by adding external parasitics, extracted from CAD tools. Caliber RCX extracts the R and C parasitics in the core device proximity area. EM tools, such as Momentum and HFSS, are used to simulate the access line effects. The real model is built by adding these two extracted parasitic parts on top of the BSIM models provided by foundries, illustrated by Fig. 2.

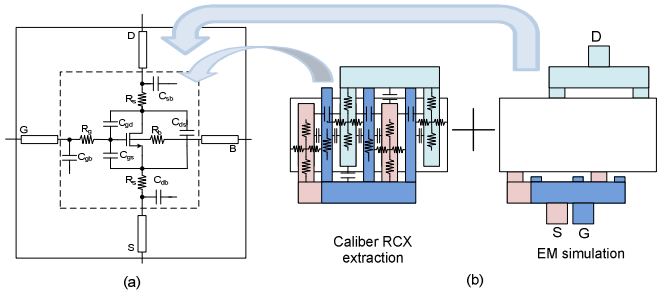

Figure 2 (a) Mm-wave MOS device model, (b) core device parasitics extracted by Caliber RCX and access lines simulated by full-wave EM tools

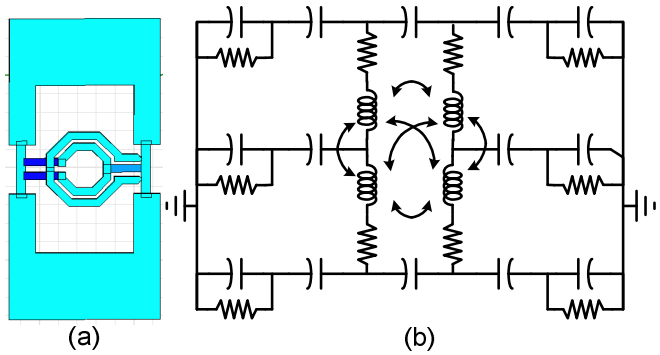

Figure 3 Monolithic transformer (a) layout and (b) model

Accurate transformer modeling is critical due to excessive coupling and bidirectional operation which significantly affects circuit performance. Our signal-driven design approach is to minimize signal propagation loss for high efficiency. However, it causes design difficulty and may result in potential unstable issue because of the strong coupling among closely positioned stages. To mitigate this issue, solid metal guard rings are added for each transformer, which minimizes the coupling by focusing the electromagnetic flux within the guard rings. The complete transformer structure including the guard ring, shown in Fig. 3(a), is simulated by full wave simulator Ansoft HFSS. Based on the simulated S parameters, we build the transformer model through physical representations of all possible parameters and coupling to facilitate circuit design. Fig. 3(b) presents the model structure. The newly built both active and passive device models are then applied into circuit simulation to optimize design parameters for best performance.

mm/sub-mm Wave Amplifiers

With the aforementioned design methodology, we have demonstrated three mm/sub-mm wave amplifiers: W-band LNA, W-band and D-band PAs all in 65nm CMOS technology. To facilitate characterization, all the three amplifiers embed input and output baluns to convert single-ended off-chip signal into differential on-chip signals in the receiver LNA and vice verse in the transmitter power amplifier. The baluns are incorporated into matching network to save extra matching components for compact and efficient design. The baluns also accomplish ESD protection because they isolate the circuits properly from outside environments to minimize exposure to harmful ESD.

Advanced CMOS process shrinking voltage supply imposes challenges on large power and high linearity design needs. We purposely choose to bias the bulk of cascode device higher (>0.5V) so that the circuit can tolerate higher supply voltages (>2V) without reliability concern.

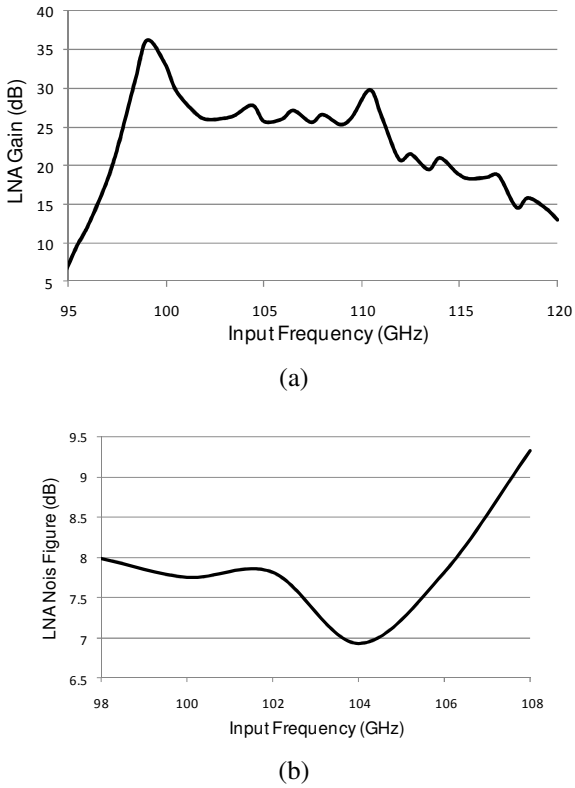

Figure 4 Measured W-band LNA results (a) power gain over 25dB from 98GHz to 111GHz, (b) minimum NF 7dB

W-band LNA is constructed according to Fig.1 with the emphasis on low noise performance. To achieve minimum noise figure and good input matching at the same time, the input device size is chosen to have the minimum noise resistance about 50ohm. The W-band LNA has 3 internal

stages and the last output driver stage for 50ohm load. It achieves power gain > 25dB over 13GHz bandwidth and the record low 7dB NF. The overall power consumption is 60mA from 1.4V supply.

W-band PA also follows the aforementioned design flow and methodology with the only exception that the last stage is configured to be common source in order to enhance the maximum output power and increase power efficiency. Therefore, it requires an extra power supply, VDD2, which is smaller than previous cascode stage power supply, VDD1. Figure 5 illustrates the measurement setup. W-band input source is generated from a frequency multiplier chain, which drives a linear external attenuator to feed the chip input. Output power is measured through a power sensor. Measurement results are presented in Fig. 6. Fig. 6(a) shows the tested output power, power gain and PAE (Power Added Efficiency) versus the input power when VDD1=2V, VDD2=1.2V. At the same supply configuration, Fig. 6(b) shows the measured Psat (saturation power) and PAE versus the input frequency, which demonstrate 12dBm Psat, 11% PAE, 10dB gain and 9dBm OP1dB. The DC power consumption is about 200mW.

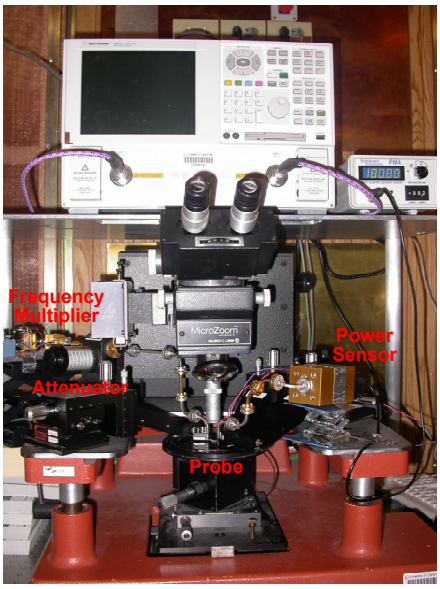

Figure 5 W-band PA large signal measurement setup

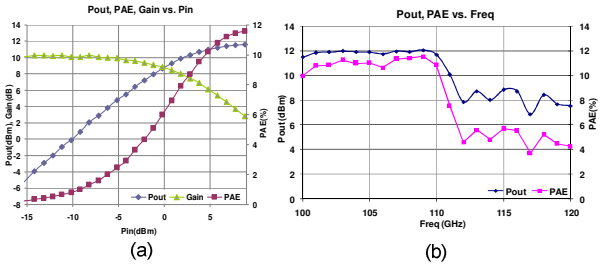

Figure 6 Measured W-band PA results: (a) output power, gain and PAE vs input power, (b) Psat and PAE vs input frequency

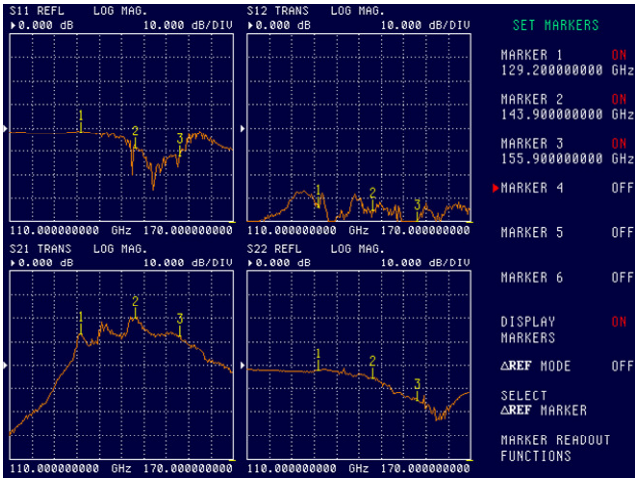

Figure 7. Measured D-band PA S parameters

D-band amplifier is designed for large power gain to boost signal level for high Signal-to-Noise-Ratio (SNR). Network analyzer with D-band frequency extension arms are used to characterize its small signal performance. Fig. 7 shows the measured S-parameters, which demonstrate maximum 20dB gain with >10dB gain over the frequency range of 128GHz~158GHz, input return loss better than -10dB from 140GHz to 156GHz, output return loss better than -10dB from 150GHz to 170GHz, as well as higher than 30dB reverse isolation. Large signal characterization is conducted in a similar setup as shown in Fig. 5 with the difference that D-band input source and instruments are used. Fig. 8 shows the measured large signal performance. At about 154GHz, the measured Psat and OP1dB are > 5.7dBm and 5dBm, respectively. The Psat and OP1dB at frequency <140GHz cannot be measured due to insufficient input source power. The D-band power consumption is about 102mW.

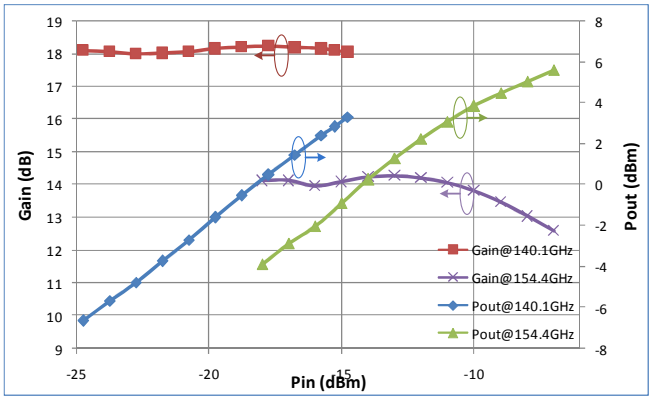

Figure 8. Measured D-band PA large signal characteristics

Table I summarizes our W-band and D-band PA performance and compares them with those of state-of-the-art. We have demonstrated higher output power, larger small signal gain and superior PAE with fully differential circuit implementation, which validates the effectiveness of our design methodology. Die photos of the three amplifiers are

shown in Fig. 9, all implemented in 65nm CMOS technology.

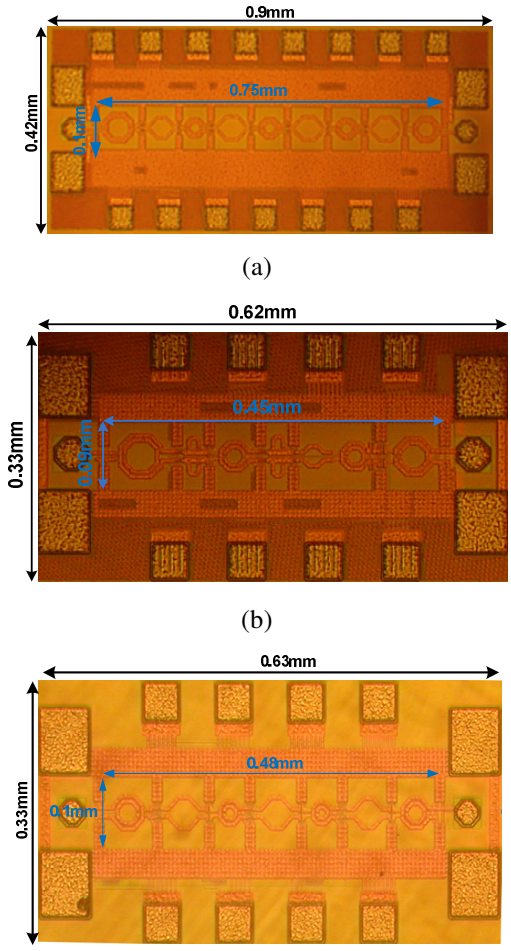

Figure 9. Die photos of (a) W-band LNA, (b) W-band PA, (c) D-band PA

Conclutions

This paper presents an effective design methodology and flow, which covers active and passive design modeling, amplifier architecture, simulation and verification scheme, etc., to achieve high performance amplifier design in mm-wave/sub-mm-wave frequency region and beyond. The scheme is validated successfully through 3 CMOS amplifiers: W-band LNA, W-band PA and D-band PA. This work contributes to the goal of integrated solutions under process/supply restrictions of deep-scaled CMOS technologies to satisfy the space, weight and power (SWaP) constrained system requirements for various applications, and push for ultra high performance integrated mm-Wave/sub mm-Wave systems with COSMOS option.

Acknowledgement

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Table I Performance Summary and Comparison

	This work	**This work**				
	D-band PA	**W-band PA**	[1]	[2]	[3]	[4]
Architecture	**Differential**	**Differential**	Single End	Single End	Single End	Single End
Techology	**65nm CMOS**	**65nm CMOS**	65nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS
Center Freq. (GHz)	**144**	**106**	150	140	104	80
Gain (dB)	**20.6**	**10**	8	8	9	8.5
Psat (dBm)	**>5.7**	**12**	6.3	>-1.8	n/a	6.6
P1dB (dBm)	**5**	**9**	1.5	-5	n/a	2.2
PAE	**3.6**	**11.4**	9.5	n/a	n/a	n/a
Power Comp. (mW)	**102**	**220**	25.5	63	22	n/a
Core Area (mm2)	**0.05**	**0.04**	0.16	0.06	0.24	n/a