

A 60 GHz Tunable Output Profile Power Amplifier in 65 nm CMOS

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Abstract—A fully integrated three-stage 60 GHz power amplifier with amplitude/phase compensation is realized in 65 nm CMOS. An adaptive feedback bias scheme with three control knobs is proposed to extend the linear operating region. At a supply voltage of 1 V, the fully differential amplifier achieves a linear gain of 15 dB and occupies a compact area of 0.056 mm². It achieves a minimal $P_{\text{sat}} - P_{1\text{dB}}$ separation of 0.6 dB by extending the $P_{1\text{dB}}$ by 8.5 dB. To our best knowledge, this is the smallest $P_{\text{sat}} - P_{1\text{dB}}$ separation reported to date. With on-chip phase compensation, the output phase variation is reduced by 57%.

Index Terms—CMOS, millimeter wave, power amplifier (PA), transformers.

I. INTRODUCTION

MULTI-Gb/s short-range wireless applications at 60 GHz require highly linear power amplifiers (PAs) to meet stringent RF linearity performance specifications with low cost commercial pricing. This letter presents a new linearity enhancement technique through a compact feedback control implemented in CMOS process that linearizes output amplitude profile (AM-AM). CMOS transmitter front-ends with PAs exhibit compressive gain profiles as shown in Fig. 1. The non-linear transconductance and temperature-dependent mobility result in early gain compression in CMOS PAs. This leads to an overall soft gain profile which has a large separation between the saturated output power (P_{sat}) and output 1 dB compression point ($P_{1\text{dB}}$) that severely limits the linear operating range under a constrained supply voltage. For the high data-rate applications with large peak-to-average power ratio, the PAs operate at power back-off from $P_{1\text{dB}}$. Moving $P_{1\text{dB}}$ closer to P_{sat} can fully utilize the limited supply voltage to maximize the linear power region, thus enlarging the linear transmitted power while satisfying the spectrum and constellation requirements. Our novel feedback structure enables this feature.

The PA architecture presented herein demonstrates the first highly linear 60 GHz PA with on-chip amplitude and phase compensations in 65 nm CMOS, which has not been reported in recent 60 GHz PA publications [1]–[7]. The bias block promptly tracks the signal output power level and returns a dc voltage to

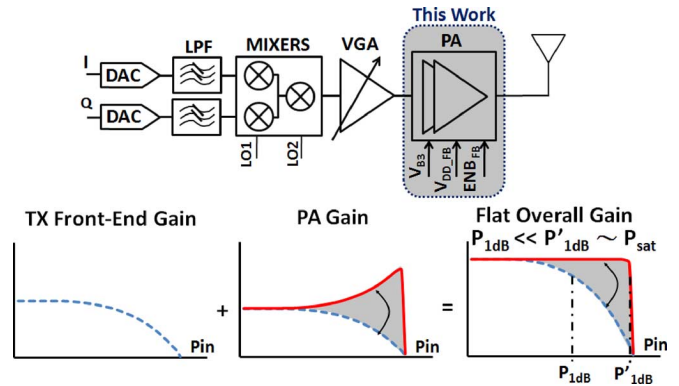


Fig. 1. Transmitter block diagram with tuning knobs and gain shaping.

the gate of the amplifier. The PA output profile is adjustable by three control knobs to compensate for the early gain compression characteristic of its preceding stages for a desirable overall response.

II. CIRCUIT DESIGN

This PA is a fully differential three-stage transformer-coupled design in 65 nm 1P6M standard CMOS process as shown in Fig. 2. This process has six metal layers with one thick top metal of 3.4 μm for low-loss passive design and interconnects. Fully differential configuration is chosen to minimize the interferences to other blocks, lower the even-order harmonics, and reject common-mode noises. The first two stages are cascode topology to boost gain and reverse isolation by mitigating the Miller effect. The last stage is a common-source amplifier with its device dimension chosen to achieve 10 dBm output power for 60 GHz standards such as IEEE 802.15.3c and WirelessHD. This PA is designed so that the last stage reaches large-signal saturation first, with each preceding stage reaching saturation approximately 3 dB later for maximum power delivery. The first two stages are biased at shallow class-AB region to provide sufficient gain and power to the last stage.

This design utilizes transformers to provide a compact impedance matching and a simple biasing scheme applied at the center-taps [7]. The width of the transformers in the first two stages (T_1 , T_2 , and T_3) is relatively narrow (4 μm) to minimize the coupling capacitance from the coils to the substrate to maximize the self-resonant frequencies. Both the primary and secondary coils are implemented on the top metal to maximize the quality factors. The width of the output transformer (T_4) is wider (10 μm) to match with large devices in the last stage and to provide sufficient current handling capability (> 100 mA). Because of its large size, a vertically-stacked transformer is used for a compact design. The self-resonant frequencies of

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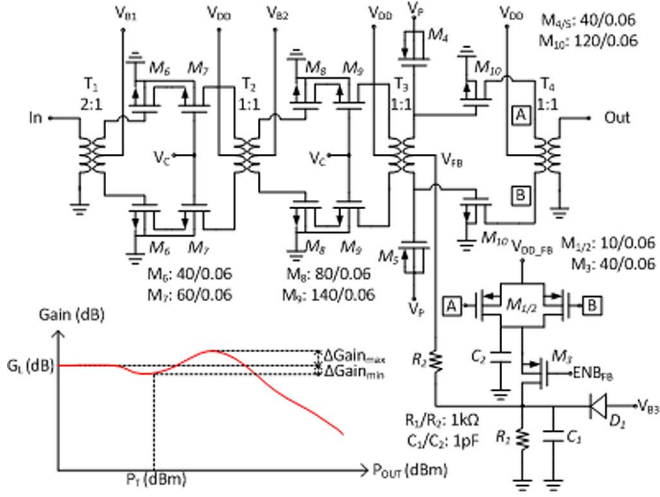


Fig. 2. Schematic of the PA with feedback bias control.

the transformers are designed to be larger than 150 GHz to accommodate parasitic capacitances from the interconnects and the devices. Stabilizing resistors are inserted at the center-taps of the transformers to improve the common-mode and bias stabilities with negligible differential-mode performance degradation. The gate terminals of the cascode devices and the power supply terminals are decoupled by high-Q capacitors to provide a low impedance path to ac ground to facilitate stability.

In order to maximize the linear operating power range by extending $P_{1\text{ dB}}$ closer to P_{sat} , a novel feedback bias control loop (M_1 – M_3 , D_1 , R_1 , R_2 , C_1 , C_2) with small area (0.4%) and power (1%) overheads is added to the last stage to dynamically adjust its gate bias V_{FB} according to the output power level as shown in Fig. 2. Low-threshold PMOS devices (M_1/M_2) are connected to the output of the last stage to sense the output voltage. These two transistors have minimal effect on the PA performance due to their small loading imposed on the PA. Depending on the sensed output voltage swing, the feedback loop modulates the gate of the last stage in real-time. The physical size (width/length) of the feedback transistors (M_1/M_2) sets the range and rate of change in the feedback bias V_{FB} . The optimal V_{FB} curve is first acquired in simulation to minimize dc power consumption in the low power region and adaptively increase the gain while power increases. The sizes of M_1/M_2 are selected accordingly so that the feedback bias matches the optimal one from the simulation. 1 pF capacitors (C_1 and C_2) are inserted to filter the high frequency components. By properly selecting the parameters of R_1 , R_2 , and C_1 , the bandwidth of the loop can be set higher than that of the signal envelope. Therefore, the dynamic gate voltage promptly tracks the input signal envelope.

Three voltage control knobs, $V_{\text{DD_FB}}$, ENB_{FB} , and V_{B3} , adjust P_{T} , $\Delta\text{Gain}_{\text{max}}$, and G_{L} , respectively, in the gain profile as indicated in Fig. 2. At low input power, the feedback transistors are off and the gate voltage V_{FB} is set by the diode (D_1) and V_{B3} at a low level to optimize efficiency. The linear gain G_{L} is determined by V_{B3} . As the output voltage swing becomes larger than the threshold voltage of the feedback transistors, the feedback loop turns on at P_{T} and controls V_{FB} . Transistor M_3 acts

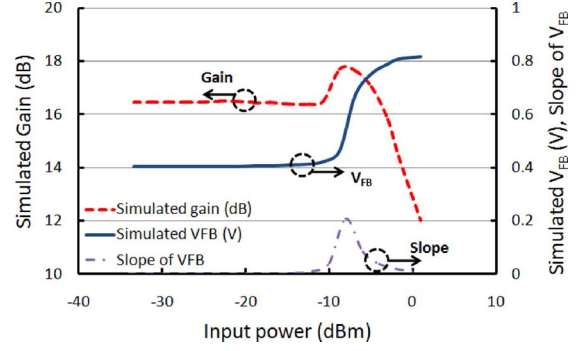


Fig. 3. Simulated gain and feedback voltage of the PA.

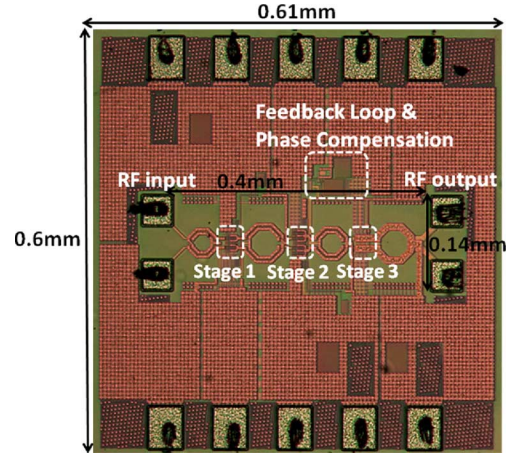


Fig. 4. Chip micrograph of the PA.

to enable the loop. Tuning the gate voltage of M_3 (ENB_{FB}) adjusts the feedback factor that determines the amount of the gain expansion $\Delta\text{Gain}_{\text{max}}$. $V_{\text{DD_FB}}$, tied to the V_{s} of M_1/M_2 , controls the triggered power P_{T} where the feedback loop occurs by changing the overdrive voltage of M_1/M_2 . The static simulated V_{FB} is shown in Fig. 3 along with the corresponding simulated gain. V_{FB} starts at 0.4 V in the small-signal region and eventually increases to 0.8 V in the saturation region. The peak gain occurs approximately where the slope of V_{FB} is at its maximum. This loop does not create any stability issue because the two poles of the loop are far below 60 GHz.

Besides amplitude distortion, phase distortion is another critical factor affecting signal linearity in CMOS PAs. A PMOS-based capacitance compensation is applied to heal phase distortion by choosing the sizes of the PMOS devices (M_4/M_5) to cancel the nonlinear NMOS capacitance C_{gs} in the PA [8]. The effects of including the PMOS devices are accounted for in the design by properly selecting the transformer T_3 such that there is no gain and power degradation.

III. MEASUREMENT RESULTS

The chip micrograph of the PA is shown in Fig. 4. The core PA occupies a compact area of $0.14 \times 0.4 \text{ mm}^2$. All of the measurements are performed through on-chip probing. The S-parameters of the amplifier are shown in Fig. 5 with a peak linear gain of 15 dB at 60 GHz. The stability factor K larger than one across the entire spectrum demonstrates unconditional stability.

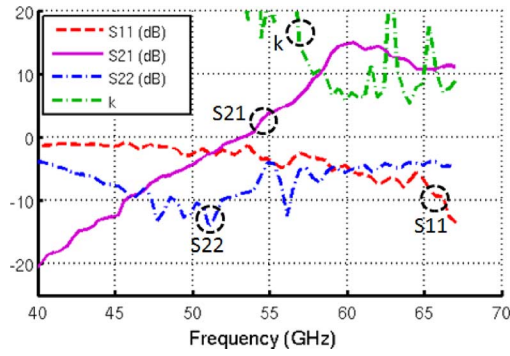


Fig. 5. Measured S-parameters of the PA.

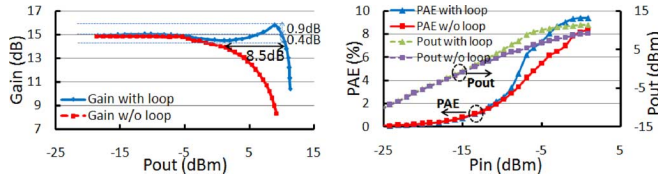


Fig. 6. Measured gain, Pout, and PAE of the PA with and without the loop.

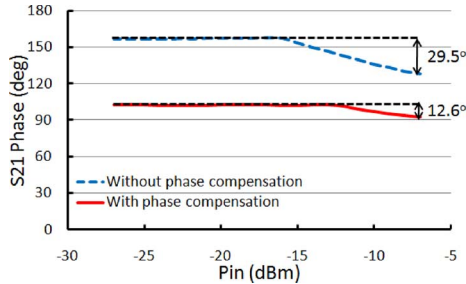


Fig. 7. Measured S21 phase of the PA with and without the phase compensation.

Large-signal performance of the PA is measured by a V-band source module and power sensor. Fig. 6 shows the gain profile, output power, and power-added-efficiency (PAE) of the PAs at 60 GHz with and without the loop in direct comparison. In the small-signal region, both PAs have the same linear gain. As the input power increases, the PA without the loop starts to compress because of the limited maximum current, whereas the one with the loop remains relatively constant until it experiences expansion before its eventual compression. The measured gain of the PA with the feedback loop compresses by 0.4 dB and expands by 0.9 dB relative to its small-signal level before it reaches $P_{1\text{ dB}}$. The $P_{1\text{ dB}}$ differs by 8.5 dB between the two PAs. At a supply voltage (V_{DD}) of 1 V, the $P_{1\text{ dB}}$ of the PA with the feedback loop is 10.7 dBm and the P_{sat} is 11.3 dBm. The peak PAE is 9.4% and the PAE at $P_{1\text{ dB}}$ is 8.3%. When V_{DD} increases to 1.2 V, the P_{sat} is 12.6 dBm and the $P_{1\text{ dB}}$ is 12 dBm at 60 GHz.

The measured S21 phase is shown in Fig. 7. The S21 phase shift is reduced by 57% from 29.5° to 12.6° by applying the on-chip PMOS-based phase compensators.

IV. CONCLUSION

A V-band PA with adaptive feedback bias control using 65 nm CMOS process is demonstrated. By the proposed on-chip tun-

TABLE I
COMPARISON OF 60 GHz SILICON PAs

	This work	[1]	[2]	[3] [*]	[4]	[5]	[6]
Technology	65nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	90nm CMOS
V_{DD} (V)	1	1	1	1.2	1.2	1.2	1.2
Gain (dB)	14.9	15.8	10	14.3	30	8.5	20
P_{sat} (dBm)	11.3	11.5	12.6	16.6	10.6	7.2	12
$P_{1\text{ dB}}$ (dBm)	10.7	2.5	8.8	11	7.5	4.2	8.2
Peak PAE (%)	9.4	11	6.9	4.9	18	2.3	9
Area (mm ²)	0.056	0.053	0.64 *	0.462	0.525	0.065	0.64 *
PAE @ $P_{1\text{ dB}}$ (%)	8.3	5 #	< 5 #	< 5 #	< 5 #	n/a	4 #
$P_{\text{sat}}-P_{1\text{ dB}}$ (dB)	0.6	9	3.8	5.6	3.1	3	3.8
Phase compensation	Yes	n/a	n/a	n/a	n/a	n/a	n/a

* Including pads
Estimated from figures
* power combining

able output profile technique, the linear operation region is effectively extended by 8.5 dB. At a supply voltage of 1 V, this compact PA achieves a linear gain of 15 dB and the lowest $P_{\text{sat}}-P_{1\text{ dB}}$ separation of 0.6 dB ever reported to our best knowledge. Table I summarizes the performance of this PA in comparison with recently published state-of-the-art 60 GHz PAs. This PA provides a high linear and low cost solution for spectrum-efficient applications.

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