A Low Power V-Band CMOS Frequency Divider With Wide Locking Range and Accurate Quadrature Output Phases

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***Abstract*—A new injection-locked frequency divider (ILFD) circuit topology, by combining the strengths of *LC* type ILFD (LC_ILFD) and ring oscillator type ILFD (RO_ILFD), is proposed to achieve high speed, low power, wide locking range and accurate quadrature output phases. The frequency-division criterion is analyzed and agrees well with simulation results. The phase-locking mechanism is also investigated with emphasis on its resilience to device and circuit mismatches. A prototype is implemented in TSMC 90 nm CMOS to validate the effective locking range of 7.4 GHz (53.4 to 60.8 GHz) with 0 dBm input signal and 5 mW DC power dissipation. The circuit attains the highest figure-of-merit (dividing frequency/power) to date for V-band frequency dividers implemented in deep-scaled CMOS technologies.**

***Index Terms*—Accurate quadrature phase, injection-locked frequency divider, low power consumption, phase noise, RF CMOS, wide locking range.**

I. Introduction

WIDE-RANGE unlicensed ISM band at 60 GHz for wireless Ethernet and Wireless HDMI (or WirelessHD) demands high-speed, broadband and low-power frequency dividers with accurate quadrature output phases for precise and efficient frequency syntheses in modern radio systems [1], [2], such as IQ mixing for direct-conversion wireless transceiver, multi-bands generation by single-sideband (SSB) mixers, etc. The phase accuracy among quadrature outputs are particularly challenging for frequency dividers implemented in deep-scaled CMOS technologies with substantial device offset and circuit mismatch due to increasing process and lithographic variations.

For high frequency operations, injection-locked frequency dividers (ILFDs) are superior to their digital counterparts [3], [4] in terms of dividing speed and DC power consumption. Nevertheless, none of the traditional types of ILFDs, including both the *Ring Oscillator* type ILFDd (or RO-ILFD) [5] and *LC* type ILFD (or LC-ILFD) [6], [7] would offer high dividing speed and wide locking range simultaneously with accurate quadrature phase outputs.

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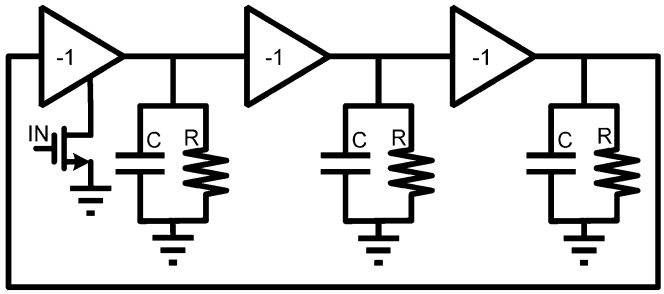


Fig. 1. Traditional ring oscillator based injection-locked frequency divider (RO-ILFD).

The RO-ILFD, as shown in Fig. 1, is known for its extensive locking range and relatively accurate output phases attributed to its close loop circuit architecture. Its maximum dividing frequency is limited by the delay of each stage, which is confined by the RC time constant. High voltage gain which is compulsory to commence the oscillation demands a high resistive load R. This in turn restricts the design options of the capacitor, C, and ultimately limits the maximum operation frequency of the divider.

By using inductor as load, the maximum operation frequency of RO-ILFD can be boosted. However, multiple inductors occupy significant silicon area and the complicated interconnection and magnetic coupling condition make this architecture non-attractive. To avoid the design complexity of inductive load RO-ILFD, [1] proposed a quadrature LC-ILFD, as shown in Fig. 2. It injects differential input signals into two stand alone *LC* cross couple pairs to generate quadrature outputs. Unlike the traditional D-Flipflop type frequency divider, this LC-ILFD reduces circuit parasitics by removing cross couple devices between I and Q pairs so that it allows enhancing the divider load inductance and enables it work at higher frequency with less power consumption. But this LC-ILFD has two disadvantages: limited locking range and poor quadrature phase accuracy. It is because the injecting current input has to go through the common source of the cross-coupled differential pair, which is with heavy parasitic capacitance. This parasitic capacitance shunting to ground digests a substantial portion of the injecting current, so only partial injecting current contributes to the oscillation of upper differential pair. Unfortunately, the injection loss becomes worse as the operation frequency increases and this resists its application in ultra high frequency domain. To extend locking range of LC-ILFD, the source shunt-peaking and power-matching techniques have been employed in [8] and [9] to enhance the injection efficiency. However, these techniques

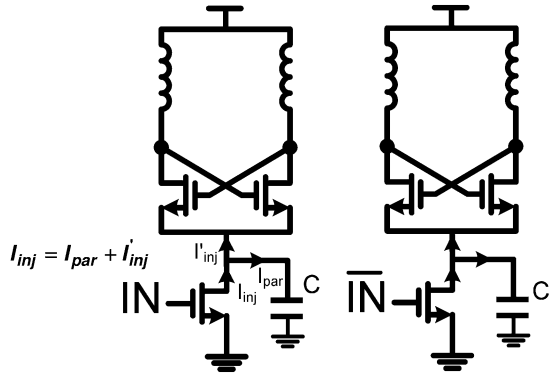


Fig. 2. Traditional *LC* based injection-locked frequency divider (LC-ILFD).

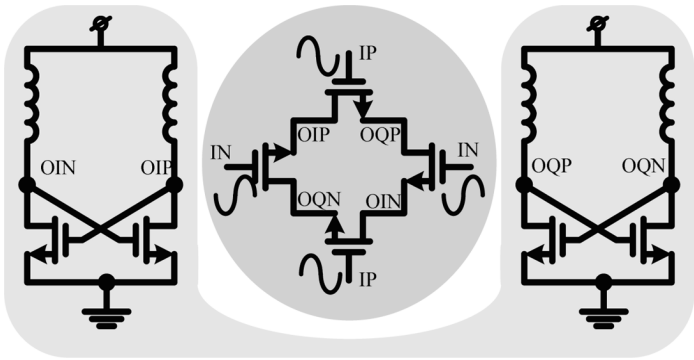


Fig. 3. WLR-ILFD with central mixer-loop sandwiched by cross-coupled pairs with resonance tanks.

entail extra passive components and increase the circuit and layout complexity. Furthermore, this LC-ILFD with two stand alone dividers has no well-defined loop and renders the divider more vulnerable to process variations, so it is reluctant to offer precise quadrature output phases. In addition, the traditional LC-ILFD will encounter the reduced signal headroom problem in further-scaled CMOS technologies owing to its stack architecture.

To overcome the aforementioned deficiencies in conventional ILFDs, a new circuit topology of *Wide Locking Range ILFD* (or WLR-ILFD) with the combined strengths of both LC-ILFD and RO-ILFD is presented in this paper to offer low power operation, high dividing speed, wide locking range and accurate quadrature output phases for V-band frequency synthesis applications.

This paper is organized as follows: Section II presents the circuit architecture and design criteria of the newly invented WLR-ILFD circuit topology. Section III analyzes the dividing mechanism for enhanced locking range and quadrature phase accuracy. Section IV provides the prototype test results with validated circuit performance and Section V summarizes the work.

II. Circuit Design

As depicted in Fig. 3, the proposed WLR-ILFD comprises a central loop made of four mixers linked back-to-back between the drain and source of adjacent nMOS devices and two stand alone cross couple differential pairs with resonance tank. The connection points, OIN, OIP, OQP and OQN, are subsequently wired to differential outputs of two identical cross-coupled nMOS pairs with loaded tanks to resonate at the desired frequency, which is the sub-harmonic of the input frequency and similar to conventional LC-ILFDs. The central loop of mixers is intended to provide the required locking range and quadrature phase outputs, which is similar to the conventional RO-ILFD.

However, the new WLR-ILFD operates very differently from the conventional LC- and RO-ILFDs. The input signal is injected to the central loop directly instead of the current source of the differential pair. This alleviates the inefficient injection issue of the conventional LC-ILFD when operating at high dividing frequency and permits the use of larger size MOS device in current source with reduced overdrive voltage for DC biasing. It also helps mitigate the headroom problem in deep-scaled CMOS under low supply voltage.

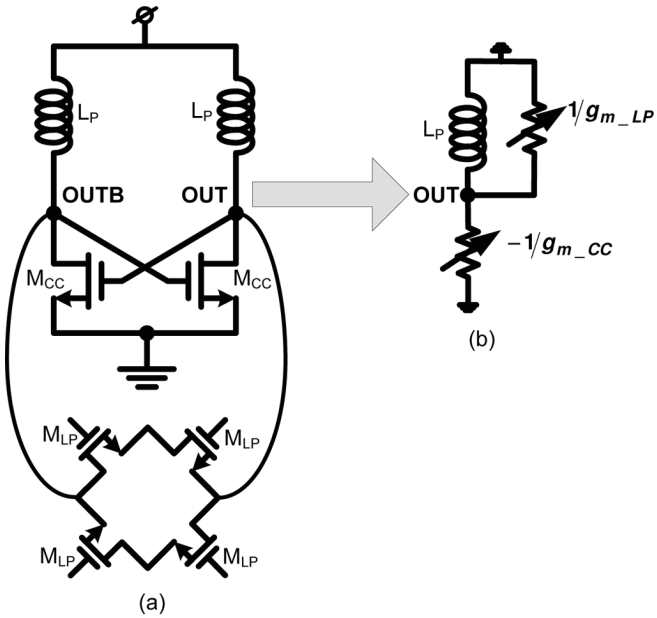


Fig. 4. (a) *LC* resonator with mixer loop loading. (b) Equivalent impedance at the resonator output.

Because the differential input signals of IN and IP are injected to gates of adjacent mixer devices in the central loop, the input signals with the same polarity (either with IN or IP) are naturally linked to the gates of diagonal-positioned mixer devices and defines the output phase relation. The output phases along the central loop at link points of OIN, OQP, OIP and OQN have been clearly defined into 0°, 90°, 180° and 270° accordingly. Among them, the OIN and OIP are tied to the output of the left-hand side cross-coupled differential pair, and the OQP and OQN are tied to the right-hand side cross-coupled differential pair, respectively.

By combining unique features of both LC- and RO-ILFDs, the proposed WLR-ILFD is most suitable to operate at the high frequency (i.e., 60 GHz) with wide locking range (>7 GHz) and high resilience to process variations so as to maintain accurate phase outputs, whose resilience factor is less than 1.7°/1%, and meet the stringent frequency syntheses requirements in future multi-gigabit/sec V-band radio systems.

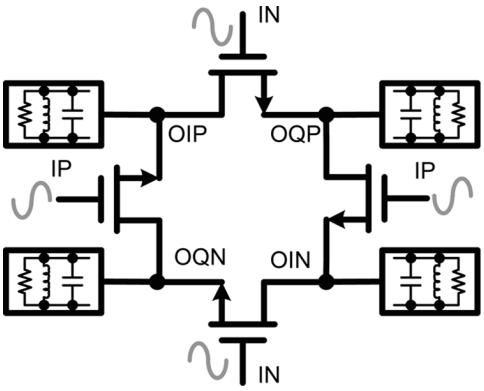


Fig. 5. Mixer loop loaded by resonance tank. Loop gain ≥ 1.

III. Analytical Models

A. Locking Range

Since the ILFD functions by synchronizing its built-in oscillation to the incident signal, both of its gain and phase relations must satisfy Barkhausen criteria. Regarding the phase requirement, the cross-couple *LC* resonators must always retain positive feedback to facilitate the tank oscillation in response to the incident signals. Regarding the gain requirement, we should guarantee the contributions from both differential *LC* resonators and the central mixer loop to obtain frequency division.

We modeled one of the *LC* resonators with the mixer loop load as shown in Fig. 4(a). The small signal equivalent model, as a simplified analysis model, is used to provide design insights. To ensure the tank oscillates at desired frequencies, the equivalent output impedance at those frequencies must be negative initially. As depicted in Fig. 4(b), the impedance at the output node can be deduced as the parallel combination of the impedance looking into one mixer device source $(1/g_{m\_LP})$) and the impedance looking into one cross couple device $(-1/g_{m\_\mathrm{CC}})$, where g_{m_LP} and g_{m_CC} represent the transconductance of the mixer device and the cross-coupled device, respectively. Since the impedance of the tank at the resonant frequency is much greater than $1/g_{m\_LP}$, the resultant output impedance becomes $-1/g_{m\_CC}\|1/g_{m\_LP}$. It must be negative initially, which implies

$$g_{m\_\mathrm{CC}} > g_{m\_LP} \tag{1}$$

would ensure the oscillation. We choose g_{m_CC} two to three times greater than g_{m_LP} to achieve sufficient design margin.

The gain of the mixer loop with four identical nMOS mixers must be larger than one to guarantee frequency division, as shown in Fig. 5. Taking one of the mixers as an example, Fig. 6 shows the analytical model. The mixer nMOS is driven by an incident signal $v_i\cos(\omega_i t+\alpha)$ at the gate to obtain synchronized sub-harmonic outputs at the source as $v_s\cos(\omega_o t+\phi)$ and at the drain as $v_d\cos(\omega_o t+\theta)$. Equation (2) represents the effective drain loading by paralleling the tank impedance of $(H_N/(1+j(2Q/\omega_N)(\omega_o-\omega_N))$, where $H_N = \omega_N LQ$, with the impedance $1/g_{m\_LP}$, which is the equivalent load contributed by the next mixer NMOS.

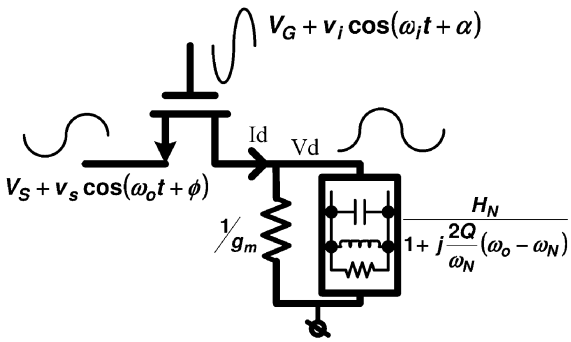


Fig. 6. Model of one mixer for dividing range analysis.

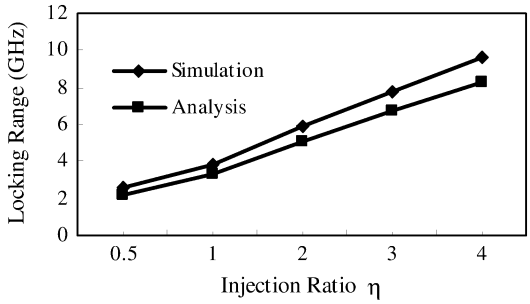


Fig. 7. Locking range versus injection ratio η.

$$\begin{aligned} Z(j\omega_o) &= 1/g_{m\_LP}\left\|\frac{H_N}{1+j\frac{2Q}{\omega_N}(\omega_o-\omega_N)}\right. \\ &\cong \frac{H_N}{H_N g_{m\_LP}+j\frac{2Q}{\omega_N}(\omega_o-\omega_N)} \end{aligned} \tag{2}$$

where ω_N is the tank resonant frequency and ω_o is the output frequency. On the other hand, the drain current of the nMOS mixer can be derived as

$$I_d = K(V_G + v_i\cos(\omega_i t+a) - V_S - v_s\cos(\omega_o t+\phi) - V_{\mathrm{th}})^2 \tag{3}$$

where $K = 1/2\mu_n C_{ox}W/L$ and $\omega_i = 2\omega_o$ for this divide-by-two case. Assuming the frequency components that are distant from the tank resonant frequency can be filtered out, and only those near the desirable output frequencies are retained and expressed as

$$\begin{aligned} I_d(j\omega_o) &= K(-2v_s(V_{\mathrm{GS}}-V_{\mathrm{th}})\cos(\omega_o t+\phi) \\ &\quad - v_i v_s\cos(\omega_o t+a-\phi)) \\ &= Re\{Kv_s(V_{\mathrm{GS}}-V_{\mathrm{th}})e^{j\omega_o t}e^{j\phi}(-2 \\ &\quad - \eta\cos(a-2\phi) - j\eta\sin(a-2\phi))\} \end{aligned} \tag{4}$$

where the injection ratio is defined as $\eta = v_i/(V_{\mathrm{GS}}-V_{\mathrm{th}})$.

To satisfy the Barkhausen criteria for oscillation, the voltage gain of each mixer element in the mixer loop must exceed unity. Therefore, the amplitude of the output, the drain voltage (v_d), must exceed that of the input, the source voltage (v_s), at the dividing output frequency. Accordingly, we can get

$$|v_d/v_s| \geqslant 1 \quad \Rightarrow \quad |v_d| = |I_d(j\omega_o)\times Z(j\omega_o)| \geqslant |v_s| \tag{5}$$

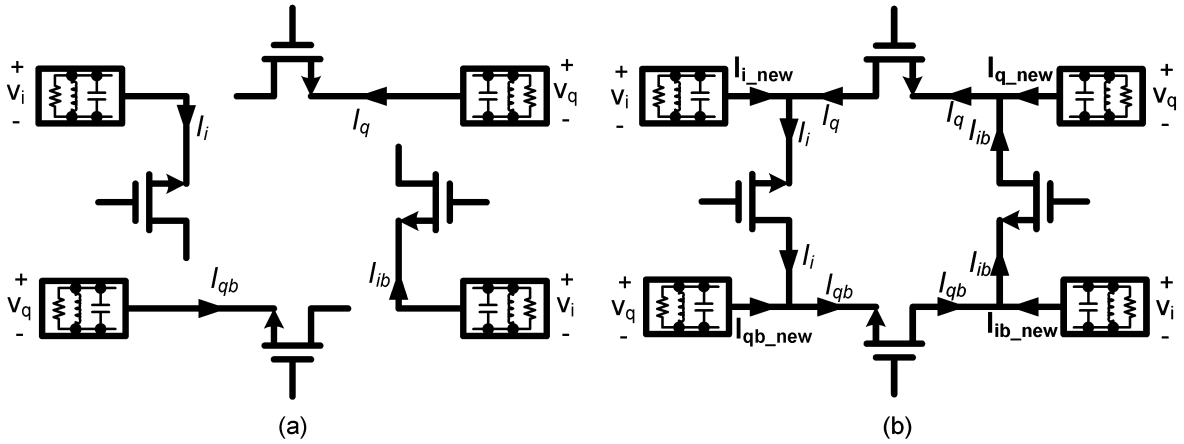


Fig. 8. (a) Initial quadrature currents applied to disconnected mixer loop (b) new regenerated quadrature current with the mixer loop reconnected.

By inserting (2) and (4) into (5), we get

$$\left|\frac{H_N K(V_{\rm GS}-V_{\rm th})(-2-\eta\cos 2\phi+j\eta\sin 2\phi)}{H_N g_{m\_LP}+j\frac{2Q}{\omega_N}(\omega_o-\omega_N)}\right|\geqslant 1 \quad (6)$$

which determines the locking range of the WLR-ILDF as

$$\frac{\Delta\omega}{\omega_N}\leqslant\frac{H_N}{2Q}g_{m\_LP}\sqrt{\eta+\frac{\eta^2}{4}}. \quad (7)$$

Analytic inequality of (7) reveals insights for WLR-ILFD design: Increasing H_N/Q, device g_{m_LP}, or injection ratio η can effectively improve the locking range. This analysis is further validated by circuit simulations as shown in Fig. 7. For example, the locking range increases initially proportional to $\sqrt{\eta}$ and gradually shifts to η as the injection ratio increases. When η or input signal increases, the results between simulation and analysis begin to deviate due to small signal model inaccuracy at large signal situations. However, this analysis method does predict the trend well and give the intuitive design insight. Compared with the locking range of $\Delta\omega=(\omega_N/2Q)(V_i/V_o)$ deduced for traditional injection locked oscillators [10], the WLR-ILFD offers enhanced locking range by implementing sufficiently high $H_N g_{m\_LP}$.

B. Phase Accuracy

Cross-coupled differential pairs may resonate at slightly different frequencies due to circuit mismatches, which is the primary reason rendering the quadrature output phases deviating from their ideal values. In this WLR-ILFD, we add a central mixer loop to mitigate the problem. Assuming one differential pair resonates at the frequency of ω_N and the other resonates at a slightly different frequency of $(1+\chi)\omega_N$, the phase of output signals from each differential pair (i.e., θ_1 and θ_2) can be written, respectively, as

$$\begin{aligned}\theta_1&=-\tan^{-1}\frac{2Q(\omega_o-\omega_N)}{\omega_N}\\ \theta_2&=-\tan^{-1}\frac{2Q(\omega_o-(1+\chi)\omega_N)}{(1+\chi)\omega_N}+\frac{\pi}{2}.\end{aligned} \quad (8)$$

Where θ_2 can be further expanded using the Taylor series expansion and ignoring the high order terms when χ is infinitesimal

$$\begin{aligned}\theta_2(\chi)|_{\chi=0}&=-\tan^{-1}\frac{2Q(\omega_o-\omega_N)}{\omega_N}+\frac{\pi}{2}\\ &\quad+\frac{1}{1+\left(\frac{2Q(\omega_o-(1+\chi)\omega_N)}{(1+\chi)\omega_N}\right)^2}\\ &\quad\times\frac{2Q\omega_o}{\omega_N(1+\chi)^2}|_{\chi=0}\bullet\chi\\ &=-\tan^{-1}\frac{2Q(\omega_o-\omega_N)}{\omega_N}+\frac{\pi}{2}\\ &\quad+\frac{2Q\omega_o}{\omega_N}\chi.\end{aligned} \quad (9)$$

Consequently, we can approximate the quadrature phase deviation $\Delta\theta$ as

$$\Delta\theta=\theta_2-\theta_1-\frac{\pi}{2}=\frac{2Q\omega_o}{\omega_N}\chi. \quad (10)$$

This phase deviation without the central mixer loop effect is essentially equivalent to that of the traditional LC-ILFD. The equivalent quality factor Q of the resonant tank is about 5, which is not high for wide locking range and accurate phase considerations.

Nonetheless, the situation changes greatly when taking the central mixer loop effect into account. First of all, the tank-induced phase deviation causes the phase of resonator current vectors $(I_i, I_{ib}, I_q, I_{qb})$ to shift correspondingly.

This mixer loop effect may be analyzed by initially disconnecting the drain of mixers from the central loop [Fig. 8(a)] and inject phase-shifted initial currents $(I_i, I_{ib}, I_q, I_{qb})$ to the source of mixers. As the loop gets reconnected [Fig. 8(b)], regenerated output current vectors $(I_{i\_\rm reg}, I_{ib\_\rm reg}, I_{q\_\rm reg}, I_{qb\_\rm reg})$ can be related to initial current vectors by applying the *KCL* to each node along the loop:

$$\begin{aligned}\overrightarrow{I_{i\_\rm reg}}&=\overrightarrow{I_i}-\overrightarrow{I_q}=\overrightarrow{I_i}+\overrightarrow{I_{qb}}\\ \overrightarrow{I_{q\_\rm reg}}&=\overrightarrow{I_q}-\overrightarrow{I_{ib}}=\overrightarrow{I_q}+\overrightarrow{I_i}\\ \overrightarrow{I_{ib\_\rm reg}}&=\overrightarrow{I_{ib}}-\overrightarrow{I_{qb}}=\overrightarrow{I_{ib}}+\overrightarrow{I_q}\\ \overrightarrow{I_{qb\_\rm reg}}&=\overrightarrow{I_{qb}}-\overrightarrow{I_i}=\overrightarrow{I_{qb}}+\overrightarrow{I_{ib}}.\end{aligned} \quad (11)$$

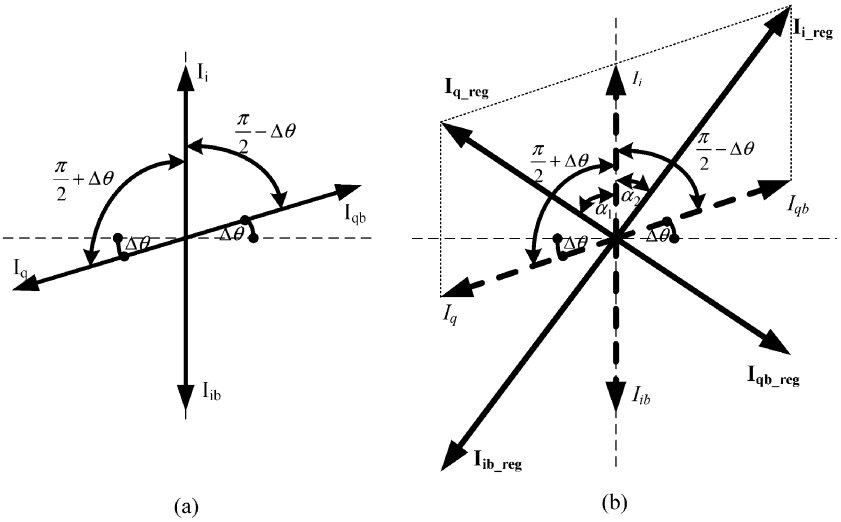


Fig. 9. (a) Phasor distribution of initial quadrature current vectors with phase deviation $\Delta\theta$. (b) Phasor representation of the relationships between initial currents and regenerated currents.

Fig. 9(a) and (b) represents the phasor relationships of original current vectors $(I_i, I_{ib}, I_q, I_{qb})$, and regenerated current vectors $(I_{i\_\mathrm{reg}}, I_{ib\_\mathrm{reg}}, I_{q\_\mathrm{reg}}, I_{qb\_\mathrm{reg}})$, respectively. As illustrated in Fig. 9(b), the angle difference of phasors $(\alpha_1 + \alpha_2)$ between the regenerated current vectors I_{i_reg} and I_{q_reg}, is affected by the initial tank current phase deviation $\Delta\theta$ and can be calculated according to simple trigonometry as

$$\alpha_1 = \arccos\left(\frac{I_i + I_q\cos\left(\frac{\pi}{2}+\Delta\theta\right)}{\sqrt{I_i^2 + I_q^2 + 2I_iI_q\cos\left(\frac{\pi}{2}+\Delta\theta\right)}}\right)$$
$$\alpha_2 = \arccos\left(\frac{I_i + I_{qb}\cos\left(\frac{\pi}{2}-\Delta\theta\right)}{\sqrt{I_i^2 + I_{qb}^2 + 2I_iI_{qb}\cos\left(\frac{\pi}{2}-\Delta\theta\right)}}\right) \quad (12)$$

and the regenerated phase deviation from the ideal quadrature value of $\pi/2$ becomes

$$\begin{aligned}\Delta\theta_{\mathrm{reg}} &= \alpha_1 + \alpha_2 - \frac{\pi}{2}\\ &= \arccos\left(\frac{I_i + I_q\cos\left(\frac{\pi}{2}+\Delta\theta\right)}{\sqrt{I_i^2 + I_q^2 + 2I_iI_q\cos\left(\frac{\pi}{2}+\Delta\theta\right)}}\right)\\ &\quad + \arccos\left(\frac{I_i + I_{qb}\cos\left(\frac{\pi}{2}-\Delta\theta\right)}{\sqrt{I_i^2 + I_{qb}^2 + 2I_iI_{qb}\cos\left(\frac{\pi}{2}-\Delta\theta\right)}}\right) - \frac{\pi}{2}.\end{aligned} \quad (13)$$

As noted in (13), we must first know the initial amplitude mismatch between I_i and I_q to obtain the regenerated current phase deviation. Since the amplitude mismatch of the current equals the voltage amplitude mismatch, we can calculate the current amplitude mismatch based on voltage amplitude mismatch. The voltage amplitude is determined by the cross coupled pair bias current I_{bias}, which is proportional to $I_{\mathrm{bias}}H_N$. H_N is the impedance of the tank.

$$\begin{aligned}V_i &\propto I_{\mathrm{bias}}H_N = I_{\mathrm{bias}}\omega_N LQ\\ V_q &\propto I_{\mathrm{bias}}H_N = I_{\mathrm{bias}}\omega_N(1+\chi)LQ.\end{aligned} \quad (14)$$

Therefore, the initial current amplitude has the same ratio:

$$\frac{I_q}{I_i} = \frac{V_q}{V_i} = (1+\chi). \quad (15)$$

When substituting (10) and (15) into (13), the phase deviation of regenerated currents becomes

$$\begin{aligned}&\Delta\theta_{\mathrm{reg}}\\ &= \arccos\left(\frac{1+(1+\chi)\cos\left(\frac{\pi}{2}+\frac{2Q\omega_o}{\omega_N}\chi\right)}{\sqrt{1+(1+\chi)^2+2(1+\chi)\cos\left(\frac{\pi}{2}+\frac{2Q\omega_o}{\omega_N}\chi\right)}}\right)\\ &\quad + \arccos\left(\frac{1+(1+\chi)\cos\left(\frac{\pi}{2}-\frac{2Q\omega_o}{\omega_N}\chi\right)}{\sqrt{1+(1+\chi)^2+2(1+\chi)\cos\left(\frac{\pi}{2}-\frac{2Q\omega_o}{\omega_N}\chi\right)}}\right) - \frac{\pi}{2}.\end{aligned} \quad (16)$$

The regenerative process iterates and progressively reaching a final phase deviation of $\Delta\Theta$ which can be closely correlated with the physical circuit simulation results as shown in Fig. 10(b) by simply fitting the formula of (16) with a constant factor K as given in (17). The value of K may depend on the design parameters, including bias conditions, choice of device sizes and tank characteristics.

$$\begin{aligned}&\Delta\Theta\\ &= \mathrm{K}\left\{\arccos\left(\frac{1+(1+\chi)\cos\left(\frac{\pi}{2}+\frac{2Q\omega_o}{\omega_N}\chi\right)}{\sqrt{1+(1+\chi)^2+2(1+\chi)\cos\left(\frac{\pi}{2}+\frac{2Q\omega_o}{\omega_N}\chi\right)}}\right)\right.\\ &\quad \left. + \arccos\left(\frac{1+(1+\chi)\cos\left(\frac{\pi}{2}-\frac{2Q\omega_o}{\omega_N}\chi\right)}{\sqrt{1+(1+\chi)^2+2(1+\chi)\cos\left(\frac{\pi}{2}-\frac{2Q\omega_o}{\omega_N}\chi\right)}}\right) - \frac{\pi}{2}\right\}\end{aligned} \quad (17)$$

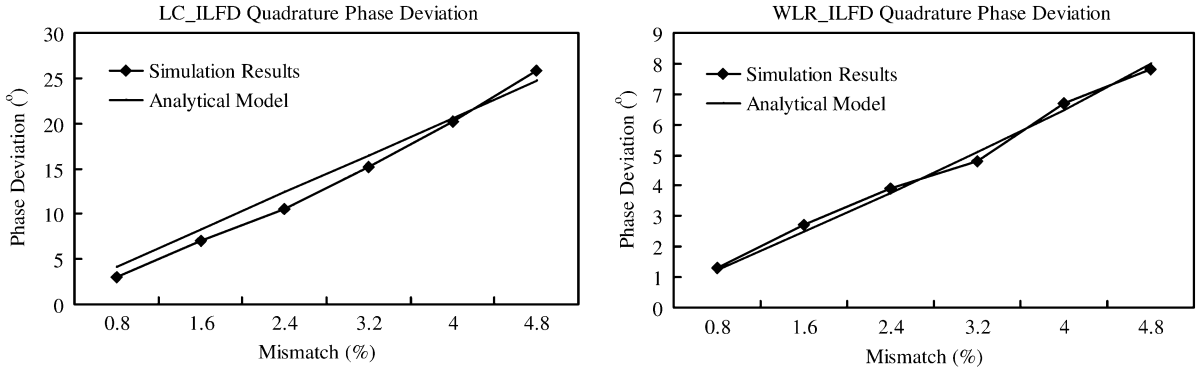


Fig. 10. (a) Traditional LC_ILFD phase deviation simulation results and analytical model results versus mismatches. (b) Proposed WLR_ILFD phase deviation simulation results and analytical model results versus mismatches.

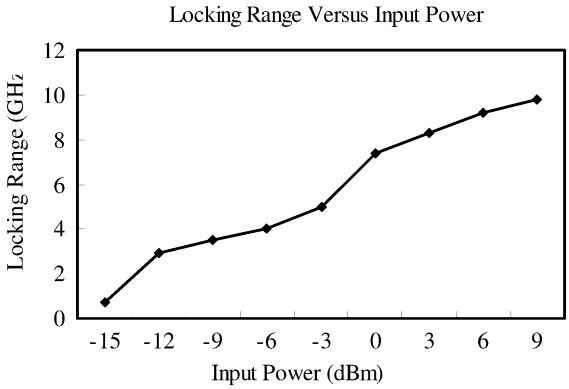


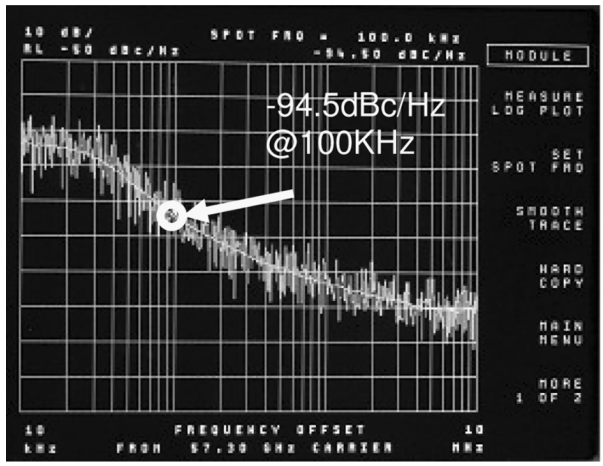
Fig. 11. Measured locking range versus input power.

Since both voltage and current signals share the common phase relationship, the phase deviation for the final quadrature output voltage signals should be $\Delta\Theta$ as well.

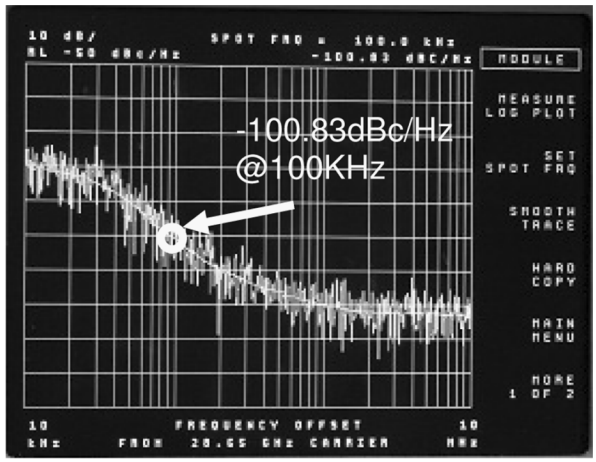
The superiority of WLR_ILFD in accurate quadrature phase generation is clearly demonstrated in Fig. 10, where we compare the quadrature phase deviation of the traditional LC-ILFD and the new WLR-ILFD via the analytical formula deduced in (17) and the physical circuit simulation based on 90 nm device models offered by the commercial Foundry. Both analytical and simulation results consistently confirm about 3 times stronger resilience of the new WLR_ILFD in quadrature phase deviation (about 1.7° per 1% of circuit mismatch) versus that of the LC-ILFD (about 5° per 1% of circuit mismatch) in defying the phase deviation introduced by circuit mismatches.

IV. Measurement Results

To validate WLR-ILFD topology, one prototype has been designed, fabricated and measured in TSMC 90 nm CMOS technology. Fig. 11 shows the dividing input frequency range increases versus input power. It is noted that the locking range increases from 700 MHz with −15 dBm input power to 7.4 GHz (53.4 to 60.8 GHz) with 0 dBm input power. The output signal levels with 53.4 GHz and 60.8 GHz inputs are about −7 dBm. Fig. 12 plots the phase noise for both input and output signals, which shows that the output signal phase noise is 6.33 dB below that of input phase noise. The reduction exceeds the theoretical value of 6 dB possibly due to spectrum analyzer limited



(a)



(b)

Fig. 12. (a) Input signal phase noise at 57.3 GHz. (b) Output signal phase noise at 28.65 GHz.

power measurement accuracy and phase noise measurement averaging effect. The die photo is given in Fig. 13 with a core area of 100 μm × 150 μm. Table I compares the performance of this WLR-ILFD with other state-of-the-art in terms of operation frequency, locking range, power consumption and Figure of Merit (F.O.M.), which is defined by the operation frequency

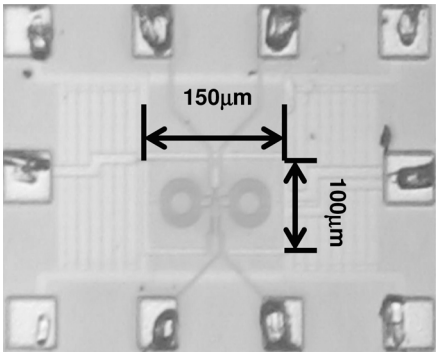


Fig. 13. Die photo.

TABLE I
COMPARISONS WITH THE STATE-OF-THE-ART

	[11]	[12]	[13]	**This work**
Technology	0.15μm GaAs	0.2μm CMOS	0.18μm SiGe	**0.09μm CMOS**
Operation Frequency	64GHz	55GHz	60GHz	**57GHz**
Locking Range	2.81GHz	3.2GHz	350MHz	**7.4GHz**
Power Consumption (normalized to diff. outputs)*	7.5mW	10.1mW	25.2mW	**2.5mW**
FOM (GHz/mW)	8.5	5.45	2.38	**22.8**

* This work and ref [13] offer quadrature outputs.

divided by power consumption. According to Table I, the proposed WLR-ILFD achieves widest locking range (7.4 GHz), highest F.O.M. (22.8 GHz/mW).

V. CONCLUSION

A new WLR-ILFD topology for injection locked frequency divider has been devised to achieve high dividing frequency, wide locking range and quadrature phase outputs by combining the strengths of both LC-ILFDs and RO-ILFDs. The dividing mechanism and quadrature phase accuracy are analyzed and the results agree well with circuit simulations. A WLR-ILFD prototype is fabricated in TSMC 90 nm CMOS technology and has realized the highest locking range (7.4 GHz) simultaneously with the highest dividing efficiency (22.8 GHz/mW) to date for V-band applications. This topology is also confirmed to be 3 times stronger in its resilience to quadrature phase deviation than that of the conventional LC-ILFD.

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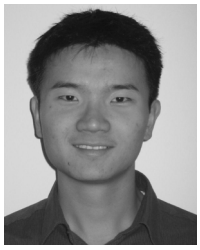

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Prof. Chang was elected to the National Academy of Engineering in 2008 and received the prestigious IEEE 2006 David Sarnoff Award for developing HBT power amplifiers and leading to their commercialization in wireless communications. He also received Rockwell's Leonardo Da Vinci (Engineer of the Year) award in 1992, National Chiao-Tung University's Distinguished Alumnus Award in 1997 and National Tsing-Hua University's Distinguished Alumnus Award in 2002. He was named an IEEE Fellow in 1996 for his pioneering contributions in ultrahigh-speed HBT integrated circuit development. Since 1997, Dr. Chang has founded a communication chip-design company in 2001 (now SST Communications after acquired by SST in 2004). He is currently Vice Chairman and Chief Technical Advisor of SST Communications Corporation.