1. Implement the equation: \( x = \left( \overline{a + b} \right) \left( \overline{c + d} + \overline{e} \right) \overline{f} \) using complementary CMOS.
   Size the devices so that the output resistance is the same as that of an inverter with an nMOS \( w/l = 1 \) and pMOS \( w/l = 2 \).
   a. Suggest an implementation that will be fastest (in your view)
   b. Show the critical path of your implementation

2. Derive the equation for CMOS power: \( P = kCV^2 f \) from the up and down transition of the CMOS inverter, as shown in class. (hint: transistors are working in linear region and saturation).

3. Using H-SPICE and standard transistor models simulate your circuit in 1. and find the critical path (worse case delay). Consider alternate implementations and check if your suggestion in 1(a) was correct.