Problem 1.1: 4-input NAND gate, \( F = A \cdot B \cdot C \cdot D \)

Problem 1.2:  \( F = AB + BC + AC \)

It's best to use Karnaugh map:

- Logic for NMOS = \( AB + BC + AC \)
- Logic for PMOS = \( \overline{A} \overline{B} + \overline{B} \overline{C} + \overline{A} \overline{C} \)
Problem 1.3: 3-input OR gate.

\[ F = A + B + C = \overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C} \]

Two possible implementations.

Simple circuit; need inverting input.  

Problem 1.4: 4-input multiplexer.

You can use one 4:1 MUX or three 2:1 MUX's.

Preferred, using less transistors.
Problem 1.5

In layout, lines of same material cannot cross. You will face that often in your layout. The common solution is to switch to a different material over the crossing to eliminate it.
Problem 1.6. S-R latch

Output: undefined, set, reset, hold