1.8 Exercises

1.1 Design a 4-input NAND gate using CMOS switch elements. Draw the full transistor circuit for the function.

1.2 \( F = \overline{AB} + BC + \overline{AC} \) implements a complemented carry function. Design a complementary CMOS gate to perform this function.

1.3 Design a 3-input OR gate. To what conclusions do you come?

1.4 A 4-input multiplexer structure is needed to multiplex four busses to a register in a microprocessor. Show two ways in which this may be implemented. Can you think of any reasons why one method is preferable to the others?

1.5 Using graph paper and colored pencils, complete a symbolic layout for the gates designed in Exercises 1.1, 1.2, and 1.3. What problems do you encounter?

1.6 Design and complete a symbolic layout for a CMOS memory element other than that shown in Fig. 1.11. Include waveform sequencing required for operation.