Recommended Reading:
Charles E. Leiserson, James B. Saxe, “Retiming Synchronous Circuitry”, Algorithmica 6(1): 5-35 (1991) (or you can use a similar version which is available online as a HP (former DEC and then Compaq) technical report)

Problem 1: The following block diagrams represent hardware realization of several streaming applications (e.g., filters). $D$ denotes the number of registers (delay elements) initially placed on a particular edge, and $x(n)$ and $y(n)$ represent input and output streams, respectively. For each design:

a) What is the implemented function in terms of input and previous output samples?

b) Improve the maximum clock frequency of the design using retiming. What is the initial and final clock period? Assume that addition and multiplication operations take one and two units of time, respectively.

Problem 2: Extend the retiming technique discussed in class to minimize the number of registers in a design (rather than optimizing the clock period).