Reading for this week

1. Kilburn T., D. B. G. Edwards, and D. Aspinall, "Parallel Addition in Digital Computers: A New Fast "Carry" Circuit", Proceedings of IEE, Vol 106, pt B, p.464, September 1959.

2. V. G. Oklobdzija and E. R. Barnes, "Some Optimal Schemes For ALU Implementation In VLSI Technology," *Proceedings of the 7th Symposium on Computer Arithmetic ARITH-7*, pp. 2-8. Reprinted in *Computer Arithmetic*, E. E. Swartzlander, (editor), Vol. II, pp. 137-142, 1985.

3. V. G. Oklobdzija and E. R. Barnes, "On Implementing Addition In VLSI Technology," *IEEE Journal of Parallel and Distributed Computing*, No. 5, pp. 716-728, 1988.

4. V. G. Oklobdzija, "Simple And Efficient CMOS Circuit For Fast VLSI Adder Realization", *Proceedings of the International Symposium on Circuits and Systems*, pp. 1-4, 1988.

5. A. Weinberger and J. L. Smith, "A Logic for High-Speed Addition", National Bureau of Standards, Circ. 591, p.3-12, 1958.

6. A. Naini, D. Bearden and W. Anderson, "A 4.5nS 96b CMOS Adder Design", Proceedings of the IEEE Custom Integrated Circuits Conference, May 3-6, 1992, p 25.5.1 - 25.5.4.

7. B. D. Lee and V. G. Oklobdzija, "Improved CLA Scheme With Optimized Delay," *Journal of VLSI Signal Processing*, Vol. 3, No. 4, pp. 265-274, 1991.

8. H. Ling, "High-Speed Binary Adder", IBM J. Res. Dev., vol.25, p.156-66, 1981.

9. R. W. Doran, "Variants on an Improved Carry Look-Ahead Adder", IEEE Transactions on Computers, Vol.37, No.9, September 1988.