and significant than papers reporting results obtained before an established deadline which is usually many weeks before a conference starting date.

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Comment†

The desirability of having good technical meetings is clearly a noncontroversial objective, and few would quarrel with the concern that L. Fein expresses in his letter. However, on a somewhat second-order level, I have some doubts concerning the solutions he proposes.

In his list of five objectionable aspects of present meetings, three—Items 1), 3), 4)—are related to procedure. Many of the recent technical meetings (*e.g.*, the AFIPS Conferences) have been planned with recognition of these and other problem areas. Item 3) does not appear to be relevant, unless the Program Chairman feels compelled to minister to the needs of the nontechnical, majority (?) group. I agree with Item 5) (too many meetings), but with reservations, as noted below.

The format he proposes, with four kinds of sessions, is a good idea, and should be helpful. However, procedures and formats by themselves are not sufficient, and other essential aspects must be considered.

The following suggests a general approach which may meet Dr. Fein's objections, but which would provide some leeway for the meeting and program committee:

1) Be sure that a need for the meeting exists. This statement is uncomfortably close to being a platitude. However, it is painfully apparent that this elementary and obvious aspect has not been considered in some past meetings. Conscientious attempts to meet this requirement would probably reduce the total number of meetings. It is possible, however, that the total number would actually increase, but with the likelihood that many of these meetings would be concerned with specific, well-defined objectives (such as meetings devoted exclusively to sales topics, or to specialized technical areas, etc.).

2) Make a distinct separation between the technical portions of the meeting and the commercial aspects. The separation may extend to the point of having separate meetings, or, at the very least, to differences in time and location of these two major items.

3) Accept papers for publication only after review of the complete text (similar standards to be applied both to volunteered and to invited papers). The review should be uncompromising in its quality standards.

4) Leave room, as Fein suggests, for informal discussion. If the talks are unreviewed prior to presentation, the attendees should know of this.

The mild objection I have to L. Fein's letter is this: He has presented some problems and proposed a solution. The problems, as defined, are somewhat exaggerated, and he takes no cognizance of the conscientious attempts which are being made to solve them. Many aspects of his prescription have been used, and since the objections he voices still exist, there must be more to be done. His letter is a good start towards initiating a discussion which, I am sure, will result in no unanimity of opinion, but which should provide valuable guides for the planning of future meetings.

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Chairman, Conference Committee
IEEE—PTGEC

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Ultimate-Speed Adders*

Lehman and Burla [1] in their TRANSACTIONS paper describe the "skip-carry" binary adders, by which an attractive compromise between speed and diode expenditure is achieved. Their paper includes a comparison of the speed and diode expenditures of several competing types of binary adders. They conclude that, except for the possible implications of accounting for the systems in which the adders are imbedded, a properly designed skip-carry adder is the fastest for a given expenditure of diodes, as well as the most economical in diodes for a given computational speed. In particular the conditional-sum adder appears in their paper to have lost the speed superiority it had in an earlier analysis [2], [3].

In this correspondence we present a point of view by which "conditional logic" and its related technique "distant-carry logic" achieve addition speeds that in principle cannot be exceeded by skip techniques. We shall explain why we feel this point of view is both meaningful and useful for a certain type of hardware technology. Upper bounds on the realizable addition speeds are derived. The speeds of conditional-sum adders and distant-carry adders turn out to approach these bounds surprisingly closely.

I. WHICH ADDER IS THE FASTEST?

The extent to which the "speed" of an adder contributes to the over-all value or effectiveness of a computer depends, of course, on quite a complex function of the costs of engineering, fabrication, operation, and maintenance of the entire computer [2]. Hence when one evaluates the utility of an entire computer the speed of the adder is likely to be drowned in a complicated sea of economic and engineering considerations.

Consequently the question, "Which adder is the fastest?" is an impossibly difficult question if we define adder speed as the contribution of an adder to over-all computational effectiveness. On the other hand it is possible to obtain a meaningful answer if we constrain the class of adders to those adders that produce in a parallel fashion a binary sum from two binary summands. We call these the "binary parallel adders."

At this point we find that we still cannot answer the proposed question, for the following reason: we have not yet defined a unit of addition time. The natural unit to adopt is the delay of a single AND gate or OR gate. In practice, however, the speeds of these gates are dependent on several factors, of which gate delay is only one. Among these other factors are the fan-in and fan-out capacities of the individual gates. In fact, when certain high-speed hardware is used, the fan-in/fan-out capacities are critical parameters forming bounds on the logic speed. More will be said about this in Section II.

When in this communication we answer the question, "Which adder is the fastest?" we shall really be answering the following more restricted question, "Which binary parallel adder consumes the fewest gate delays in adding two summands, under the constraint that the fan-in and fan-out capacities of the individual gates do not exceed certain specified limits?"

Now we ask ourselves, "How useful is the answer to the above relatively constrained question?" *i.e.*, "Is the class of adders under consideration so narrow that the answer is neither interesting nor useful?" It turns out that practically all of the "fast" adders used in practice fall into two classes: the binary parallel adders and the redundant-number-system adders. (The latter class includes the separate-carry-storage adders.) We expect that under certain design specifications that binary parallel adders will be preferable. For these conditions a quantitative description of the speeds of the binary parallel adders in terms of fan-in/fan-out capacities, summand length, and diode count should be useful. Under other conditions, the redundant-number system offers an attractive approach [6].

A quantitative description of the speeds of binary parallel adders for the case of a fan-in capacity of two appears in an earlier paper [2], and is extended here to more general fan-ins and fan-outs. From this evidence we note the following: If the maximum permissible fan-in per gate is two, and if the admissible fan-out per gate is unrestricted, then the conditional-sum adder is the fastest known adder. (In Section II we discuss why a fan-in of two is realistic when certain high-speed hardware is used.) Empirical evidence also indicates that if—in addition to the fan-in constraint—fan-out is constrained to lie below or at a specified constant, then the conditional-sum adder is still the fastest known adder.

Why, then, does the conditional-sum adder appear slower than the carry-skip adder in the second example of Lehman and Burla's paper? (Hereafter we shall refer to the latter adder as the "Lehman-Burla example.") The reason is that the Lehman-Burla example is built of gates having fan-ins as large as eight, and that the delay of each of their multiple-input gates is equal to that of any other of their gates independently of the individual fan-ins. These multiple-input gates are practical when ordinary diodes are used; however, if high-speed devices such as

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tunnel diodes are used, the fan-in/fan-out constraint is much more severe.

In this correspondence we shall compare the Lehman-Burla example to the conditional-sum adder and at the same time try to maintain fairness in the matter of fan-in and fan-out maxima. To do this, one of the following approaches seems to be required: 1) Replace every multiple-input gate in the Lehman-Burla example by a binary tree of two-input gates, such as that in Fig. 6(a), and replace every multiple-output gate by a binary tree such as that in Fig. 6(b). 2) Extend the conditional-sum design approach in a manner that will take advantage of the availability of multiple-input gates with fan-in-independent delays.

The first approach raises both the addition time and diode expenditure of the Lehman-Burla example substantially above those of a 54-bit conditional sum adder. This is a consequence of the fact that both the over-all delay and the diode count of the tree network exceeds those of the corresponding multi-input gate. It seems that the Lehman-Burla example is poorly matched to two-input gates; hence the first approach is not fair to the skip-carry technique. The second approach has therefore been tried. The results are reported later in this letter.

II. Are Low Fan-Ins and Fan-Outs Realistic?

Although today fan-ins and fan-outs as large as 8 are realizable and often practical, computer technology is moving in the direction of very small fan-ins and fan-outs. The reason for this is that high speed and small geometric size are both highly valued properties of computer components. As gate geometry becomes smaller, gate gain also becomes smaller. Furthermore, the reduced fabrication precision resulting from a reduced gate geometry corrupts the signal resolution. Greater gate speed normally accompanies the smaller geometric size. This situation manifests itself empirically as a pseudo-gain-bandwidth-product limitation. Examples of this new technology are phase-locked oscillators, tunnel diodes, and microwave logic.

Consequently, it seems inevitable that computer circuit designers will soon be forced to deal with low-gain gates, *i.e.*, gates having low fan-ins and fan-outs.

III. Is There a Form of Conditional-Logic Adder to Which the Lehman-Burla Example May Be Fairly Compared?

That is, can conditional logic be extended in such a way that it will be efficient when the maximum permissible fan-in is three or more?

The answer is yes. The Lehman-Burla example makes use of gates for which $\gamma=8$ and $\delta=7$, where we define $\gamma \triangleq$ maximum permissible fan-in, $\delta \triangleq$ maximum permissible fan-out. To compare this fairly with a conditional-logic adder, we must permit ourselves the possibility of incorporating larger fan-ins and fan-outs in conditional-logic adders. This may be accomplished by raising the radix r of the adder to an integral power of 2, say $r=2^p$. We shall call p the "span." (Lehman-Burla's "group size" corresponds to our p.)

This results in a conditional sum adder in which binary-coded conditional sums and carries are generated for each r-ary digit. The number of gates becomes larger than that in the Lehman-Burla example, but the computation time—or, more accurately, the effective carry-production time—is reduced to $t=\hat{\log}_p (n+1)$, where n is the length of the summand register, t is the carry-production time defined by Lehman-Burla, and the circumflex indicates that $\hat{\log}_p x$ is the smallest integer not less than $\log_p x$.

When $p>2$, the resulting conditional-sum adder requires a maximum fan-in of $\gamma \cong p!$. On the other hand, a conditional-*carry* adder based on the same basic concept will require a maximum fan-in of $\gamma=p$. Furthermore the conditional-carry adder uses significantly fewer gates than the conditional-sum adder when $p>2$.

It turns out that the conditional-carry adder can be simplified further by the use of "auxiliary carries" in place of conditional carries. When this is done, lo and behold, we have the "simultaneous carry" adder described by Weinberger and Smith [4]! (Simultaneous carry logic has aso been known as "look-ahead carry" and "distant-carry" logic. We shall use the term "distant carry.") To compare the conditional-carry and the distant-carry logic, examine Figs. 1 and 2. Fig. 1 shows the basic conditional-carry logic for a span of 5; Fig. 2 shows the basic distant-carry logic for a span of 5. The next hierarchic level of distant-carry logic is illustrated in Fig. 3. (In Figs. 1–3, e and f are auxiliary carries, while c^0 and c^1 are conditional carries.)

Hence, it seems appropriate to compare the Lehman-Burla example with a fully layered distant-carry adder for spans of $3 \leq p \leq 8$. The results of such a comparison show that one may, by the distant carry technique, attain a carry-production time of

$$t = \tfrac{1}{2} + \hat{\log}_p (n+1)$$

where n is the summand length.[1] For example, if $p=8$, then $\log_p (n+1)=\log_8 (55)=1.93$. Consequently $t=2.5$. This value of t is five-eighths of the carry-production time in the Lehman-Burla example, achieved at a cost of an approximate doubling in the diode expenditure.

In the event $p=2$ and $\delta \geq n+3$, the conditional-sum adder will be faster than a distant-carry adder by the time $\Delta t=\frac{1}{2}$, because there is no need to assimilate carries in the conditional-sum adder.

IV. Numerical Comparison

Table I displays the results of a comparison of three fully layered 54-bit distant-carry adders with the Lehman-Burla example. Undoubtedly further simplifications of the distant-carry adders could be made (as, for example, was done by Weinberger and Smith [4]) in such a way as to reduce the diode expenditure without incurring a loss in addition time. No attempt at such simplifications, however, was made in this comparison.

Our version of the distant-carry adder with a span of 6 is shown in Fig. 4. The carry-production time and diode expenditure of this adder, as well as two other similarly structured adders with spans of 4 and 8, were computed and the results tabulated in Table I in the rows labeled DCA_p, p denoting the span. The last two columns of Table I show the numbers of extra diodes ΔD required to reduce the maximum fan-out, δ, to 7 and γ.[2] The value of 7 was chosen because this is the value of δ in the Lehman-Burla example. In all cases the extra diodes required for fan-out reduction are less than 6 per cent of the original number of diodes, D, and hence are not significant considerations.

We note in Table I that additional time must be bought at a disproportionate cost in diodes. However, it may be worthwhile in some instances to pay a 100 per cent increase in hardware for a 37 per cent reduction in addition time, since a time saving accumulates over the life of the computer. Therefore, Q is not necessarily the best figure of merit of the adders. Other figures of merit, such as $(t/n) \log D$ might result in more realistic relative standings [2].

The following tentative conclusion is also indicated in Table I: For a given addition time, the number of diodes is minimized by using the smallest possible span for the required summand length n. (This corroborates Lehman-Burla's design principle *b*.) Another tentative conclusion is that ΔD increases as p increases if δ is constant.

The following questions are stimulated by the remarks of Lehman-Burla in the last paragraph of their paper: 1) For a given addition speed, which adder expends the most diodes? 2) For a given diode expenditure which adder is fastest? Unfortunately, Table I cannot answer either of these questions directly. We believe, however, that skip-carry cannot achieve the speeds of fully layered distant-carry or conditional sum at *any* expenditure of diodes, because the latter two techniques give us adders whose addition times seem to approach the shortest that can be physically realized. In the next section we shall describe the evidence supporting this belief.

VI. What Is the Evidence Supporting the Thesis That Conditional-Logic and Distant-Carry Techniques Yield Near-Ultimate-Speed Adders?

Basically, addition speed is limited by gate delay and by fan-in and fan-out capacities of the individual gates.

Fig. 5 (p. 146) illustrates the interdependence of the sums and output carries of a six-bit adder on the summand bits in the preceding columns. Note that the maximum fan-in and fan-out indicated in the illustration are both equal to the summand length, namely 6. If the available fan-in and fan-out per gate are both less than 6, then clearly the addition time or carry-production time will necessarily be greater than a single-gate delay.

To determine a lower bound on the addition time or carry-production time, note from Fig. 6 (p. 146) how tree networks can implement large fan-ins and fan-outs with low-gain gates. Each of these tree networks is minimal both in its gate expenditure and

[1] We refer here to our version of the distant-carry adder, illustrated in Fig. 4.

[2] The encircled numbers in Fig. 4 indicate fan-out requirements of certain sections of the adder.

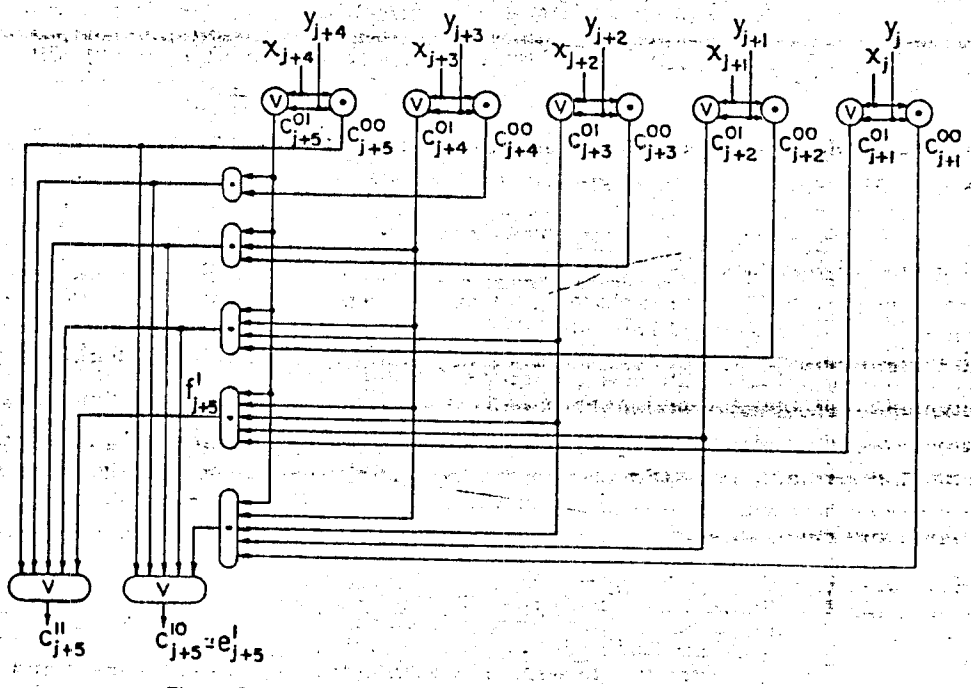


Fig. 1—Conditional carry selector for a span of 5 at level 1 (denoted as K_5).

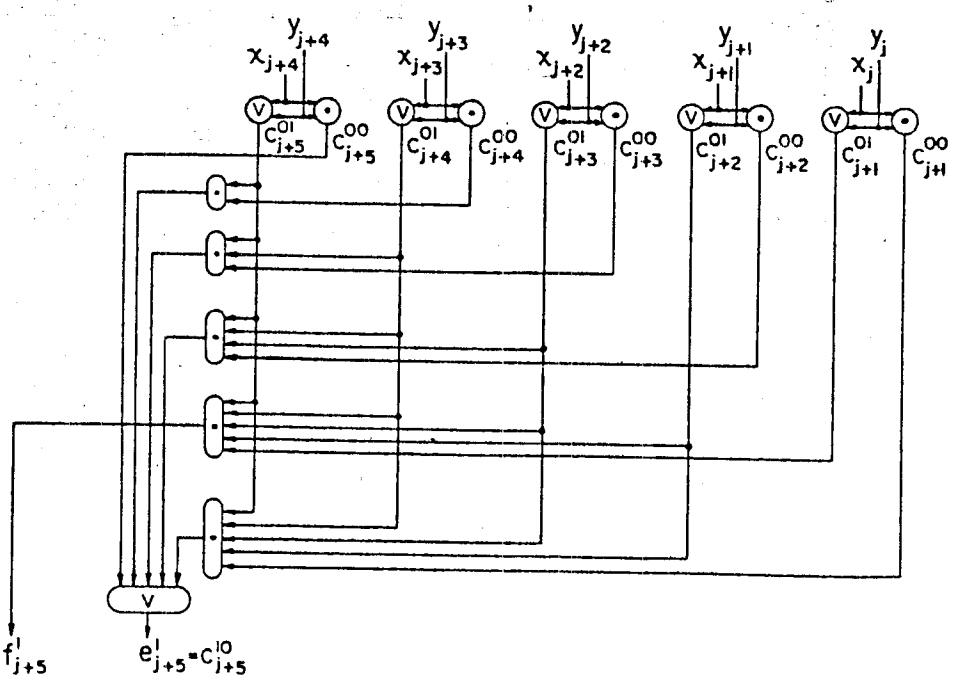
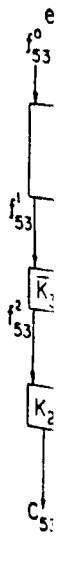


Fig. 2—Auxiliary carry selector for a span of 5 at level 1 (denoted as $\overline{K_5}$).



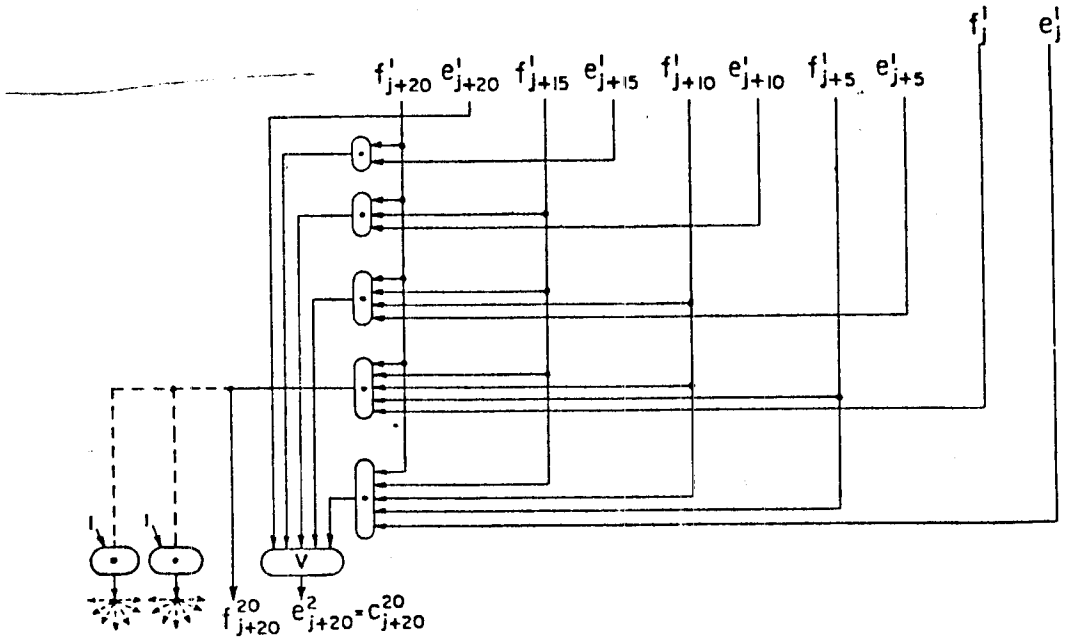


Fig. 3—Auxiliary carry selector for a span of 5 at level 2 (denoted as $\overline{K_5}$). Dotted lines indicate how fan-out of one of the auxiliary carries may be increased.

TABLE I

	t	$100\,t/n$	D	D/n	Q	γ	δ	ΔD $\delta=7$	ΔD $\delta=\gamma$
Lehman-Burla	4	7.4	1014	18.8	17	8	7	0	0
DCA_4	3.5	6.48	1376	24.6	19.9	4	40	31	75
DCA_6	3.5	6.48	1610	28.7	23.2	6	39	34	42
DCA_8	2.5	4.63	2127	38.1	22.1	8	70	64	53

$t \triangleq$ carry-production time.

$t_0 \triangleq$ carry-production time of a pure ripple-carry adder.

$D \triangleq$ number of diodes.

$n \triangleq$ summand length.

$Q \triangleq 100\,tD/(t_0 D_0)$, where $D_0 \triangleq$ number of diodes in a pure ripple-carry adder.

$\gamma \triangleq$ maximum permissible fan-in per gate.

$\delta \triangleq$ maximum permissible fan-out per gate.

$\Delta D \triangleq$ additional diodes needed for fan-out reduction.

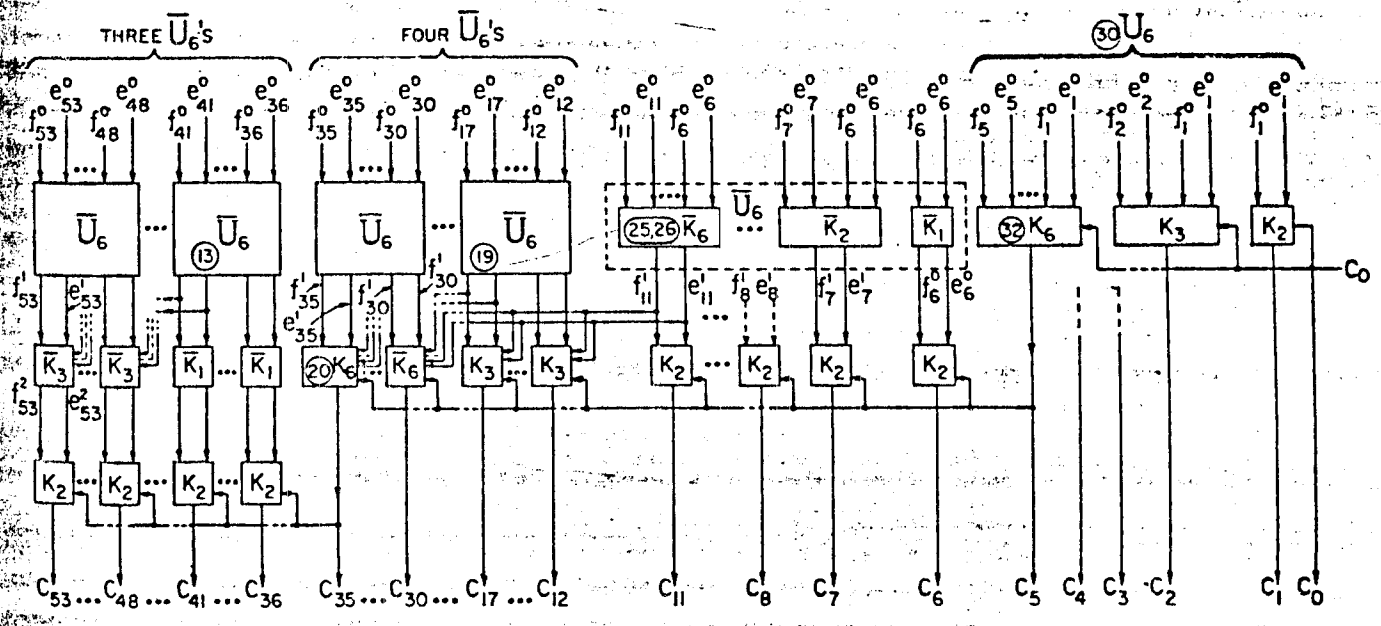


Fig. 4—A fully layered distant-carry adder with a span of 6.

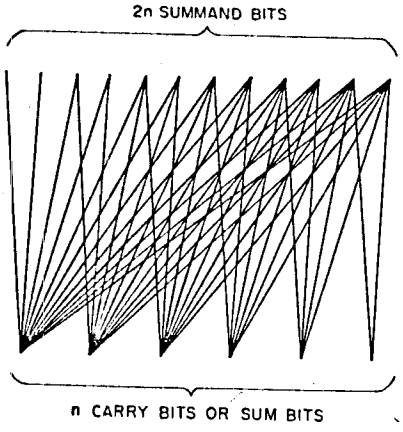


Fig. 5—Pattern of fan-in and fan-out for a six-bit adder ($n=6$)

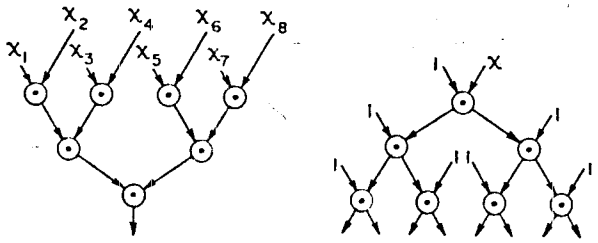


Fig. 6—Circuits for (a) increasing the fan-in and (b) increasing the fan-out.

its over-all delay provided the available gates have maximum permissible fan-ins (or fan-outs) equal to the number of converging (or diverging) branches at each node of the tree.

Returning to Fig. 5, note that information on the column 0 summand bits must reach column 5 as part of a fan-out of 6 emanating from column 0. Implementing this fan-out by a tree network contributes $\lceil \log_\delta n \rceil$ gate delays to the addition time. (We define $\lceil \log\ x \rceil$ as the smallest integer not less than $\log x$.) Note also that the sum and output-carry bits of column 5 are dependent upon $2n$ summand bits; hence the generation of the sum and output-carry bits at column 5 requires an effective fan-in of $2n$. Implementing this fan-in by a tree network contributes $\lceil \log_\gamma 2n \rceil$ gate delays. Since the tree networks impose minimal over-all delays for given γ and δ, the over-all addition time or carry-production time cannot be less than Max $[\lceil \log_\gamma 2n \rceil, \lceil \log_\delta n \rceil]$ gate delays. Note that Lehman-Burla's definition of t is one half the number of gate delays.[3] Hence,

$$t_* \geq \tfrac{1}{2} \text{ Max } [\lceil \log_\gamma 2n \rceil, \lceil \log_\delta n \rceil] \qquad (1)$$

where t_* is defined as the shortest realizable addition time or carry production time.

An analysis of the distant-carry adder shows that the carry-production time of this adder is

$$t_{DCA} = \lceil \log_\gamma (2n+2) \rceil + \tfrac{1}{2} \lceil \log_\delta \left(n+1-\frac{n+1}{\gamma} \right) \rceil. \qquad (2)$$

[3] We assume in our analysis that the delays of AND gates and OR gates are equal. This assumption is not needed in Lehman and Burla's analysis, because in their circuits AND gates and OR gates separate each other. In our circuits we sometimes use cascades of AND gates or OR gates to build fan-ins or fan-outs exceeding the gate capacities.

An analysis of the 2-span conditional-sum adder gives the following addition time:

$$t_{CSA} = \lceil \log_2 (2n+2) \rceil + \tfrac{1}{2} \lceil \log_\delta \left(\frac{n+1}{2} \right) \rceil. \qquad (3)$$

When $\delta=\gamma$ and n is large, the addition/carry-production times of both the direct-carry adder and the conditional-sum adder are approximately three times the lower bound indicated in the right member of (1). On the other hand, when $\delta \ll \gamma$, then t_{DCA} and t_{CSA} are almost equal to the right member of (1). Hence in the fan-out-limited case the conditional-sum adder and direct-carry adder seem to approach the ultimate in speed. For the cases where $\delta \approx \gamma$ or $\delta \gg \gamma$ then the *CSA* and *DCA* are not necessarily ultimate-speed, but analysis under the fan-in/fan-out constraint indicates that they are the fastest known adders. [In particular, when $\gamma=2$, the conditional-sum adder is faster than the direct-carry adder; for $\gamma>2$ the *CSA* is out of the running altogether, because its fan-in requirements seem to be proportional to P!.

When $\gamma \ll \delta$, the sum/carry processing times of the conditional-sum adder and direct-carry adder are about twice the right-hand member of (1). At first sight this factor of two might appear large. Upon reflection, however, we see that it is, in fact, surprisingly small. The normal-form realization of a general Boolean function of $2n$ variables requires as many as 2^{2n-1} AND gates (or OR gates) feeding an OR gate (or AND gate). Imposing the fan-in constraint, we must replace the $2n$-input AND gates and the 2^{2n-1}-input OR gate by tree networks of the form of Fig. 6(a); furthermore, internal fan-outs as large as 2^{2n-1} in the normal-form network may have to be implemented by tree networks of the form of Fig. 6(b). Hence we expect that implementing a $2n$-variable Boolean function will generally require many more gates and will consume much more delay than that of a single-tree network.

In fact we would expect from these considerations that the ratio $t_*/\log_\gamma 2n$ will increase rapidly as n increases. Hence it is surprising (and gratifying) that $t_*/\log_\gamma 2n$ remains approximately constant at the value 2 independently of the size of n when $\gamma \ll \delta$. (The factor of two can be explained by the fact that each AND gate must be followed by an OR gate when $\gamma \ll \delta$.)

We suspect, therefore, that this factor of two represents very nearly the ratio between ultimate realizable speeds and the upper bound implied by (1) when $\gamma \ll \delta$.

VII. A Few Miscellaneous Items

1) The carry-skip or "look-ahead" technique is a combination of distant-carry logic [4] and ripple-carry logic [5]. It is possible to have a pure ripple-carry logic, and it is possible to have a pure distant-carry logic, but it is not possible to have a pure carry-skip logic.

2) Fig. 4 of the Lehman-Burla paper [1] is a hybrid of a fully layered distant-carry adder and a ripple-carry adder. Hence certain parts of the ripple-carry logic are superfluous. In particular, the lower right-hand AND gate in each ripple-carry tetrad of gates for columns $i+1$ to $i+5$ may be deleted. The resulting circuit has the form of our Fig. 2, if we delete from Fig. 2 the gate forming the auxiliary carry f^1_{i+5}.

3) The effective carry-production time of the 54-bit conditional-sum adder is $t=6$ rather than the 5.5 listed in Lehman-Burla's Table II. Apparently Lehman and Burla noted that the conditional carries in the *H* modules of Fig. 2 of Sklansky [3] are produced in $\Delta t=1/2$. However, the conditional-sum bits in these modules consume $t=1$. In the columns covered by the last layer of conditional logic, the final-sum bits cannot be produced until the conditional-sum bits in the earlier layers are transmitted downward. Hence the sum-bit-propagation time, rather than the carry-propagation time, determines the speed of this adder.

4) Lehman-Burla's computation of the addition time for the "simultaneous-carry" adder is $t=4$, while we compute $t=3.5$ for our version of the same type of adder. An analysis of Weinberger and Smith's 53-bit adder (Fig. 10 of [4]) also yields $t=3.5$.

VIII. Summary and Conclusions

1) The following inequality describes a lower bound on the physically realizable addition or carry production time of an n-bit binary adder:

$$t_* \geq (1/2) \text{ Max } [\lceil \log_\gamma 2n \rceil, \lceil \log_\delta n \rceil].$$

2) Conditional logic and distant-carry logic are strongly related.

3) Conditional-sum adders are the fatest known adders when the maximum permissible fan-in, γ, is two. (This low fan-in is realistic for certain types of high-speed hardware being developed today.) When $\gamma=2$, distant-carry adders are both faster and require fewer gates than conditional-sum

adders. There is some reason to believe that the speeds of the conditional-sum adder for $\gamma=2$ and the distant-carry adder for $\gamma>2$ are the ultimate achievable or very nearly so.

4) Skip-carry adders are hybrids of distant-carry logic and ripple-carry logic. These adders achieve a reduction in diode expenditure over that of pure distant-carry logic at the cost of a less-than-proportionate reduction in speed.

5) For a prescribed maximum acceptable addition time, the gate expenditure of distant-carry and conditional-logic adders seems to be minimal when the span is made as small as possible. This corroborates an observation by Lehman and Burla.

6) It would be worthwhile to attempt to improve the logical design of distant-carry and conditional-sum adders in such a way as to bring their diode expenditures close to that of skip-carry adders without any concomitant speed reduction.

ACKNOWLEDGMENT

The writer is grateful to M. Lehman of the Israel Ministry of Defence and to R. O. Winder, H. S. Miiller, and S. Amarel of RCA Laboratories for their critical comments.

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Dr. Lehman's Comments

Having been permitted a preview of the note by Sklansky commenting on a paper by Burla and myself [1], I should like to make the following remarks.

Continued study of the binary adder design problem in connection with the preparation of a paper presented at the IFIPS 1962 Congress [7], and further thought since, has convinced me that the search after a "best," a "fastest" or a "most efficient" circuit is futile. In any attempted optimization, whatever the criterion, the circuit and performance specification must be most clearly stated, since a "best" circuit for 50-bit words, for one-Mc circuitry, or when using transistors may be quite out of the running for 10- or 100-bit words, at nanosecond speeds or when using tunnel diodes. Furthermore, in most applications, it is the probable maximization of machine utilization which is of ultimate significance. Minimization of carry propagation or addition time is not necessarily the only or the best way to achieve this. Moreover at the highest speeds the logically faster circuit is not necessarily physically faster. Increased cabling and higher component densities in the more complex circuits may often do more harm than good.

Studies of the type undertaken, in connection with binary adder circuits, by Sklansky, by Burla and by myself are of importance nevertheless, in that they lead to a fuller understanding of the circuits and of the principles underlying them.

The ideas expressed above are probably universally acceptable. Where Sklansky and I differ is in our assessment of the future of the device (gate) with small fan-in and small fan-out. Being far closer to the source of new ideas than I am, Sklansky should be better informed of present trends in component and circuit developments and design. Where a genuine need exists, however, a solution can usually be found for most problems. Thus I believe that in the future too, devices with fan-in and fan-out each of order five or more will be perfectly practical, yielding circuits as fast as and probably cheaper than those based on gates with more restricted operating conditions. Thus the theoretical analysis of Sklansky's Section VI appears of little practical importance. His lower bound for attainable speed in a limited class of adders is interesting but surely it is precisely those cases which he does not consider which are of significance. How realistic is an assessment based on circuits with a fan-in of two and a large or even unrestricted fan-out, for example?

The value of an adder comparison excluding the class of redundant-number-representation circuits is also to be doubted, but even in his restricted class Dr. Sklansky does not, for example, include skip or pyramid circuits except in the vaguest terms.

Thus I do not believe that Sklansky has satisfactorily answered his question, "Which is the faster adder?" In fact this question appears to me to be meaningless. If, as seems reasonable, we define an adder as the physical realization of some logical scheme for achieving (binary) addition within some larger system, no absolutely "fastest adder" can exist.

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Dr. Sklansky's Reply

I am very grateful to Dr. Lehman for his comments. They are perhaps representative of the point of view of the logical designer strongly motivated toward over-all machine effectiveness and economy.

My over-all reaction to his comments is that they seem to originate from a misunderstanding of the principal theme of my correspondence. That theme is *not*, "What is the fastest adder?" It is, rather, a continuation of a discussion, begun by Lehman and Burla in their paper [1], on the question, "What are the relative logical speeds of parallel binary adders—in particular, skip-carry adders—and at what cost in diode expenditure are these logical speeds achieved?" The correspondence was an attempt to show 1) that fan-in/fan-out considerations will change the relative standings of the papers considered in the Lehman and Burla paper, in particular the conditional-sum and distant-carry (or "simultaneous-carry") adders, and 2) that as a hybrid between ripple-carry and distant carry, there is little hope that a skip-carry adder can achieve the logical speeds of distant-carry logic under *any* diode expenditure, for a given fan-in/fan-out constraint. My discussion of upper bounds on addition speeds was intended to lend a certain plausibility to 2), although admittedly these bounds are not tight enough to constitute anything more than an argument. The discussion of these bounds was not based on the assumption of low fan-ins—as Dr. Lehman seems to imply—although the case $\gamma \ll \delta$ did receive special attention for mathematical reasons, not for its practical interest.

I agree with Dr. Lehman in his contention that devices with fan-ins and fan-outs of order five to ten will remain practical for a long time, in spite of the fact that the advent of nanosecond circuitry points to low fan-in/fan-out as a problem to live with at very high operating frequencies. The correspondence, however, does not address itself only to low fan-in circuitry—it emphasizes that no matter what the fan-in/fan-out of the available hardware may be, the fan-in/fan-out size should be a significant parameter in any comparison of logical speeds. Thus in Table I of the correspondence, adders with relatively high fan-in/fan-out are compared.

Dr. Lehman questions the utility of considering circuits having a low fan-in (in particular, a fan-in of two) and a large fan-out. My answer to this is at the logical design level rather than at the component-design level: A component having a low fan-in and high fan-out may be replaced by a tree of similar components in which the fan-out per component is as low as desired. In many distant-carry and conditional-sum adders of practical interest, such a replacement will not incur a reduction in the over-all logical speed. This is the case for the adders discussed in Section IV of the correspondence. The number of diodes consumed in such a replacement are given in the last two columns of Table I.

Dr. Lehman brings forth the embarrassing question of the utility of this entire discussion—including, by implication, the Lehman-Burla adder comparison—when he casts doubt on the value of an adder comparison that excludes the class of redundant-number-system circuits. The correspondence was a response to the Lehman-Burla comparison, and retained the same framework of discussion, including the implied assumption on the utility of the discussion itself. My feelings on Dr. Lehman's doubt-casting are: 1) that parallel binary adders have not yet been made obsolete by any means (where by "parallel binary adders" we exclude redundant-number-system adders), and 2) that parallel binary adders are relatively easy to compare analytically—which means we can obtain certain interesting and useful design information at relatively little effort.

Dr. Lehman goes on to object that even within the class of parallel binary adders, the correspondence is not sufficiently comprehensive, apparently because it does not bring the same quality and intensity of discussion to such circuits as the skip-carry and the pyramid adders as it does to the distant-carry and the conditional-sum adders. Again this reflects a certain amount of misunderstanding of the principal aim of the correspondence, which was to demonstate the importance of the fan-in/fan-out constraint and to comment on Lehman and Burla's contention that skip-carry adders are

superior with respect to diode expenditure per unit of logical speed. With this aim in mind, I felt a discussion of adders other than distant-carry, conditional-sum, and skip-carry was unnecessary. Because the skip-carry adder is a hybrid of a ripple-carry adder and a distant-carry adder, because ripple-carry adders and the related carry-detection adders are slower on the average than distant-carry adders [2], and because distant-carry and conditional-sum adders seem to approach the ultimate in speed, I felt that a detailed general analysis of skip-carry adders was unnecessary, and that a single numerical example (Table I) would suffice to demonstrate my point.

The correspondence, by the way, should not be taken as a criticism of the skip-carry concept. It is, rather, a criticism of the evaluation of that concept.

References

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[4] A. Weinberger and J. L. Smith, "A one-microsecond adder using one-megacycle circuitry," IRE Trans. on Electronic Computers, vol. EC-5, pp. 65–73; June, 1956.
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The Fabrication of Low Resistances at Liquid Helium Temperatures*

The operation of linear cryogenic amplifiers, as well as other cryotron devices, often requires resistances that are extremely small, but nonzero. One means of obtaining such a resistance is to construct it of a short length of copper wire It is then necessary to know the value of the resistivity of copper at liquid helium temperatures. This resistivity is considerably lower than the room temperature value, and it will vary with the impurity levels, and somewhat with the temperature. A range of values for resistivity, which has been obtained experimentally, will be given here. This range should not be considered to represent the upper and lower limits of resistivity available but just to represent a small sample of values. These values are presented as a first approximation to the actual resistivity and should be used as such.

$$1.2 \times 10^{-8} \text{ ohm-cm} \leq \rho \leq 1.8 \times 10^{-8} \text{ ohm-cm.}$$

The copper wire used in these measurements was of "thermocouple grade."

When making soldered connections to these resistances care must be taken since the contact resistance resulting from improperly soldered connections may be many times the value of the desired load resistance. (There may be applications where load resistance in the order of 10^{-5} ohms or smaller is desired.) Contact resistances that are usually negligible become important in such cases. If clean unoxidized leads, which are carefully tinned, are used, these contact effects can be greatly reduced.

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