Reviewing 4-to-2 Adders for Multi-Operand Addition*

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Abstract

Recently there has been quite a number of papers discussing the use of redundant 4-to-2 adders for the accumulation of partial products in multipliers, claiming one type to be superior to other types. This paper analyses the use of various 3- and 4-element redundant digit sets for radix 2, and compare their adder implementations using various encodings of the digits and carries. It is shown that theoretically they are equivalent, and differences in their implementations need only be very marginal. Another recent proposal for the use of the digit-set $\{0, 1, 2, 3\}$*, with a special 3-bit encoding of digits, is analyzed and some optimizations are shown, including the possibility of using a 2-bit encoding, simplifying the wiring of a multiplier tree. All these proposed designs are shown to be equivalent to a standard 4-to-2, carry-save adder, except possibly for a few signal inversions.*

1. Introduction

When implementing fast multipliers in VLSI, a major part of area and time is spent on accumulating partial products using some kind of tree structures. Originally these were based on the use of full-adders (and occasionally at the ends some half-adders), reducing the sum of three rows to the sum of two rows, using either the Wallace- [17] or Dadda- organizations [2] of the tree structure. As these structures are not very regular to lay out due to the 3-to-2 structure, it was suggested to use 4-to-2 adders which allow the use of binary tree structures. [18] seems to be the first to propose their use, based on the carry-save representation, where two addends are considered an encoding of a single operand represented using the redundant digit-set $\{0, 1, 2\}$. Thus the 4-to-2 adder can be considered an adder taking two such operands and adding them to produce the result in the same representation. This addition can be performed in digit parallel, and thus in constant time, using an array of such digit adders. Radix 2 signed-digits for 4-to-2 adders over the digit-set $\{-1, 0, 1\}$ were then later proposed in [15, 5]. Recently [3] proposed using the digit-set $\{0, 1, 2, 3\}$ with a special 3-bit encoding of the digits, and most recently [10] compared various 3- and 4-element digit sets using some particular encodings, claiming significant differences in the implementation of these. Other publications discussing multiplier organizations are [16, 11, 6, 7, 8, 9, 12, 19], and plenty more.

After an introduction in Section 2 on the standard carry-save 4-to-2 adder, and some results on the use of signals with negative weights, Section 3 goes through a detailed review of a series of 4-to-2 adders recently presented in [10]. These are all based on digit codings of the form $d = \pm 2d^h \pm d^l$ for redundant digit-sets with 3 or 4 elements, and using a special technique denoted *equal-weight grouping*, or EWG. Here columns of bits of the same weight are accumulated, but producing a

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sum represented in the various digit-sets. Results from SPICE simulations on the designs were presented, whereupon the authors then postulate some claims on the relative performances when using the investigated digit-sets.

The following Section 4 then shows that all these designs can be implemented using the very same basic 4-to-2 carry-save adder, just using alternative external connections and possibly a few inverters. Hence there are no principal differences between the use of the various digit sets, as opposed to the claims of the paper, nor to the use of the digit encodings proposed or the 4-element digit-sets.

Section 5 reviews some other recent results from [3], where the use of the digit-set $\{0, 1, 2, 3\}$ and a special 3-bit encoding of that digit-set is employed. The authors claim to achieve fairly significant speed-ups by this encoding. By a detailed analysis and identification of some basic building blocks, it is shown that it is not necessary to use the particular 3-bit encoding to obtain the same effect, there is an equivalent 2-bit encoding. It is found that a saving in the wiring can be obtained by reorganizing the building blocks. Finally it is then shown that this design is also equivalent to one based on the standard 4-to-2 carry-save adder. In Section 6 conclusions are drawn.

2. A basic building block.

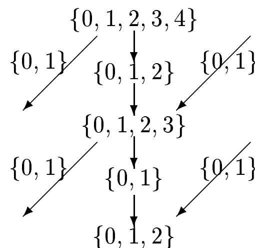
We will start by looking at the basic functionality of a 4-to-2 adder, whose purpose in a multiplier (and other multi-operand addition problems) is reducing the sum of four binary operands to the sum of two. The operands can be partial products as generated and delivered in parallel at the leaves of the tree, or at the internal nodes of the tree they can be the result delivered as pairs of operands, forming the result of other 4-to-2 adders. In general we shall assume that such operands and results can have a specific positive or negative weight (is to be added or subtracted).

A pair of two bits of positive weight can be interpreted as a digit in the set $\{0, 1, 2\}$, the *carry-save digit-set*, employing the *carry-save encoding*:

$$\begin{array}{lll} 0 & \sim & 00 \\ 1 & \sim & 01 \quad \text{or} \quad 10 \\ 2 & \sim & 11 \end{array} \tag{1}$$

where it may be noted that the digit value 1 has two encodings.

Usually the 4-to-2 adder is considered an adder taking two such carry-save operands, and delivering the sum of these in the same carry-save representation. But alternatively interpreted at the digit level, it may also be considered a digit-set converter from the set $\{0, 1, 2\}+\{0, 1, 2\} = \{0, 1, 2, 3, 4\}$ into the set $\{0, 1, 2\}$, where such a conversion can be pictured in a diagram [4]:



The converter or 4-to-2 adder can be realized by a combination of two full adders as in Figure 1, where the tuple (i_1, i_2), respectively (i_3, i_4), is the carry-save encoding of the operands, and (o_1, o_2) represents the result. Note that carries (c'_{in}, c''_{in}) similarly is a carry-save encoding of the incoming "double" carry, and (c'_{out}, c''_{out}) of the outgoing carry, corresponding to the previous conversion diagram.

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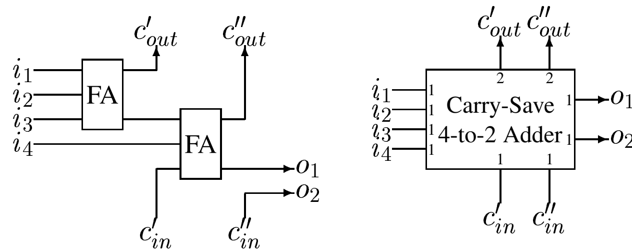

Figure 1. 4-to-2 carry-save adder composed of two full adders, and "box" version.

A particularly efficient realization of a 4-to-2 adder was shown in [7], as illustrated in Figure 2, where the XOR-gates were implemented by MUXes using pass-transistors.

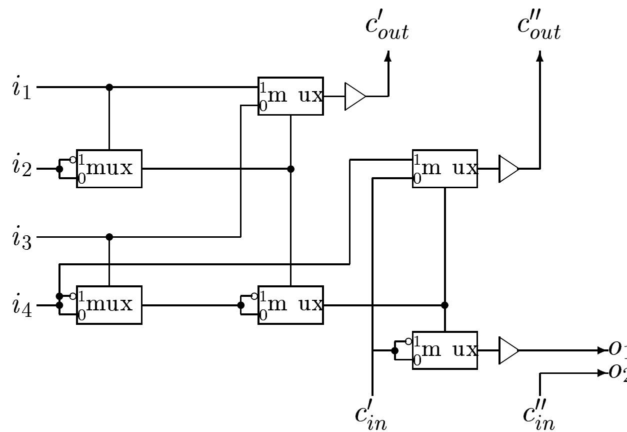

Figure 2. 4-to-2 carry-save adder built of multiplexers.

Note that the addition of the carry c''_{in} is obtained at no cost in Figures 1 and 2, corresponding to the second conversion in the conversion diagram above being without cost in logic.

The transistor implementation of the XOR-gates in [7] uses a "dual-rail" representation of signals, these being provided and used in true as well as in inverted form. This implies that inversion of a signal can be realized by twisting wires, and thus at no cost in logic.

For the following discussion we will use the simplified "box"-version of Figure 1, not being concerned with the actual implementation of the logic. Signals are marked with their relative weight.

In Figures 1 and 2, and according to the carry-save representation, the signals $i_1, i_2, i_3, i_4, c'_{in}, c''_{in}$, o_1 and o_2 all have the weight 1, while c'_{out} and c''_{out} have weight 2, corresponding to the equation

$$2(c'_{out} + c''_{out}) + (o_1 + o_2) = i_1 + i_2 + i_3 + i_4 + c'_{in} + c''_{in}. \tag{2}$$

We will in the following assume that $o_2 = c''_{in}$, since this allows c''_{in} to be added in at no cost. Thus we have the following defining equations

$$\begin{aligned} o_1 &= (i_1 + i_2 + i_3 + i_4 + c'_{in}) \bmod 2 \\ o_2 &= c''_{in} \\ c'_{out} + c''_{out} &= (i_1 + i_2 + i_3 + i_4 + c'_{in}) \operatorname{div} 2, \end{aligned} \tag{3}$$

where the pair c'_{out}, c''_{out} provides a carry-save encoding of the combined carry in $\{0, 1, 2\}$.

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To allow changes in the weights for other digit sets, following [1] we note this theorem:

Theorem 1 *Let a binary signal $b \in \{0, 1\}$ have associated weight w, so that the value of the signal is $v = w\,b$. Inverting the signal into $1 - b$, while at the same time negating the sign of the weight, changes its value into $v' = v - w$, i.e., the value is being biased by the amount $-w$.*

Proof: Trivial since $v' = (-w)(1 - b) = wb - w = v - w$. □

When changing the interpretation of input signals as representation of values, it is then necessary to perform equivalent changes in the interpretation of the output signals. E.g., when the the domain of input to an adder or a digit-set conversion is being biased, the output must be equivalently biased.

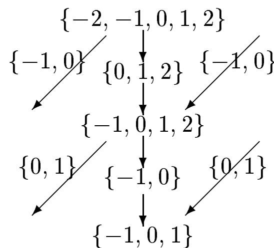
Now consider the base 2 digit-set $\{-1, 0, 1\}$ using the *signed-digit* encoding (also denoted *borrow-save*), where two bit strings are considered a string of digits:

$$\begin{array}{cccccccl} \times & \otimes & \times & \cdot & \cdot & \cdot & \times\;\times & \text{Neg. weight} \\ \times & \otimes & \times & \cdot & \cdot & \cdot & \times\;\times & \text{Pos. weight} \end{array}$$

obtained by pairing bits using the digit encoding:

$$\begin{array}{rcll} -1 & \sim & 10 & \\ 0 & \sim & 00 & \text{or} \quad 11 \\ 1 & \sim & 01, & \end{array} \tag{4}$$

where the left-most bit has negative weight. The conversion diagram for the addition of two signed-digit operands then may look as:



If in Figure 1 we change the input so that (i_1, i_2) and (i_3, i_4) represent signed-digits, with i_1 and i_3 respectively having negative weight and the signals thus delivered inverted, then the input is being biased by -2. The output must then according to equation (2) be equivalently biased, which is possible by changing the sign of c'_{out} by inverting its signal value. But then c'_{in} must also change sign, which changes the bias in the input to -3. Finally, to compensate we must change the sign of the weight of o_1, corresponding to the output (o_1, o_2) now representing a signed-digit, hence the signals must now satisfy the following equations:

$$\begin{array}{rcl} 2((1 - c'_{out}) + c''_{out}) + ((1 - o_1) + o_2) & = & (1 - i_1) + i_2 + (1 - i_3) + i_4 + (1 - c'_{in}) + c''_{in} \\ \text{or} \qquad 2(-c'_{out} + c''_{out}) + (-o_1 + o_2) & = & -i_1 + i_2 - i_3 + i_4 - c'_{in} + c''_{in} \end{array}$$

and the equivalent equations derived from (3). Inverting the signals appropriately in Figure 1 we obtain Figure 3.

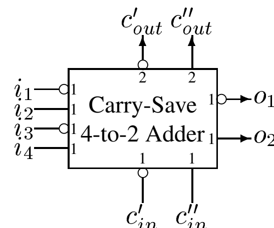


Figure 3. 4-to-2 signed-digit adder obtained from a carry-save adder

Theorem 2 *In a computational model where inversion is without cost in area and time, radix 2 signed-digit addition can be realized at exactly the same cost as carry-save addition.*

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Observe that if an array of such adders are connected (here vertically) to form an n-digit adder, then no inversions are needed between the individual adders. Similarly if a tree of such arrays are formed to perform multi-operand addition (here horizontal connections), then all the inversions internally in the tree can be eliminated.

Theorem 3 *Multi-operand addition of radix 2 signed-digit operands can be implemented by a tree of carry-save adders, by inverting all negatively weighted signals on input as well as on output, but with no changes internally to the tree.*

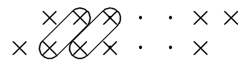
3. Codings of the form $\pm 2d^h \pm d^l$.

Recently in [10] various radix 2 redundant digit-sets, using encodings of the form (d^h, d^l) with $d = \pm 2d^h \pm d^l$, were suggested and analyzed, employing a particular way of implementation denoted *equal-weight grouping* or EWG, to be described below. The digit-sets investigated were

$$\begin{array}{rclrcl} \mathcal{D}^{(SD)} & = & \{-1,0,1\} & \mathcal{D}^{(CS2)} & = & \{0,1,2\} \\ \mathcal{D}^{(SD3^{(-)})} & = & \{-2,-1,0,1\} & \mathcal{D}^{(CS3)} & = & \{0,1,2,3\} \\ \mathcal{D}^{(SD3^{(+)})} & = & \{-1,0,1,2\}. & & & \end{array} \quad (5)$$

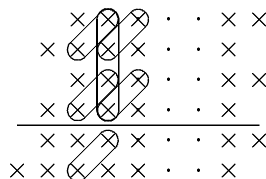
The digit-sets $\mathcal{D}^{(SD)}$ and $\mathcal{D}^{(SD3^{(-)})}$ are coded as $d = -2d^h + d^l$, corresponding to a 2's complement encoding of the digit d. Since the digit-set $\mathcal{D}^{(SD)}$ does not include -2, the bit-pattern $(d^h, d^l) = (1, 0)$ is not valid in the SD representation. The set $\mathcal{D}^{(SD3^{(+)})}$ is realized by changing the sign of both components, i.e., $d = 2d^h - d^l$. The $\mathcal{D}^{(CS3)}$ and $\mathcal{D}^{(CS2)}$ digit-sets are coded with $d = 2d^h + d^l$, where the bit-pattern $(d^h, d^l) = (1, 1)$ is invalid in the $\mathcal{D}^{(CS2)}$ representations.

Since the encodings employ weights differing by a factor of 2, neighboring digits d_i and d_{i-1} in a radix representation overlap one another, i.e., d_i^l has the same weight as d_{i-1}^h,

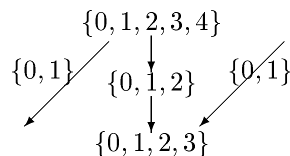


but accumulation of several bit-vectors from the encoding of digit vectors can still be performed in vertical columns. This is what the authors of [10] denote *equal-weight grouping* or EWG-form.

Normally redundant adders are used to reduce the sum of two digit-vectors to a single redundant digit-vector, absorbing and emitting suitable carries. With additions of the form $\mathcal{D}+\mathcal{D} \to \mathcal{D}$, where $\mathcal{D}$ is one of the above listed CS digit-sets, e.g., with $\mathcal{D} = \mathcal{D}^{(CS3)}$, then $\mathcal{D}+\mathcal{D} = \{0,1,2,3,4,5,6\}$. With EWG, bits from the encoding of two neighboring positions are added, the summation takes bits in a column forming a sum in $\{0,1,2,3,4\}$, but producing the resulting digit in $\mathcal{D}^{(CS3)} = \{0,1,2,3\}$ as shown in the following diagram (without the carries):



The coding used for $\mathcal{D}^{(CS2)}$ and $\mathcal{D}^{(CS3)}$ is $d = 2d^h + d^l$. Since the bit-vectors all have positive weight, it is a digit-set conversion of the form:



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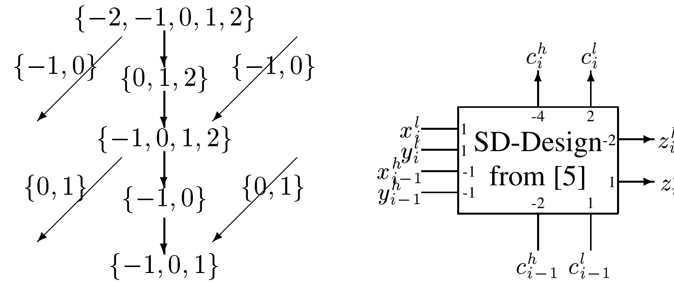
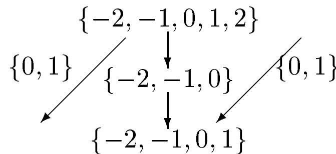
for the case of addition in $\mathcal{D}^{(CS3)}$, where using EWG the conversion is from $\{0,1,2,3,4\}$ back into $\mathcal{D}^{(CS3)} = \{0,1,2,3\}$. When the coding is $d = -2d^h + d^l$, two of the bit-vectors have negative weight, and by EWG the mapping is from $\{-2,-1,0,1,2\}$ to $\{-1,0,1\}$.

For comparison the authors then consider four cases:

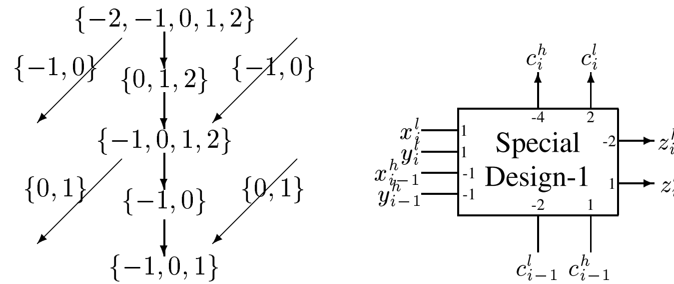
1. $\underline{SD + SD \to SD}$:[1] Here they employ the signed-digit, 4-to-2 adder from [5] using the encoding $-1 \sim 11$, $0 \sim 00$ and $1 \sim 01$, corresponding to 2's complement encoding (but it could also be interpreted as a sign-magnitude). The carry-set $\mathcal{C}^{(SD)} = \{-1,0,1\}$ is assumed to be in the same encoding.



2. $\underline{SD3^{(-)} + SD3^{(-)} \to SD3^{(-)}}$: The carry-set used is $\mathcal{C}^{(SD^{(-)})} = \{-1,0,1\}$, despite the fact that $\{0,1\}$ is sufficient, as can be seen from this conversion diagram:

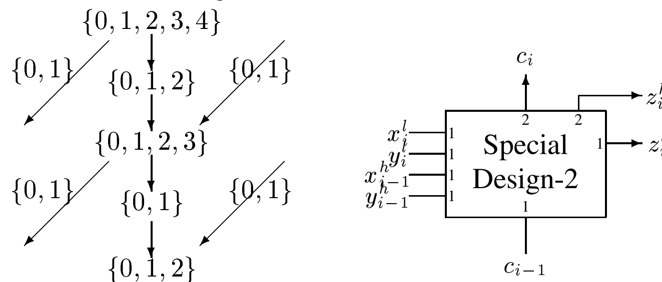


The signals in their mux-based design are assumed to have the weights shown in the diagram:



It is noted that the addition $SD3^{(+)} + SD3^{(+)} \to SD3^{(+)} = \{-1,0,1,2\}$ can be realized by interchanging the positive and negative inputs.

3. $\underline{CS2 + CS2 \to CS2}$: The carry-set here is proven to be $\mathcal{C}^{(CS2)} = \{0,1\}$, as the two outgoing carries in the diagram is shown never simultaneously to be 1. Another mux-based design is used in [10], with assumed weights as indicated:



[1] This is the notation used in [10], note that due to EWG this is **not** set addition.

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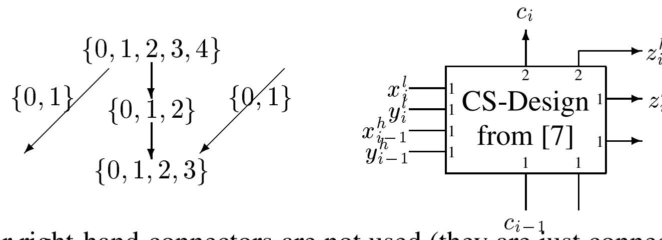
4. $\underline{CS3 + CS3 \to CS3}$: The carry-set is again $\mathcal{C}^{(CS3)} = \{0, 1\}$, hence a simplified conversion is sufficient. To implement the adder they employ the 4-to-2 compressor (carry-save based) from [7], as described in Figure 2. Again they do not describe the connections and weights, but we assume they are as described here:



where the lower right-hand connectors are not used (they are just connected by a "jumper".)

Note that for all four designs above, input is provided in the EWG-form by combining signals (bits of the same absolute value weight) from two neighboring digit positions, but output is delivered in the proper encoding for the particular digit-set. The authors of [10] performed SPICE simulations of the four designs above, yielding the following table (their Table 8):

Adder Cell	Critical Path Delay (ns)
SD	0.78750
$SD3^{(-)}$	0.96025
$CS2$	0.66100
$CS3$	0.46580

On page 1276 of [10] it is stated:

> *"multipliers based on $CS3$ can be expected to outperform multipliers based on other redundant representations"*

and furthermore using arguments on digit-set cardinalities:

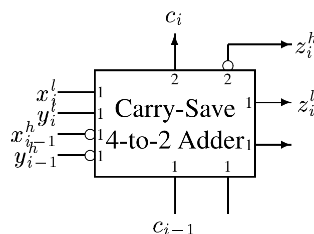
> *"Therefore, cells such as 1 and 3 from [the listing above] are fundamentally more complex, hence, bigger and slower."*

4. Alternative implementations.

Using the results of Section 2, *and contrary to the above statements*, we shall now show that all the four adder cases can be implemented by the same hardware, e.g., the efficient design from [7] as used in Figure 2 and case $CS3$ above, just using an alternative signal interpretation. It will then be apparent that there are no advantages in using the particular codings of the form $\pm 2d^h \pm d^l$, as opposed to the form $d' \pm d''$, traditionally used for carry-save and signed-digit encodings.

We will do this by showing that in the above four cases there exist alternative implementations, using any generic 4-to-2 carry-save adder. In particular we may employ the mux-based design from [7], where it is possible at no cost in transistor count to add properly placed signal inversions.

1. $\underline{SD + SD \to SD}$



where the lower right-hand connectors are not used (they are just connected by a "jumper".)

2. $\underline{SD3^{(-)} + SD3^{(-)} \to SD3^{(-)}}$: Obviously the diagram above can also be used here , since it delivers a result in $\{-1, 0, 1\} \subset SD3^{(-)} = \{-2, -1, 0, 1\}$.

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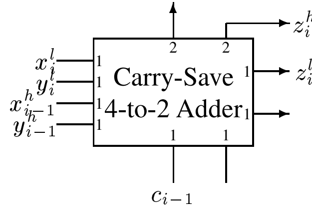
3. $\underline{CS2 + CS2 \rightarrow CS2}$: The standard carry-save adder can directly be used, just using different output connections to deliver the result in the $2d^h + d^l$ encoding.



4. $\underline{CS3 + CS3 \rightarrow CS3}$: The same 4-to-2, carry-save adder as in the previous case can be used since $\{0, 1, 2\} \subset \mathcal{D}^{(SD3)} = \{0, 1, 2, 3\}$. Note that this was the solution used in [10].

Observe again, that in any array-structure of such adders (e.g., in a multiplier tree), there is no need for inversions internally in the array. We can thus conclude that it is possible to implement addition in these five digit-sets (including $SD3^{(+)}$) with the very same logic, except possibly for a few inversions, which may even be trivially realized at no cost in logic.

5. Another example using the digit-Set $\{0, 1, 2, 3\}$.

In [3] another implementation was proposed employing the digit-set $\{0, 1, 2, 3\}$, albeit with a 3-bit encoding of digits, where the value of the code can be obtained by adding the values of the three bits (d, e, f) for all the valid combinations, $v = d + e + f$, where $(e, f) \neq (1, 0)$. Internally a unique 2-bit coding (t, w) was also used:

Value	0	1	–	2	1	2	–	3
d, e, f	000	001	010	011	100	101	110	111
t, w	00	01	–	10	01	10	–	11

Observe that (t, w) is the same encoding as used in [10] for the digit-sets $\mathcal{D}^{(CS2)} = \{0, 1, 2\}$ and $\mathcal{D}^{(CS3)} = \{0, 1, 2, 3\}$, with digit value $v = 2d^h + d^l$. Mapping from (d, e, f) into (t, w) is performed by the logic in Figure 4 (slightly reorganized from [3]), shown together with a simplified block symbol.

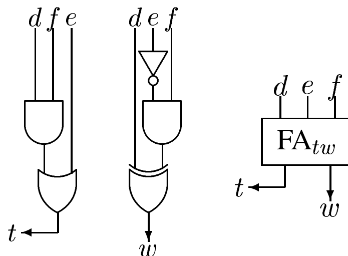


Figure 4. Mapping from (d, e, f) into (t, w).

This logic is functionally equivalent to a full-adder, except for the restrictions on the input (d, e, f) (which we will denote the *def*-encoding), and coding of the output in the (t, w)-form (denoted the tw-encoding). [3] then describes various adders for combinations of operands in the redundant *def*-encoding and ordinary binary, with output in *def*-encoding. We shall only go into details with two of these. The first we describe in Figure 5 is an adder taking four ordinary binary operands, and delivering their sum in the *def*-encoding, here shown slightly modified from [3].

Observe that the left-most part of Figure 5, computing (t_{out}, d), is a standard full-adder, and the right-most part is a recoding where arithmetically $e + f = i + t$, but assures that only legal

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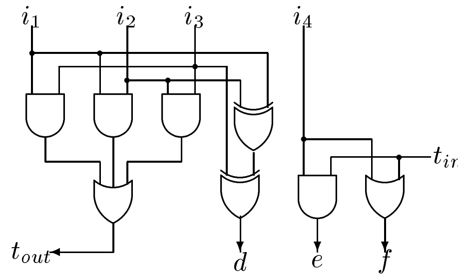

Figure 5. Adder taking four binary signals into (d, e, f) encoding.

combinations of d, e, f are produced ($(e, f) \neq (1, 0)$). This is the logic needed at the first level of a multiplier tree, the critical path here is through two XOR gates, and the authors claim a speedup of about 1.7 compared to an ordinary 4-to-2 adder.

For the case of two redundant operands the critical path is two XORs, plus an AND and an OR gate, where the authors have found a speedup of about 1.2. The following conversion diagram shows how the addition is performed:

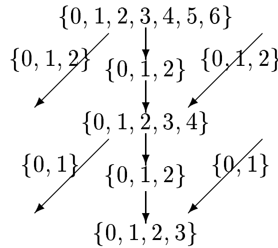

Figure 6, reproduced with slight modifications from [3], shows their implementation, using a carry in $\{0, 1, 2\}$ in carry-save representation (t^1, t^2), plus a carry u in $\{0, 1\}$.

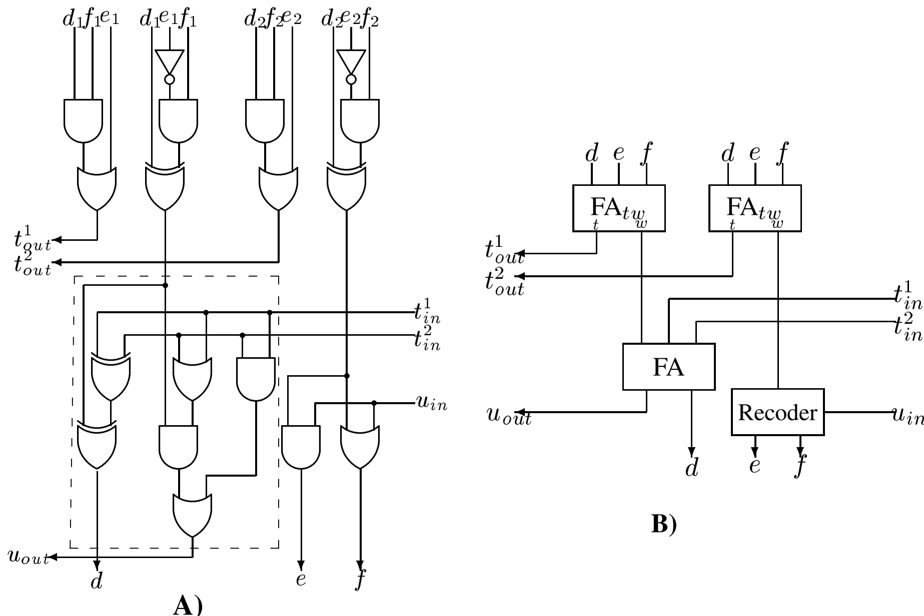

Figure 6. A: Adder with two redundant operands, B: Block diagram.

Observe that the dot-framed part is again a standard full-adder, and the logic producing e and f is again the recoding assuring $(e, f) \neq (1, 0)$. Figure 6-A can also be described in a simplified way by the block diagram of Figure 6-B.

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Now note that instead of using the *def*-coding at input and output, we may as well remove the two FA_{tw} adders at the top, and add one at the bottom, thus using the tw-coding on input and output, as illustrated in Figure 7.

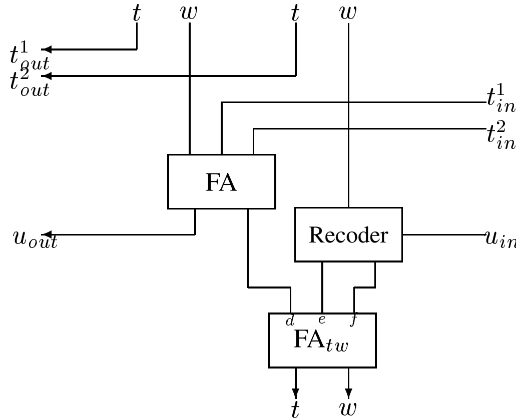

Figure 7. Reorganized 4-to-2 tw-adder.

We have thus shown that it is not necessary to use the *def*-encoding at the external interface to the adder, and that the 4-to-2 adder in tw-encoding can be implemented with only about two thirds of the logic needed for the adder using def-encoding, as presented in [3]. The critical paths here are of the same length as in Figure 6.

We finally need the adder-type to use at the first level of an adder tree, i.e., taking four binary signals and producing their sum in tw-encoding, and a recoding to use at the root of the adder tree. Both of these are trivially found as shown in Figure 8.

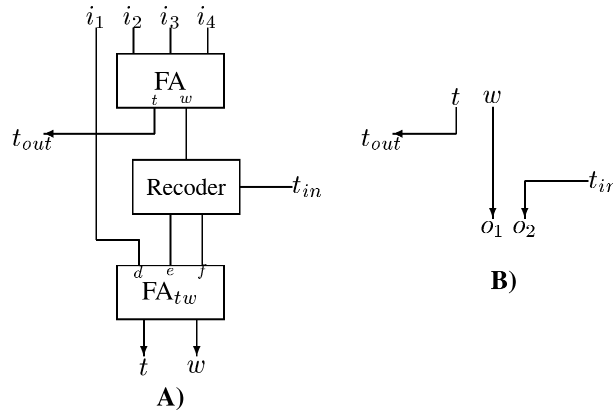

Figure 8. A: First level adder for tw-encoded result. B: Root conversion.

However, the simplifications of the nodes do not help in an adder tree, since there still is a *def*- to tw-conversion between each level in the tree, and at the first level an extra similar conversion is needed now as seen in Figure 8-A. Note though that at the root of the tree, instead of a FA_{tw} adder to convert from def- to tw-encoding, now only the simple re-wiring in Figure 8-B is needed to deliver the ordinary carry-save encoding of the result. Thus the critical path of the tree is unchanged.

But more important, the wiring of the tree is now simplified, since only two signals instead of three are needed in each connection between the layers of the adder tree.

Now observe that in all places where signals e, f are fed into an FA_{tw}-adder, there is a recoding taking place, to assure that the pattern $(e, f) \neq (1, 0)$. If the logic of that recoding is combined with the logic of the FA_{tw}-adder, it appears that the result is an ordinary full-adder. Just consider

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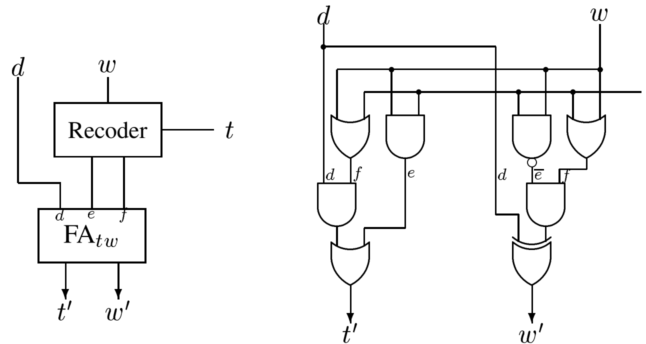
Figure 8-A with input (d, w, t) to the combination of a recoder and FA$_{tw}$-adder, with output denoted (t', w'), then from the combined logic



we find $t' = dw + dt + wt$ and $w' = d \oplus w \oplus t$, which is the functionality of a standard full-adder. We have thus shown that the proposed adder is again equivalent to the standard carry-save, 4-to-2 adder based on the digit-set $\{0, 1, 2\}$, and the speed difference observed is due to different implementations of the full-adders used.

6. Conclusions

Using some trivial results on signal weights it has been shown that there are no fundamental differences between the redundant, radix 2, 4-to-2 adders based on carry-save, and those based on signed-digit representations, i.e., digit sets $\{0, 1, 2\}$ and $\{-1, 0, 1\}$ with their usual encodings. There need only be very small differences between implementations, as only a few inverters are needed to change one type of adder into the other. For multi-operand addition, as in multiplication using an array- or tree-structure of adders, it has been shown that inversions are only needed on appropriate input and output signals, no changes are necessary internal to the array- or tree-structure. In a computational model where inversion is without cost in area and time, signed-digit arithmetic can be performed at exactly the same cost as carry-save.

After a review of some redundant adder designs from [10] for a variety of digit-sets (3-and 4-element), for which claims were made about principal differences and relative speeds, it was shown that they can in fact all be implemented by the same basic 4-to-2 carry-save adder, just using some other interface wiring to the environment and possibly a few inverters. Hence there is no principal difference between the use of, say, the digit-sets $\{0, 1, 2, 3\}$ and $\{0, 1, 2\}$, the difference is just a question of interpretation of which signal-pairs constitute encodings of digits.

Finally another proposal in [3] to use a radix-2, 4-element digit-set with a 3-bit digit encoding, has been reviewed. It is shown that this design is only marginally different from the adder in [10] also employing the digit-set $\{0, 1, 2, 3\}$, and thus can also be interpreted as a normal 4-to-2, carry-save adder. It was furthermore shown that the 3-bit encoding is not necessary, a standard 2-bit encoding can be used. Actually, it is found that the difference is only in the positioning of the boundaries between the levels in a multiplier tree.

All the proposed 4-to-2 adder designs, employing digit or carry encodings of the form $v = d' \pm d''$ or $v = \pm 2d' \pm d''$ (including also the sign-magnitude encoding), have thus been shown to be equivalent to a carry-save adder over the standard carry-save digit-set $\{0, 1, 2\}$, except possibly for a few signal inversions. It is conjectured that there are no other fundamentally different digit encodings that will allow for faster implementations. Any single, or two or more alternating, optimal adder designs employing encodings of the form $v = d' \pm d''$ can be used internally in an array (or tree) for multi-operand addition; only at the external interfaces to the array it may be necessary to add inverters, adapting to the digit set and encoding used in the environment.

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