Computer Arithmetic

Prof. Vojin G. Oklobdzija

Assignment No. 2.
Due: May 4, 2004

Homework Assignment No. 2:

1. Read Knowles paper. Examine all possible 16-bit minimal-depth expansions where you are allowed to change the radix (radix-2 was used in Knowles paper). You are allowed to use radix-3 and radix-4 (radix-5 and greater are considered not feasible for CMOS). You should start with the higher radix stage at the inputs followed with radix-2 stage. Higher radix stage should always be followed by radix-2 stage. (we are contemplating use of compound domino logic – yielding the most efficient implementation). The last stage should not contain higher radix. It should be either radix-2 or inverter. How many schemes can you create ?
   (a) Suggest several such 32-bit expansions that you may consider to be good.
   (b) How many levels (minimal) would be in a 64-bit adder ?

2. (problem contributed by Paolo) Read Carry-Select paper by Bedrij. Assume that 4-bit addition will be done in two logic stage delay (MCC used). Assume that two logic stage have fan-in of two and fan-out of two. Assume that fan-in of four increases delay by one logic stage. Quadrupling the fan-out would result in one additional logic stage delay.
   (a) You are do design a 64-bit adder using Bedrij's scheme. You will start with a four-bit lsb group, but you are allowed to vary the size of the group so that the delay is balanced. (you want to finish your conditional addition by the time select signal arrives, thus you are allowed to have larger msb stages). Find an optimal group sizes achieveing minimal delay.
   (b) What is the minimal delay of such adder expressed in logic levels ?