Midterm Exam: May 28, 2004

1.16 (a) Show that the overflow in addition in the two's complement system can be detected by the exclusive-or of the carry-in and the carry-out of the most significant bit.

(b) Show that the last expression does not work properly in the ones' complement system.

2.18 Ling's adder (Doran 1988; Ling 1981) uses a more efficient recurrence for carries compared with the recurrence used in the carry-lookahead adders discussed in

Section 2.1. The expressions used there are

$$p_i = x_i \oplus y_i, \quad g_i = x_i y_i, \quad c_{i+1} = g_i + p_i c_i, \quad s_i = c_i \oplus p_i$$

Ling defines a new "carry" function $h_i = c_{i+1} + c_i$, resulting in the following adder expressions:

$$t_i = x_i + y_i, \quad g_i = x_i y_i, \quad h_i = g_i + t_{i-1} h_{i-1}, \quad s_i = t_i \oplus h_i + g_i t_{i-1} h_{i-1}$$

(a) Show that Ling's expressions produce the correct sum.

(b) Consider the expressions for a group of four bits and show that Ling's approach is more efficient than the conventional one with respect to the number of gates and fanin.

2.21 Using a prefix adder as a basis, design a network that produces simultaneously $s = x + y$ and $z = x + y + 1$. This network is useful in rounding for floating-point addition.

3.24 Design a network consisting of full-adders and half-adders to compute

$$z = a - 3b + 5c$$

where a, b, c are integers in the range $[-4, 3]$, represented in the two's complement system.

(a) What is the least number of bits necessary to represent z?

(b) Show the bit-matrix before and after simplification.

(c) Show your final network. Minimize the delay and the number of FA/HA modules in the reduction to two operands.

(d) What is the minimum precision of the carry-propagate adder needed to produce the final result? Which type of CPA would be best suited?

.18 Consider the implementation of 12×12 multiplication with operands and product in two's complement representation. Use 5×5 multiplication modules (two's complement representation).

(a) Determine how many modules are required.

(b) Show the bit-matrix to be added, identifying the output bits of each multiplication module.

(c) Determine the network of full-adders and half-adders required to reduce the bit-matrix to two rows, using the column reduction approach.