Written Homework Assignment #1

1. Identify the control (or branch) hazard and modify the code to eliminate the branch hazard assuming the branch decision is made in ID stage.

```
...
beq   $12, $0, L1
add   $5, $0, 1
beq   $12, $5, L2
add   $15, $14, $2

L1:    add $12, $12, -1
       add $5, $6, $5
L2:    or $3, $4, $12
...
```

2. Calculate how many clock cycles are needed to execute the instructions below with and without pipeline? You can assume the following:

1) Instruction Fetch take 2 ns
2) Instruction Decode 1ns
3) ALU 2ns
4) Memory Access 2ns
5) Write Register 1ns

```
add $1, $6, $11
lw   $2,  8($12)
lw   $3,  8($13)
and $4,  $9, $14
or   $5, $10, $15
```

3. How can the structural hazard on register file be eliminated? What advantage can we take from the clock?