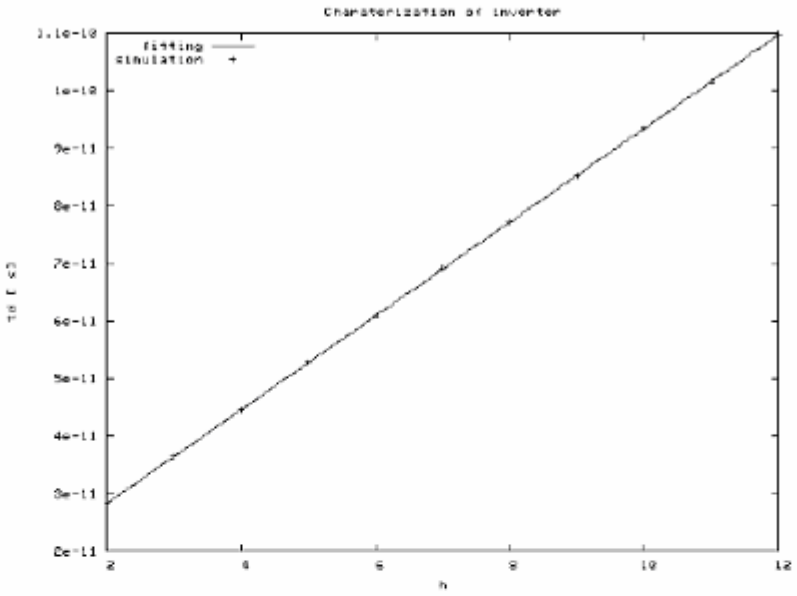
Homework 3 Solutions

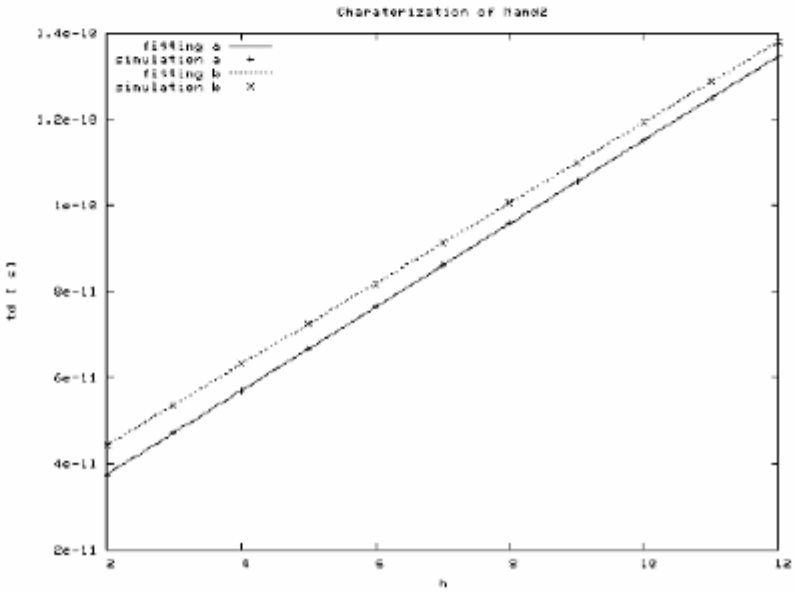
Problem 1:

The characterization of required gates is summarized below.

```
**** Inverter (a)! ****
input   g[norm]   p[norm]   g[ps]     p[ps]
a       1.0000    1.4781     8.1413   12.0340
```

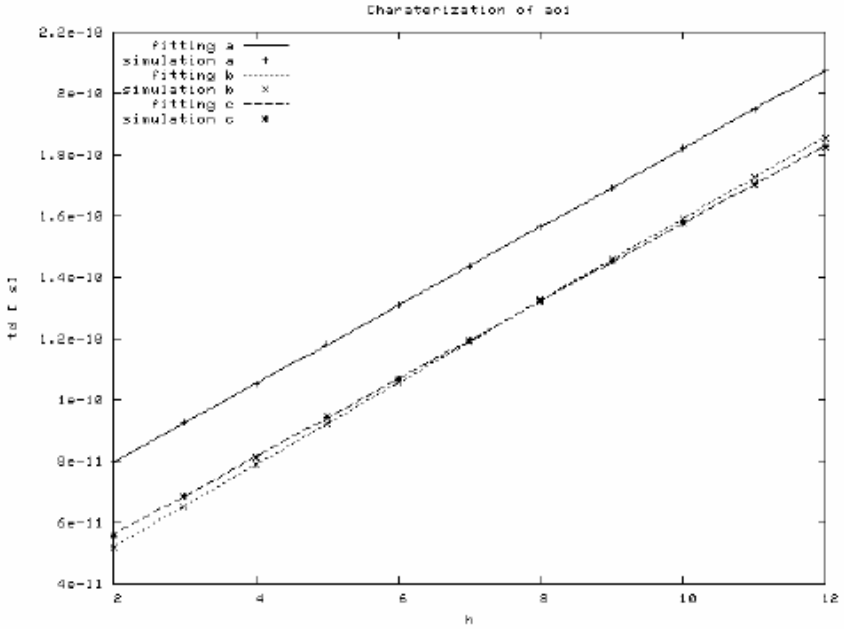



```
**** Nand2   (a*b)! ****
input   g[norm]   p[norm]   g[ps]     p[ps]
a       1.1929    2.2218     9.7117   18.0880
b       1.1514    3.1414     9.3740   25.5750
```



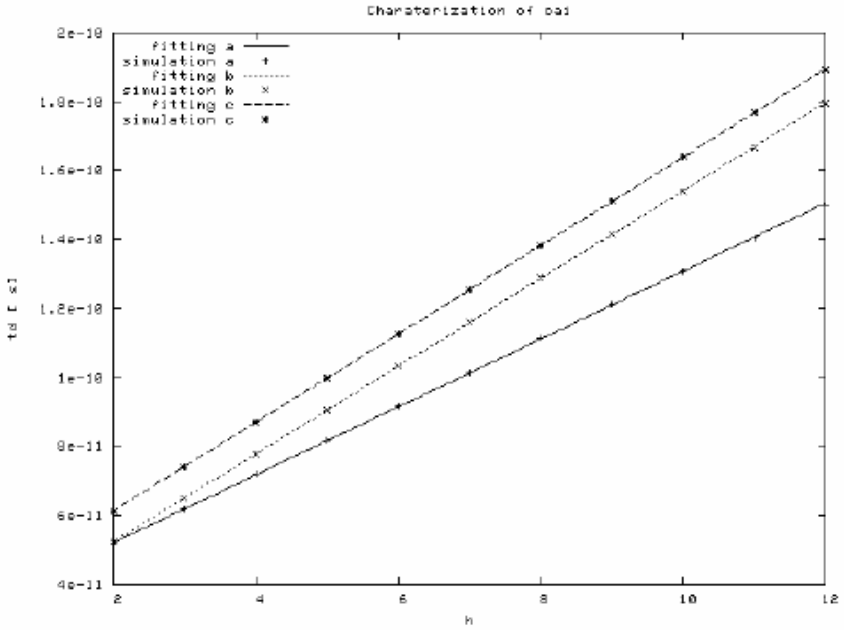
**** AOI [a+(b*c)]! ****

input	g[norm]	p[norm]	g[ps]	p[ps]
a	1.5701	6.6493	12.7830	54.1340
b	1.6424	3.1206	13.3710	25.4060
c	1.5593	3.7645	12.6950	30.6480



**** OAI [a*(b+c)]! ****

input	g[norm]	p[norm]	g[ps]	p[ps]
a	1.2089	3.9877	9.8419	32.4650
b	1.5611	3.3255	12.7090	27.0740
c	1.5732	4.4000	12.8080	35.8220



Problem 2:

Using the gate characterization of problem 1, the optimal stage effort, f_o can be computed.

$$f_o = (GBH)^{1/6} = [(g^3_{OAI}\, g^2_{AOI}\, g_{NAND2})(2^5)(64/1)]^{1/6} = 5.44$$

The corresponding gate sizes are (from the output to the input):

$C_{OAI\_6} = b\, C_{out}\, g / f_o = (2)(64C_{in})(1.57) / 5.44 = 36.9C_{in}$

$C_{AOI\_5} = (2)(36.9C_{in})(1.66) / 5.44 = 22.5C_{in}$

$C_{OAI\_4} = (2)(22.5C_{in})(1.57) / 5.44 = 13.0C_{in}$

$C_{AOI\_3} = (2)(13.0C_{in})(1.66) / 5.44 = 7.93C_{in}$

$C_{OAI\_2} = (2)(7.93C_{in})(1.57) / 5.44 = 4.57C_{in}$

$C_{NAND2\_1} = (4.57C_{in})(1.19) / 5.44 = 1.0C_{in}$

The total delay of the path:

$$D = (6\, f_o + 3p_{OAI} + 2p_{AOI} + p_{NAND2})\, \tau =$$

$$= [6\ (5.44) + 3\ (4.40) + 2\ (3.67) + 2.22]\ (8.14ps) = 451ps$$

Problem 3:

(a) With LE sizing, it is observed that all nodes at the same stage level have equal loading. Therefore, the branching factor at each node can be easily computed as:

$$b = (g_{AOI/OAI} + g_{INV}) / g_{AOI/OAI}$$

The detail spreadsheet is attached below. The computation of *G*, *B*, *H* and gate sizes are straight-forward. The computation of *f_opt* will lead to circular recurrence. To avoid that, *f_est* is used for sizing. The solution is reached when *f_est* = *f_opt*. It is indicated by *Error* cell.

	NAND2	AOI	OAI	INV	tau
g	1.19	1.66	1.57	1	8.14
p	2.22	3.67	4.4	1.48	

f_est	5.13	Error	0.000
Cin	1.00		

Stage	Off-path	On-path	Branch
		NAND2	
1		1.00	1.00
	INV	*OAI*	
2	1.68	2.63	1.64
	INV	*AOI*	
3	3.24	5.37	1.60
	INV	*OAI*	
4	6.46	10.15	1.64
	INV	*AOI*	
5	12.47	20.70	1.60
Load	64	64	

G_calc	8.08
B_calc	6.88
H_calc	64
fopt_calc	5.13

	(tau)	(ps)
Total Delay	44.02	358.37

(b) Using the netlist (included in the end), SPICE simulation data is obtained. Note that Cin is set to 1μm.

```
$DATA1 SOURCE='HSPICE' VERSION='U-2003.03-SP1    '
.TITLE '* takehome exam5'
  tdf          tdr           tda             q           e
  3.505e-10    3.535e-10     3.520e-10      -8.204e-13   8.204e-13
```

The worst-case delay goes through the bottom AOI of stage 5. The resulting delay is 353.5ps. It agrees very well to the estimation (358.4ps).