A 3.8ns CMOS 16×16 Multiplier Using Complementary Pass Transistor Logic

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ABSTRACT

A 3.8ns 257mW CMOS 16x16 multiplier with a supply voltage of 4V is described. A complementary pass transistor logic(CPL) is proposed and applied to almost the entire critical path. The CPL consists of complementary input/output, nMOS-pass-transistor logic network and CMOS output inverters. The CPL is twice as fast as the conventional CMOS due to lower input capacitance and higher logic construction ability. Its multiplication time is the fastest ever reported, including times of bipolar and GaAs ICs, and it is also shown to be further enhanced to 2.6ns 60mW at 77K.

1. INTRODUCTION

The speed of CMOS devices, which were used mainly in low-power high-densisty chips, has increased drastically with the rapid progress in miniaturization. CMOS speed is getting close to that of Si bipolar technology; for example, with submicron CMOS technology, a 15ns 1Mb SRAM[1] and a 7.4ns 16×16b multiplier[2] were actually realized. However, the recent progress in large-scale numerical simulations and the real-time digital-signal processing requires further improvement in CMOS speed.

A multiplier is an essential element in any digital signal processing circuit, and constitutes the critical path in DSP and FPU LSIs. Therefore, the demand for multiplier-performance improvement is increasing. Consequently, many fast multipliers based on various device technologies, e.g. Si bipolar, GaAs, JJ, have been reported. This paper describes a 0.5μm-CMOS 16x16b multiplier with a multiplication time of 3.8ns at a supply voltage of 4V, which is the fastest ever reported including bipolar[3] and HEMT[4] ICs. The circuit techniques and the technology used in this multiplier have the potential for 100MHz operation of 32-64bit floating point multiplication, thus realizing very fast DSP, FPU and ASICs.

A new family of advanced differential CMOS logic, complementary pass transistor logic(CPL) is proposed and fully utilized on almost the entire critical path to achieve this very fast speed. First, the CPL is introduced and then CPL implementation of the multiplier is described.

2. CPL: THE CONCEPT AND EXAMPLES

There have been several differential CMOS logic families proposed, such as CVSL[5] and DSL[6], for CMOS-circuit-speed improvement. These have the common features of complementary-data input/output, nMOS logic tree, and pMOS cross-coupled load, which can reduce input capacitance and increase logic-construction ability; thus, they were claimed to enhance speed. However, the actual advantage of these circuits is less than that anticipated in the original paper, as clarified in Ref.7. This is because the pMOS cross-coupled latch cannot easily be inverted due to the regenerative property of the latch.

The main concept behind CPL is the utilization of nMOS pass-transistor network for logic organization, instead of source-grounded nMOS trees in the conventional differential logic, as shown in Fig.1. CPL consists of complementary input/output, nMOS-pass-transistor logic network and CMOS output inverters. The pass transistors perform both pull-down and pull-up, thus pMOS latch can be eliminated, allowing the advantages of the differential circuits to be fully enjoyed in CPL. The CMOS output inverters amplify the output signal, increase the logic threshold voltage, and drive capacitive load. The logic-threshold shift is

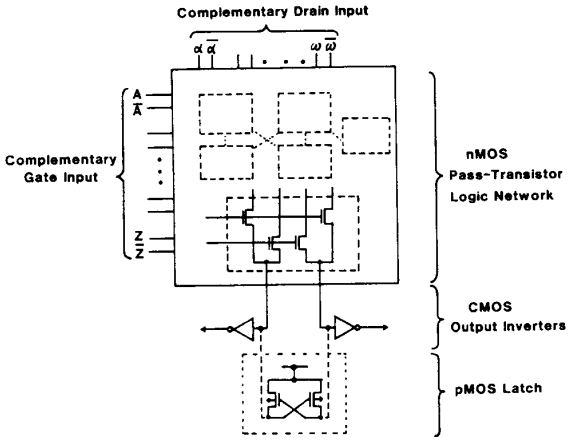

Fig.1 Basic circuit configuration in CPL.

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necessary, because the high level of the pass -transistor output is lowered from the supply voltage by the threshold voltage of the nMOS. These output inverters are "overhead", in the sense that they are needed whether the circuit has 1, 2, or many inputs. Therefore the overall device count will be minimized by designing with complex logic functions. The pMOS latch can also be added to CPL, as shown in Fig.1, in order to only decrease static power consumption, as opposed to the conventional pull-up function.

Arbitrary Boolean functions can be constructed from the pass-tranistor network by combining four basic circuit modules: an AND/NAND module, an OR/NOR module, an XOR/XNOR module and a wired-AND/NAND module, as shown in Fig.2, in which the XOR/XNOR module is used once[8]. Note that these various functions are produced by an identical circuit configuration with the change of input configuration. This property of CPL is apparantly suitable for masterslice design. The 3- and the more-way input logic functions can also be easily constructed similarly to the 2-way logic in Fig.2.

The CPL full adder, which is used in the present multiplier design, is shown in Fig.3(a). Since pMOS can be eliminated in logic construction, the input capacitance is about half that of the conventional CMOS configuration[3] shown in Fig.3(b), thus achieving higher speed and lower power dissipation. Moreover, the powerful logic-construction ability of CPL due to the multi-level pass-transistor network realizes complex Boolean functions efficiently in a small number of MOS transistors, thus reducing area and delay time. In fact, the transistor count in CPL full adder is 28 in the active area of $3.7\times11.4mm^2$, whereas in CMOS it is 40 in the area of $5.5\times8.6mm^2$. Further, the complementary -input/output function eliminates the internal inverter to provide XOR input in the full adder, thus reducing critical-path gate count. The measured worst delay time of the CPL full adder in a 10-stage full-adder chain is as small as 0.31ns/b, as shown in Fig.4. On the other hand, the conventional CMOS full adder, which is designed and fabricated on the same wafer, requires 0. 63ns/b. Thus the CPL is twice as fast as the conventional CMOS.

Another example of CPL in the multiplier is as a 4 -bit carry-look-ahead(CLA) unit used in a final 32b adder. The circuit of this unit is shown in Fig.5. The 32b adder includes 6 CLA units. The unit employs CPL to quickly transfer the carry-output to the upper unit(C4 and C4) after receiving the carry-input from the lower unit(C0 and C0). Complementary carry data can be inverted simply by twisting the carry lines. Thus the circuit requires only one pass transistor and a simple inverter to generate next-unit input. The measured delay time is only 0.15ns/4b.

3. MULTIPLIER ARCHITECHTURE

The 16×16-bit multiplier was designed using a parallel multiplication architecture, as shown in Fig.6. A Wallace-tree adder array and a CLA adder were used to minimize the critical-path gate stages. The critical path consists of a partial product generator, 7 full adders, a look-ahead carry generator, and 2 carry -propagate circuits (Fig.5).

4. DEVICE FABRICATION

The multiplier and the full-adder chains are fabricated with the double-level-metal $0.5\mu m$-CMOS technology. The minimum feature size is $0.5\mu m$, and the gate oxide thickness is 12.5nm. In this fabricated $0.5\mu m$-CMOS device optimized for CPL, the pass-transistor -nMOSs are designed to have a threshold voltage of 0V as shown in Figs.3 and 5. This reduces the static power dissipation and delay time. The interconnection metal consists of 1st-level W and 2nd-level Al. The W was adopted for its high immunity to electromigration.

5. PERFORMANCE RESULTS

A microphotograph of the multiplier is shown in Fig.7. The multiplier has 8500 transistors in an active area of $1.3\times3.1mm^2$, whereas the area including bonding pads is $1.6\times4.5mm^2$. The performance was measured using the worst case pattern, FFFF×8001-7FFF×8001. Circuit simulation was also performed to confirm that this pattern consists of a series of worst case operations of the full adder and the CLA. The multiplier chip was mounted on the 68-pin pin-grid-array ceramic package, followed by waveform observation of the clock inputs and the product outputs through the source follower circuit on the chip. The multiplication time was measured at both room and liquid nitrogen temperatures. The latter was considered for high-end applications, such as super computer. The maximum multiplication time was 3.8ns and 2.6ns at room and liquid-nitrogen temperatures, respectively, as shown in Figs.8, 9, and 10. Power dissipation was 257mW and 60mW at 300K and 77K, respectively, for 10MHz operation in a pattern of FFFF× FFFF-0000×FFFF.

Multiplication times at both room and liquid-nitrogen temperatures are faster than those of any other devices, including bipolar transistor, GaAs-MESFETs, and HEMTs, as is shown in Fig.11. In addition, the power dissipation of the multiplier is much lower than that of the other devices. The features of this multiplier are summarized in Table 1.

6. CONCLUSIONS

This paper described a fast 16×16-bit multiplier using a new differential CMOS logic family, CPL. In CPL, differential logics are constructed without pMOS latching load, thus the speed is twice as fast as

conventional CMOS. The multiplier is the fastest ever reported at both 300K and 77K, proving that the half micron CMOS technology fully utilizing CPL at least has a speed which is competitive with those of other fast devices with a much smaller power dissipation at room temperature, and is faster at liquid-nitrogen temperature.

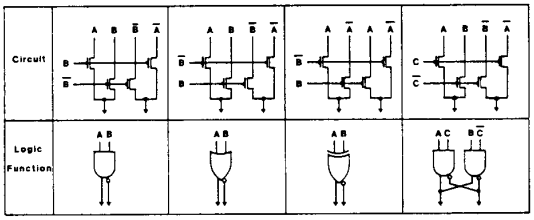


Fig.2 Circuit modules in CPL.

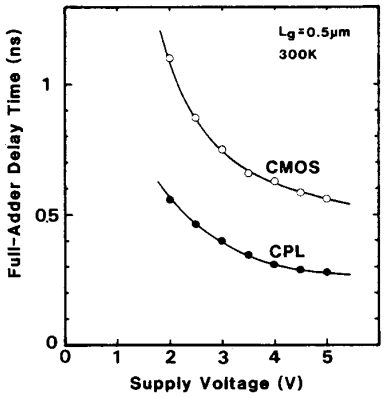


Fig.4 Full-adder delay time vs. supply voltage.

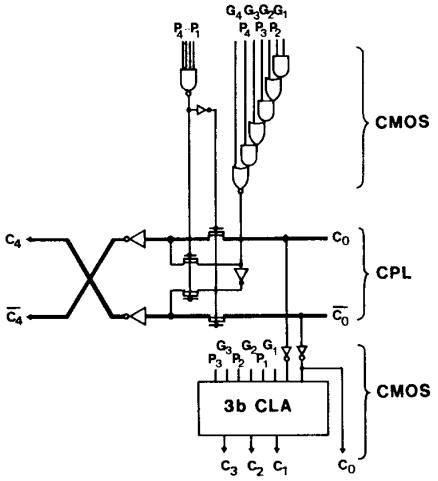
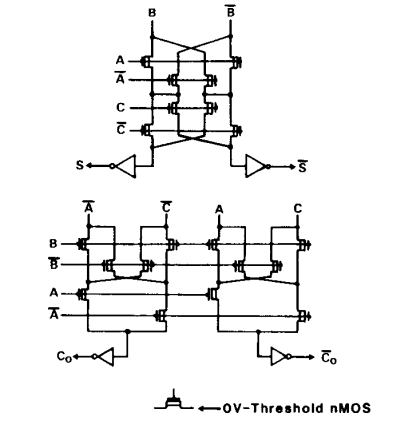
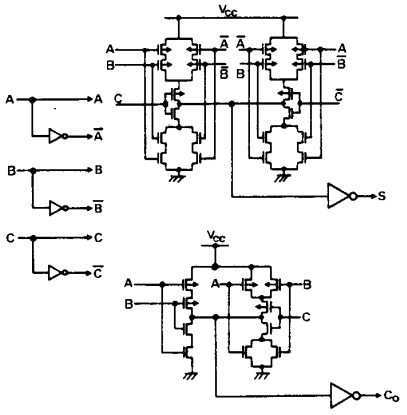


Fig.5 4-bit carry-look-ahead circuit using both CMOS and CPL. Cj: carry, Gj: generator, Pj: propagator.



(a)



(b)

Fig.3 Full-adder circuit (a)CPL, (b)CMOS.

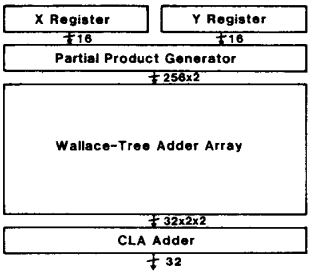


Fig.6 Block diagram of 16×16b multiplier.

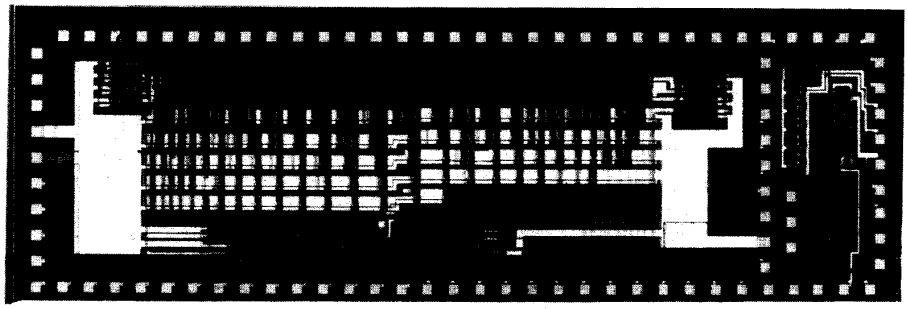


Fig.7 Microphotograph of the 16×16b multiplier chip(left) and 10-stage full-adder chains(right)

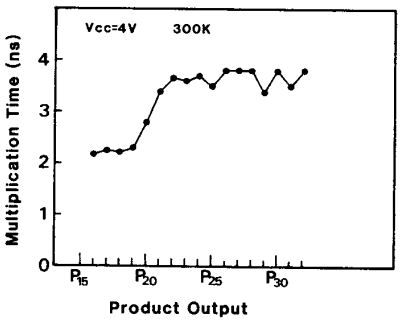


Fig.8 Measured multiplication time.

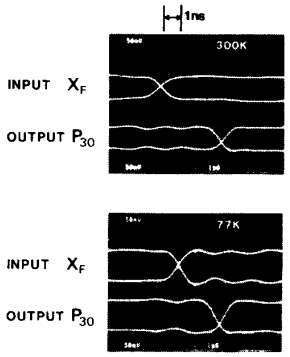


Fig.9 Measured waveforms

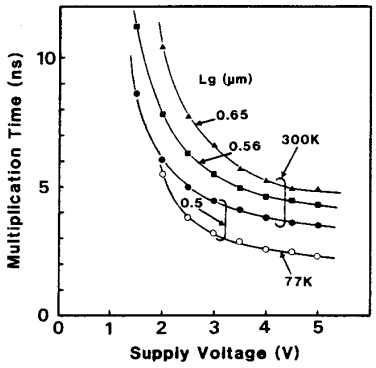


Fig.10 Measured multiplication time vs. supply voltage.

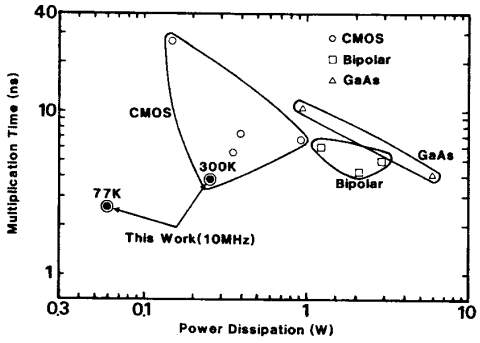


Fig.11 Comparison of delay and power dissipation of high speed 16×16b multipliers.

Table 1. Features of 16×16 bit parallel multiplier

Architecture	Wallace Tree + Carry Look Ahead			
Technology	0.5μmCMOS			
Gate Length	0.5μm			
Gate Oxide Thickness	12.5nm			
Metal Line/Space W	0.8/0.8			
Al	1.0/1.0			
Active Area	1.3x3.1mm²			
Transistor Count	8500			
Multiplication Time	3.8ns	(@4V, 300K),	2.6ns	(@4V, 77K)
Power Dissipation(10MHz)	257mW	(@4V, 300K),	60mW	(@4V, 77K)

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