TA 5.4: A 1.5ns 32b CMOS ALU in Double Pass-Transistor Logic

Makoto Suzuki, Norio Ohkubo, Toshiaki Yamanaka, Akihiro Shimizu[1], Katsuro Sasaki

Hitachi, Ltd./[1]Hitachi VLSI Engineering Corp., Tokyo, Japan

A 32b CMOS ALU, fabricated using 0.25μm CMOS technology, has 1.5ns addition time with 2.5V supply. This addition time is achieved using double pass-transistor logic (DPL) and a conditional carry-selection (CCS) carry look-ahead circuit.

Enhancing the performance of macros such as ALUs is a key to constructing a high-performance microprocessor that uses macro-intensive design for high MIPS performance. Several pass-transistor logic families for macrocell design, such as complementary pass-transistor logic (CPL), have been proposed for increasing the speed of CMOS circuits [1]. The CPL circuit has, because of input capacitance and functionality, been proven to be fast, but CPL implementation, particularly for low-voltage design, must take into account noise margin and speed degradation caused by mismatched input signal level and the logic threshold voltage of the CMOS inverter, both fluctuating independently with process variations.

Figure 1 shows the circuit of a double pass-transistor logic (DPL) gate for AND/NAND or XOR/XNOR. Figure 2 shows a full adder using the DPL gates. The DPL gate consists of complementary inputs/outputs, nMOS and pMOS pass-transistors, and CMOS output buffers. Current paths for S and Co outputs, when A=B=C="L level", are shown by the bold line in Figure 2. The main feature of the DPL gate is that two pass-transistors provide current paths for any pull-down or pull-up operation. This double-transmission characteristics of the DPL circuit compensates the speed degradation due to the usage of pMOS, and it allows the full-swing essential at low-supply voltage. In the DPL design, the widths of nMOS and pMOS pass-transistors are respectively one-third and two-thirds that of the nMOS pass-transistor in the CPL gate. The area penalty of the DPL gate, compared with the CPL gate, is small because the total DPL gate width is the same as that of the CPL gate. For the worst-case pattern, the DPL full adder is as fast as CPL, 18% faster than the conventional pass-transistor logic [2] with complementary inputs/outputs, and 37% faster than CMOS. As for the carry output delays that determine ALU speed, the DPL full adder is the fastest of these full adders.

The DPL gate is applied in the entire critical path of the ALU. The most important component in high-speed ALU design is the carry look-ahead. Figure 3 shows a 4b conditional carry selection (CCS) circuit compared with a conventional AND-OR carry look-ahead circuit. In the conventional circuit, generated carries (G_j) are propagated (P_j) through the AND-OR circuit chain to form a group-generate (GG) signal. In the CCS circuit, conditional carry signals for each bit, $C_j(0)$ (assuming incoming group-carry of "0") or $C_j(1)$ (assuming incoming group-carry of "1"), are selected by multiplexers according to conditional carry signals of the previous bit, $C_{j-1}(0)$ or $C_{j-1}(1)$.

$$
\begin{aligned}
C_j(k) &= G_j + P_j C_j\text{-}1(k) \\
&= G_j = X_j Y_j && \text{if } C_j\text{-}1(k) = 0 \\
&= G_j + P_j = X_j + Y_j && \text{if } C_j\text{-}1(k) = 1 \quad k = 1 \text{ or } 0
\end{aligned}
$$

This conditional carry-selection procedure finally forms the conditional-group carries, GC(0) and GC(1). Thus the critical path of carry propagation consists of three multiplexers instead of three AND and three OR gates. The CCS scheme also avoids the series connection of the pass-transistors comprising the multiplexers that is used in a transmission-gate conditional-sum adder [2]. Applying DPL for the critical path of the ALU with the conventional AND-OR carry look-ahead circuit reduces addition time 11% below that of an ordinary CMOS ALU. Using the CCS scheme for the carry look-ahead circuits reduces the addition time 30%, corresponding to one-generation advance of process technology.

The 32b ALU test chip with carry-select architecture uses 0.25μm triple-metal CMOS technology. The gate length is 0.25μm for both the nMOS and pMOS transistors. The gate oxide thickness is 6.5nm. Figure 4 is a block diagram of the 32b ALU. The DPL gate is used for all the circuits from the half adders (HA) to final conditional-sum selection (CSS) circuits. The CCS scheme is applied to the carry look-ahead circuit CLA1 as well as CLA2. The carry look-ahead circuit for the upper-half 16b (CLA2H) uses a conditional carry-selection method: group carry signals are generated assuming the carry of the lower-half 16b and are selected according to the incoming carry. This architecture enhances parallelism and results in fast operation. TX and TY signals select the function of the ALU. The test chip, measuring 1.58x0.38 mm^2, is shown in Figure 5. A CMOS ALU measuring 2.1x0.26 mm^2 has also been designed. The area penalty of the DPL ALU, compared with the CMOS ALU, is 10%. As shown in Figure 6, addition time is 1.5ns with a supply voltage of 2.5V. At 50MHz operation with about 12% gate activity, power dissipation is 8.0mW. Figure 7 shows the measured supply-voltage dependence of ALU addition time, revealing excellent low-voltage performance and the agreement with the results of circuit simulation. DPL AND/NAND and OR/NOR ring oscillators show measured speed improvements of 15% and 30% over CMOS NAND and NOR ring oscillators. DPL gates and the CCS adders also enhance performance of other macros such as floating-point units.

Acknowledgments

The authors thank K. Shimohigashi, T. Nishimukai, T. Nagano, M. Hiraki for their useful discussions. The authors are greatly indebted to T. Nishida, N. Hashimoto, N. Ohki, and H. Ishida for their process technology and device fabrication.

References

[1] Yano, K., et al., "A 3.8-ns CMOS 16x16-b Multiplier Using Complementary Pass-Transistor Logic", IEEE J. Solid-State Circuits, vol. 25, pp. 388-395, April 1990.

[2] Rothermel, A., et al., "Realization of Transmission-Gate Conditional-Sum (TGCS) Adders with Low Latency Time", IEEE J. Solid-State Circuits, vol. 24, pp. 558-561, June 1989.

0-7803-0987-1 / 93 / $3.00 / © 1993 IEEE

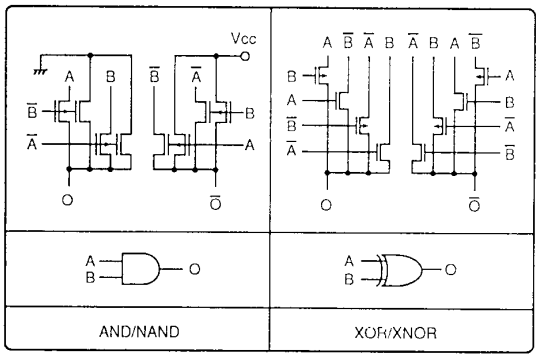

Figure 1: Double pass-transistor logic (DPL) gates.

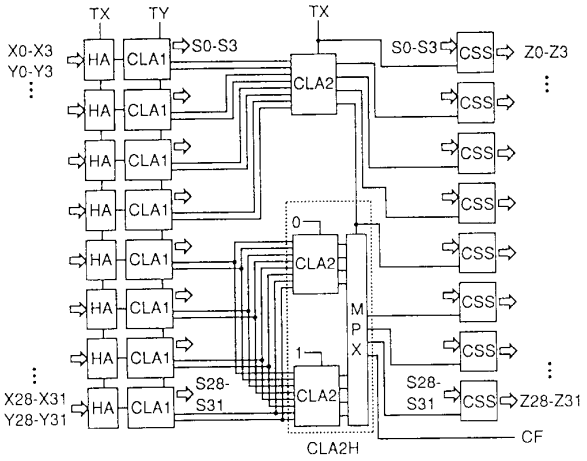

Figure 4: Block diagram of the 32b ALU.
Figure 5: See page 267.

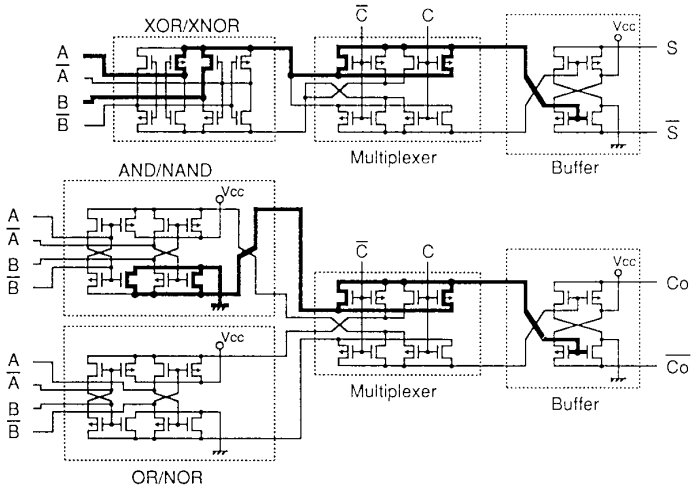

Figure 2: DPL full adder.

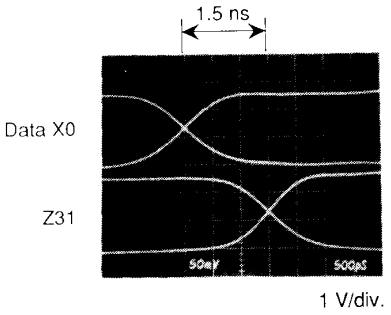

Figure 6: Measured 32B alu waveforms.

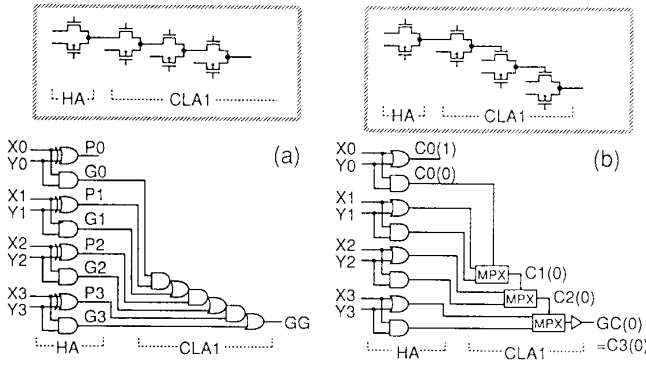

Figure 3: Carry look-ahead (CLA) circuit.

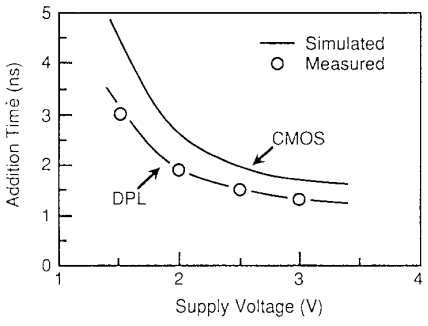

Figure 7: Addition time of 32b ALUs vs. supply voltage.

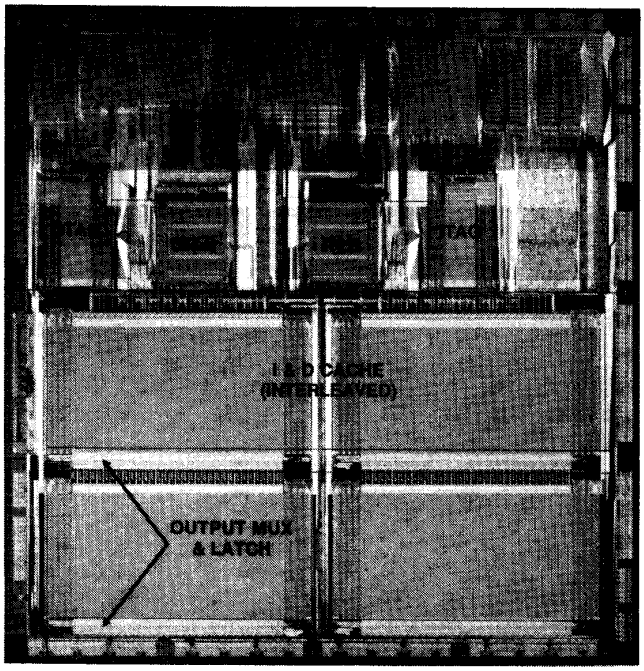

Figure 2: 256kb CAMMU chip micrograph.

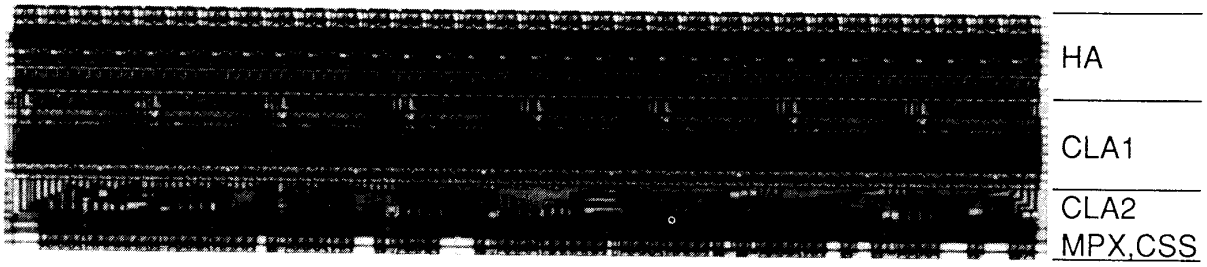

Figure 5: Micrograph of the 32b ALU (1.58x0.38mm²)