A 1.5-ns 32-b CMOS ALU in Double Pass-Transistor Logic

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***Abstract*—This paper describes circuit techniques for fabricating a high-speed adder using pass-transistor logic. Double pass-transistor logic (DPL) is shown to improve circuit performance at reduced supply voltage. Its symmetrical arrangement and double-transmission characteristics improve the gate speed without increasing the input capacitance. A carry propagation circuit technique called conditional carry selection (CCS) is shown to resolve the problem of series-connected pass transistors in the carry propagation path. By combining these techniques, the addition time of a 32-b ALU can be reduced by 30% from that of an ordinary CMOS ALU. A 32-b ALU test chip is fabricated in 0.25-μm CMOS technology using these circuit techniques and is capable of an addition time of 1.5 ns at a supply voltage of 2.5 V.**

I. Introduction

ENHANCING the performance of macros is essential to the construction of high-performance microprocessors where macrointensive design is used to achieve a high MIPS performance. Of the many data path macros, ALU's, or adders, are the key components in processor chips for ALU's in execution units, floating-point adders, and final carry propagation adders in floating-point multipliers and digital signal processing units. A number of fast adder architectures have been proposed in the long history of computer arithmetic [1]–[7], some of which use pass-transistor logic for carry propagation [6], [7]. Pass-transistor logics gain their speed advantage over CMOS due to their high logic functionality. However, a problem with this architecture is the series connection of the pass transistors in the carry propagation path.

This paper describes circuit techniques for realizing a faster adder using pass-transistor logic. A carry propagation technique called conditional carry selection (CCS) has been developed to solve the series connection problem, and double pass-transistor logic (DPL) has been developed to improve circuit performance at reduced supply voltage. A symmetrical arrangement and the double-transmission characteristics of the DPL gate compensate for the speed degradation due to the usage of both PMOS and NMOS pass transistors. Applying these circuit techniques, the addition time of a 32-b ALU can be reduced by 30% from that of an ordinary CMOS ALU. A 1.5-ns 32-b ALU has been developed using 0.25-μm CMOS technology and these circuit techniques [8].

Double pass-transistor logic and its characteristics are discussed in Section II. The conditional carry-selection circuit is described in Section III. Section IV describes the architecture and simulated results of a fabricated 32-b ALU test chip. Some experimental results are shown in Section V, and the conclusions are summarized in Section VI.

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II. Double Pass-Transistor Logic

Several pass-transistor logic families for macrocell design have been proposed for improving the performance of CMOS circuits. Complementary pass-transistor logic (CPL) [9] is one example; it has been applied to the full adders in multiplier circuits and has been shown to result in high speed due to its low input capacitance and high logic functionality. However, when implementing CPL, particularly in reduced supply voltage designs, it is important to take into account the problems of noise margins and speed degradation. These are caused by mismatches between the input signal levels and the logic threshold voltage of the CMOS inverters, which fluctuates with process variations. DPL is a modified version of CPL that meets the requirement of reduced supply voltage designs.

A. DPL Gate

A basic circuit diagram of a DPL gate is shown in Fig. 1. By simply exchanging the input nodes, two-input AND/NAND, OR/NOR, XOR/XNOR gates and multiplexers can be constructed. The DPL gate consists of complementary inputs/outputs and is thus a dual rail logic like CPL. Dual rail logic has been widely used for other logic families, such as clocked CVSL [10], and for self-timed logic [11] and bipolar DCS logic [12]. DPL gates consist of both NMOS and PMOS pass transistors, in contrast to CPL gates, where only NMOS pass transistors are used.

Fig. 2 compares the construction of XOR gates in CPL, CMOS, and DPL pass-transistor logics. The CPL gate consists only of NMOS transistors, resulting in low input capacitance and high-speed operation. However, the above-mentioned problems are caused by the high output signal level being lower than the supply voltage V_{CC} by the NMOS threshold voltage V_{th}. The usual way to avoid this is to use CMOS pass-transistor logic. Full-swing operation is attained by simply adding PMOS transistors in parallel with the NMOS transistors. However, this addition results in increased input capacitance.

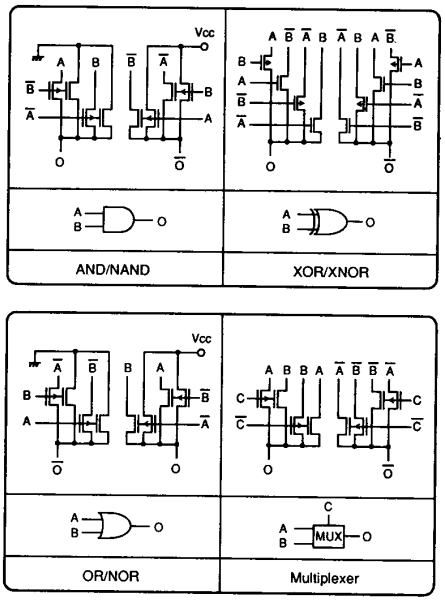

Fig. 1. Double pass-transistor logic (DPL) gates.

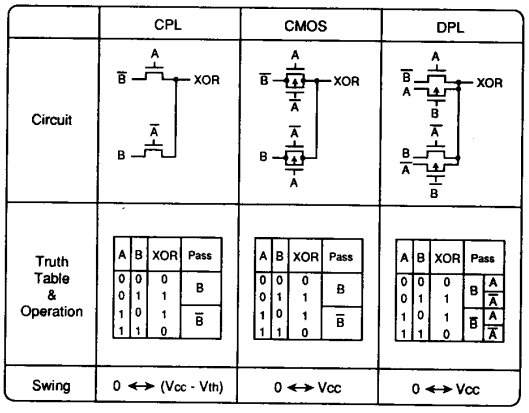

Fig. 2. Comparison of CPL, CMOS, and DPL pass-transistor logics for XOR gates.

In the DPL gate, the inputs to the gates of the PMOS transistors are changed from A to B. This arrangement compensates for the speed degradation of CMOS pass-transistors in two ways. First, it is a symmetrical arrangement whereby any input is connected to the gate of one MOSFET and the source of another. In the case of the XOR/XNOR, as can be seen in Fig. 1, it is perfectly symmetrical. Any of the inputs A, $\overline{A}$, B, and $\overline{B}$ is connected to the gates of the NMOS and PMOS and to the sources of the NMOS and PMOS. This results in a balanced input capacitance and reduces the dependence of the delay time on data.

Secondly, it has double-transmission characteristics. The truth tables in Fig. 2 show how the pass transistors operate for the XOR function. In this table, the column labeled Pass shows which signals are passed and performs the XOR function. For example, in the DPL gate, both A and B are passed when A and B are low. In both the CPL and CMOS implementations, the gate input A or $\overline{A}$ controls the pass transistors. When A is low, B is passed, and $\overline{B}$ is passed when A is high. In the DPL gate, on the other hand, there are two types of pass transistors: one is controlled by A and the other by B. The A-controlled pass transistors operate in the same way as CPL and CMOS. For the B-controlled pass transistors, when B is low, A is passed, and $\overline{A}$ is passed when B is high. As a result, there are always two current paths driving the buffer stage.

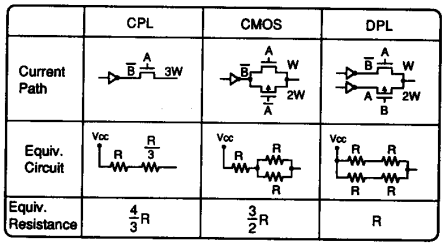

Fig. 3. Comparison of equivalent resistance for CPL, CMOS, and DPL pass-transistor logics.

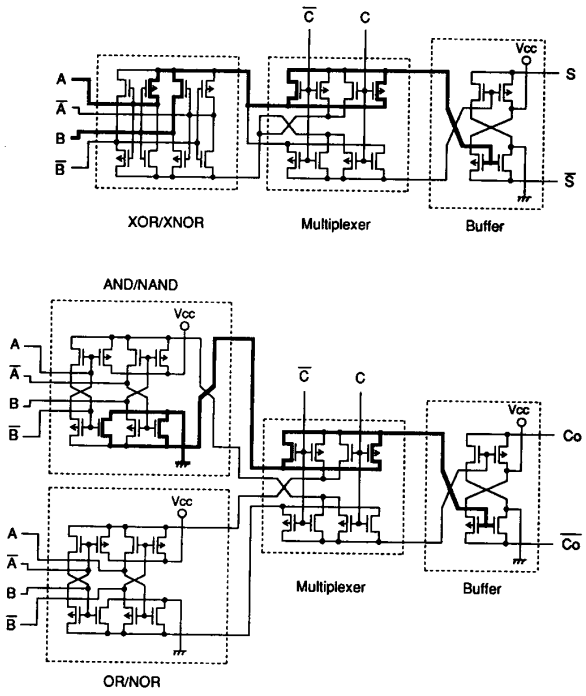

Fig. 4. DPL full adder.

Fig. 3 compares the equivalent resistance of the pass transistors. In order to compare the driving source impedance, the equivalent resistance includes that of the CMOS buffer with the same input capacitance. This comparison is rather simplified, but it qualitatively illustrates the double-transmission property. In the DPL design, the widths of the NMOS and PMOS pass transistors are one-third and two-thirds, respectively, of the NMOS pass transistor in the CPL gate, so the input capacitance and the gate area are nearly the same for all these architectures. As shown in Fig. 3, the resistance, including that of the CMOS buffer of the previous stage, is smallest for the DPL gate due to its double-transmission property.

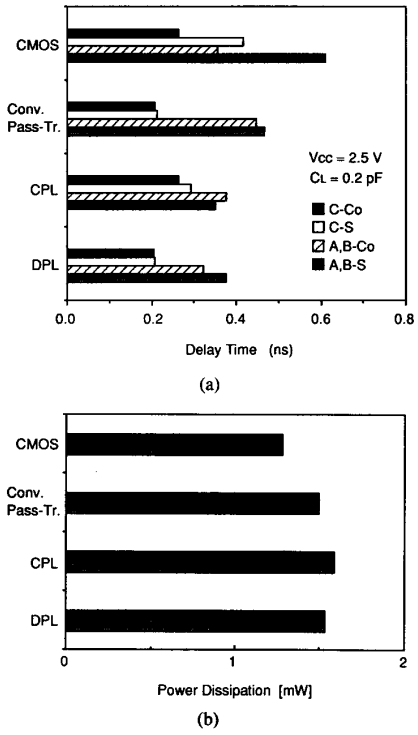

Fig. 5. Comparison of four types of full adders. (a) Delay times. (b) Power dissipation.

B. DPL Full Adder

We evaluated the speed advantage of the DPL gate using a full adder as an example. Fig. 4 shows the circuit of this full adder. The sum output portion consists of XOR/XNOR gates, a multiplexer, and a CMOS output buffer. The carry output portion consists of AND/NAND gates, OR/NOR gates, a multiplexer, and a CMOS output buffer. The current paths for the $\overline{S}$ and $\overline{Co}$ outputs when A, B, and C are all low, for example, are shown by the bold lines. These current paths include two pass transistors, and there are two current paths for each output, as discussed above.

Fig. 5 compares the simulated delay times and power dissipation of four kinds of full adders: CMOS [13], conventional CMOS pass-transistor logic [7] arranged in a dual rail structure, CPL [9], and DPL, with a load capacitance of 0.2 pF. For the slowest path that determines the speed of, for example, a multiplier, the DPL full adder is as fast as CPL, 18% faster than the conventional pass-transistor logic, and 37% faster than CMOS. As for the carry output delays ($C - Co$ and $A - Co$) that determine the ALU speed, the DPL full adder is the fastest of all. The power dissipation is simulated for 250-MHz operation with 0.2 pF loaded on each output regardless of whether it is single or dual rail logic. Under these conditions, the pass-transistor architectures show slightly higher power dissipation than CMOS because they have dual rail structure and double the load capacitance. The load capacitance determines which architecture dissipates the least power, and at lower load capacitance the dual rail pass-transistor architectures dissipate less power than CMOS.

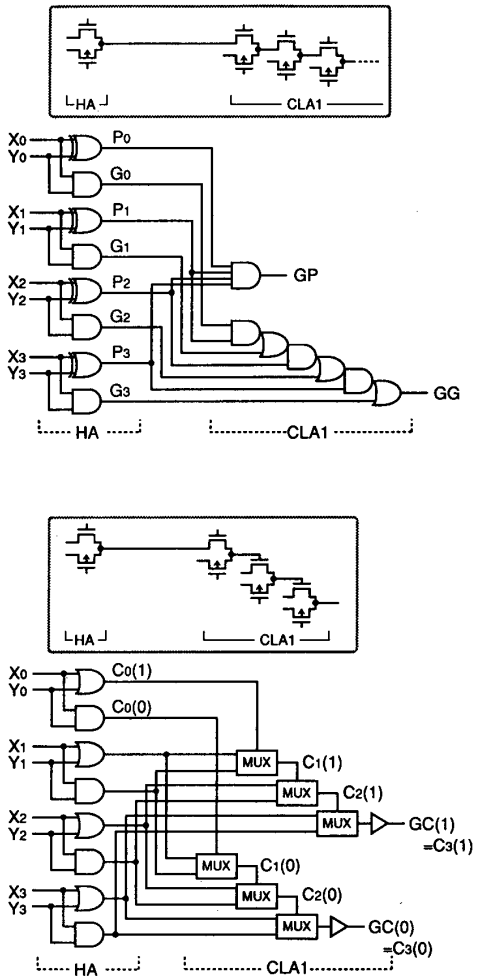

Fig. 6. 4-b carry look-ahead circuits. (a) Conventional AND–OR carry look-ahead circuit. (b) Conditional carry select (CCS) circuit.

III. Conditional Carry Selection Circuit

The most important component of high-speed ALU's is a look-ahead carry circuit. We have developed a new look-ahead carry scheme, called conditional carry selection (CCS). Fig. 6 compares a 4-b implementation of this scheme with a conventional AND-OR carry look-ahead circuit. In the conventional circuit [Fig. 6(a)], generated carry signals (G_j) are propagated (P_j) through an AND-OR circuit chain to form a group-generate (GG) signal, which is expressed as

$$\begin{aligned} C_3 &= G_3 + P_3 \cdot [G_2 + P_2 \cdot (G_1 + P_1 \cdot G_0)] \\ &\quad + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_{-1} \\ &= GG + GP \cdot C_{-1} \qquad (1) \\ GG &= G_3 + P_3 \cdot [G_2 + P_2 \cdot (G_1 + P_1 \cdot G_0)] \qquad (2) \\ GP &= P_3 \cdot P_2 \cdot P_1 \cdot P_0. \qquad (3) \end{aligned}$$

Thus, the 4-b carry look-ahead circuit involves three AND-OR circuits in its critical path. Furthermore, using pass-transistor

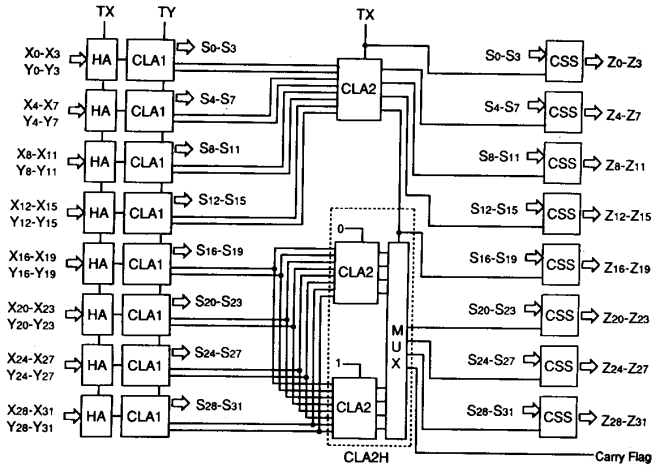

Fig. 7. Block diagram of the 32-b ALU.

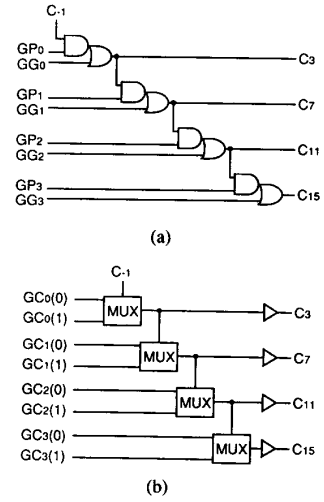

Fig. 8. Four-block carry look-ahead circuit CLA2. (a) Conventional AND-OR carry look-ahead circuit. (b) Conditional carry select (CCS) circuit.

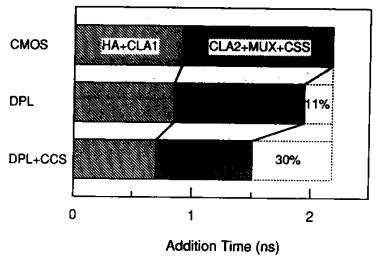

Fig. 9. Simulated comparison of 32-b ALU addition times.

logic, there are seven pass transistors connected in series, as shown in the inset figure above.

On the other hand, in the CCS architecture conditional carry signals for each bit $C_j(0)$ (assuming an incoming group carry of 0) or $C_j(1)$ (assuming an incoming group carry of 1) are selected by the multiplexers depending on the conditional carry signals of the previous bit, $C_{j-1}(0)$ or $C_{j-1}(1)$, as expressed by

$$C_j(k) = G_j + P_j \cdot C_{j-1}(k)$$
$$= G_j = X_j \cdot Y_j \quad (\text{if } C_{j-1}(k) = 0) \tag{4}$$
$$= G_j + P_j = X_j + Y_j \quad (\text{if } C_{j-1}(k) = 1) \tag{5}$$
$$k = 0 \text{ or } 1.$$

This conditional carry selection procedure finally forms the conditional group carries $GC(0)$and $GC(1)$. In this way, the critical carry propagation path can be constructed by three multiplexers instead of three AND-OR gates. As shown in Fig. 6(b), the CCS architecture also avoids the series connection of pass transistors in the multiplexers, as used in a transmission-gate conditional-sum adder [7], Manchester carry chain [14], or the AND-OR carry look-ahead circuit of Fig. 6(a).

IV. 32-b ALU Architecture

Fig. 7 shows a block diagram of the 32-b ALU based on carry select architecture [3]. DPL gates are used for all the circuits from the half adders (HA) to the final conditional-sum selection (CSS) circuits. The CCS architecture is applied not only to the 4-b carry look-ahead circuit CLA1 but also to the block carry look-ahead circuit CLA2, where four AND-OR circuits can be replaced with four multiplexers, as shown in Fig. 8. The CSS circuit consists of a multiplexer that selects the conditional sums, $S_j(0)$ or $S_j(1)$, according to the incoming block carry signal. In the carry look-ahead circuit, the upper 16 bits are processed by a conditional carry selection method whereby block carry signals are generated by CLA2, assuming the carry of the lower 16 bits C_{15} to be 0 or 1, and are then selected by the multiplexer according to the incoming true carry. This architecture enhances parallelism and results in fast operation. This is because the carry signals of the upper 16 bits are calculated in parallel with those of the lower 16 bits, and the carry signals of the upper 16 bits are generated after the delay time of a single multiplexer. The TX and TY signals select the function of the ALU.

Fig. 9 compares the simulated addition times of 32-b ALU's. An ordinary CMOS ALU uses the carry look-ahead circuits

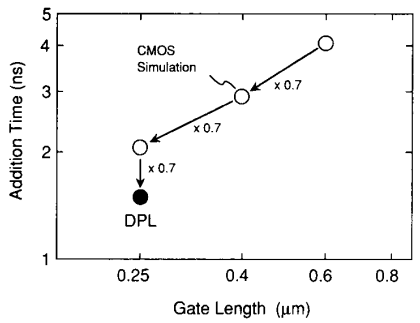

Fig. 10. Simulated addition time improvement with decreasing device dimensions.

TABLE I
PROCESS TECHNOLOGY

Technology	0.25-μm CMOS Triple Metal
MOSFET	
Gate Length	0.25 μm
Gate Oxide	6.5 nm
Contact/Via 1	0.3 μm × 0.3 μm
Via 2	0.6 μm × 0.6 μm
First Metal Width/Space	0.5 μm / 0.4 μm
Second Metal Width/Space	0.5 μm / 0.4 μm
Third Metal Width/Space	0.7 μm / 0.6 μm

of Fig. 6(a) and Fig. 8(a) and the architecture of Fig. 7, with the CMOS combinational gates like a four-input AND-OR-NOT gate. The combination of DPL with a conventional AND-OR carry look-ahead circuit reduces the addition time by 11% from that of an ordinary CMOS ALU, and the combination of DPL with a CCS carry look-ahead circuit reduces the addition time by 30%. Fig. 10 shows the simulated reduction of addition time with decreasing device dimensions. The CMOS simulation was done for an ordinary CMOS ALU with decreasing supply voltages for each generation—5 V, 3.3 V, and 2.5 V, respectively. The addition time is reduced by 30% for each generation. Therefore, the 30% improvement of the DPL and CCS architecture corresponds to a one-generation advance in process technology.

V. EXPERIMENTAL RESULTS

The 32-b ALU test chip described above was fabricated using 0.25-μm triple-metal CMOS technology. The major process parameters are summarized in Table I. Actually, this test chip was fabricated on the same wafer as an SRAM test chip [15]. An i-line stepper was used for all layers. The first metal is tungsten, and the second and third metals are aluminum. A micrograph of the test chip is shown in Fig. 11. It measures 1.58 mm × 0.38 mm (0.6 mm^2). We also designed an ordinary CMOS ALU as discussed in Section IV that measures 2.1 mm × 0.26 mm (0.55 mm^2). The area penalty of the DPL ALU, compared with the CMOS ALU, is thus 10%. This device is capable of performing 32-b additions in 1.5 ns at a supply voltage of 2.5 V, as shown in the

Fig. 11. Micrograph of the 32-b ALU test chip.

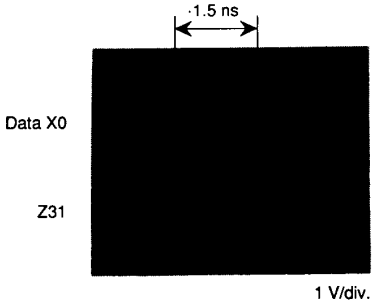

Fig. 12. Measured waveforms of the 32-b ALU test chip (1.58 mm × 0.38 mm).

TABLE II
CHARACTERISTICS OF THE 32-b ALU TEST CHIP

Organization	32-b ALU
Architecture	Carry Select Addition
Circuit	DPL
	CCS CLA
Addition Time	1.5 ns
Power Dissipation	8 mW (at 50 MHz)
Supply Voltage	2.5 V
Chip Size	0.60 mm^2

waveforms of Fig. 12. The power dissipation was measured at the maximum frequency limit (50 MHz) of the pattern generator and was found to be 8 mW with about 12% gate activity. This extrapolates to 107 mW at a 1.5-ns cycle time. The characteristics of this 32-b ALU test chip are summarized in Table II. Fig. 13 shows how the addition time depends on the supply voltage. The solid lines show the simulated results for CMOS and DPL ALU's, and the circles show the results for the DPL ALU measured at room temperature. The DPL ALU has an excellent low-voltage performance and agrees well with the results of circuit simulation. DPL AND/NAND and OR/NOR ring oscillators have also been fabricated, showing speed improvements of 15% and 30% compared with CMOS NAND and NOR ring oscillators, respectively.

VI. CONCLUSION

Double pass-transistor logic (DPL) has been developed to improve circuit performance at reduced supply voltage. Its symmetrical arrangement and double-transmission characteristics compensate for the speed degradation arising from the use of PMOS and NMOS pass transistors. A carry propagation circuit technique called conditional carry selection (CCS) has been developed to solve the problem of series-connected pass transistors in the carry propagation path. By combining these

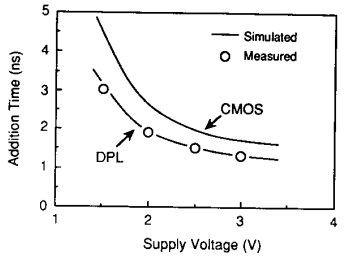

Fig. 13. Variation of the addition time of 32-b ALU's with supply voltage.

circuit techniques, the addition time of the 32-b ALU can be reduced by a substantial 30% from that of an ordinary CMOS ALU. A 1.5-ns 32-bit ALU has been developed using 0.25-μm CMOS technology and these circuit techniques. It should also be possible to apply the proposed DPL gates and CCS adder architecture to other data path macros, such as floating-point units, resulting in processing units with very high performance.

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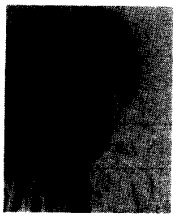

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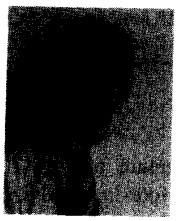

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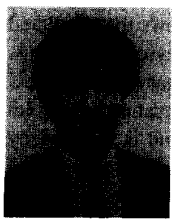

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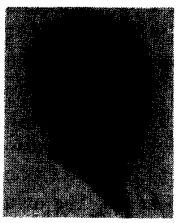

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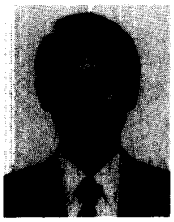

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