TP 5.6: 0.5V SOI CMOS Pass-Gate Logic

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Demand for low-power ULSIs for mobile electronic equipment is increasing rapidly. To reduce power consumption, lower operating voltage and minimized device size (or count) is essential. To lower the actual threshold voltage and lower the operation voltage, SOI MOSFET with gate-body connection is proposed [1]. However, the circuit architecture that affords the maximum advantage of the body controlled SOI MOSFET is not reported. This SOI CMOS pass-gate logic offers the lowest operation voltage and reduced transistor dimensions.

Figure 1 shows conventional and proposed pass-gate logic. In the conventional complementary pass-gate logic (CPL, Figure 1a), the high-level signal of the pass-gate network is less than the supply voltage, Vcc [2]. This is because the pass-gate turns off when the source voltage reaches Vcc-Vt, where Vt is the threshold voltage of pass-gate which is increased by the body-effect. The drive capability of the network is degraded due to the channel resistance of pass-gates, so the output signal from the pass-gate network is amplified by using the buffer. In SOI CMOS pass-gate logic (Figure 1b, c), the body of SOI pass-gate is connected to the input signal given to the gate. Low threshold voltage for the on-state pass-gate and high threshold voltage for the off-state pass-gate is realized, and the increase in the threshold voltage due to the body-effect is suppressed. Two types of buffer suitable for the SOI pass-gate logic are examined. The buffer used in the Type A logic is composed of two CMOS inverters and a pMOS latch circuit, as shown in Figure 1b. The body of the MOSFET is connected to the gate (gate-body connection, GBC scheme). For the buffer used in the Type B logic, pull-up pMOSFETs are cross-coupled [3]. The body of the cross-coupled pull-up pMOSFET is connected to the buffer input, (input-body connection, IBC scheme), as shown in Figure 1c. Figure 2 shows the full-adder delay versus supply voltage. For SOI pMOS / nMOSFETs, the absolute value of the threshold voltage is 0.4V at 0V body-bias, and is 0.17V at 0.5V body-bias. Due to the low threshold voltage for the on-state MOSFET in the GBC scheme, the Type A full-adder reduced the delay to 1/3 of that of the conventional SOI CPL at 0.5V. Lowest operation voltage, V_{CCmin}, is improved by 0.17V by the GBC scheme, where V_{CCmin} is defined as the supply voltage which gives 2ns delay.

Transistor dimension are optimized for Type A (GBC) and Type B (IBC) pass-gate logic. The major difference between Type A and Type B logics is that the pass-gate network drives only two nMOSFETs in the Type B logic, while the pass-gate network drives two nMOSFETs and two pMOSFETs in the Type A logic. Figure 3 shows the full-adder delay versus the gate-width of the pass-gate network. By use of optimized buffer dimensions (Wp/Wn=0.6, Wu/Wn=0.4 for the Type B logic, and Wp/Wn=2.0, Wu/Wn=1.1 for the Type A logic), the optimum pass-gate width of the Type B logic is 0.6Wn, while that for the Type A logic is 1.3Wn. As a result, the total transistor dimension of the Type B logic is less than half that of the Type A logic.

The buffer using cross-coupled pull-up pMOSFETs reduces total transistor dimensions. There are two design options to control the body-bias. Figure 4 shows two types of buffer chain using the cross-coupled pull-up pMOSFET. One type uses the GBC scheme, and the other uses the IBC scheme (Figure 4). In the buffer using the GBC scheme, the on-state pull-up pMOSFET keeps high threshold voltage until the output node responds. This is because the body of the pull-up pMOSFET is connected to the output node. In the buffer using the IBC scheme, on the other hand, the threshold voltage of the on-state pull-up pMOSFET decreases before the output node responds. As a result, the buffer using the IBC scheme operates with high-speed and small short-circuit current, compared with the buffer using the GBC scheme.

A 40-stage buffer chain is used to measure the speed advantage of the buffer using the IBC scheme, in the Type B logic. A micrograph of the test chip is shown in Figure 5. Figure 6 shows the ratio of the buffer delay with the IBC scheme to that with the GBC scheme versus supply voltage. Measured threshold voltage of the SOI MOSFET is 0.58V at the body-bias of 0V, and 0.35V at the body-bias of 0.5V, respectively. The IBC scheme is 36% faster than the GBC scheme at 0.5V, and the V_{CCmin} is improved by 0.08V. Type B logic using the IBC scheme is 10 times faster than the CPL, and the minimum operation voltage is improved by 0.25V.

Multiplication is useful for estimating the logic performance. In the pass-gate full-adder using the buffer with the IBC scheme, the dissipation is reduced by 0.5V operation and reduced transistor dimensions. For a 16x16b multiplier using a Wallace-tree adder and CLA adder, the simulated multiplication time is 18ns at 0.5V. And the power-delay product is 70pJ including 50pF I/O, was more than an order of magnitude improvement for the CPL (Figure 7).

Acknowledgments:

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References:

[1] Assaderaghi, F., et al., "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," IEDM Techical Digest, pp. 809-812, Dec., 1994.

[2] Yano, K., et al., "A 3.8-ns CMOS 16μ 16-b Multiplier Using Complementary Pass-Transistor Logic," IEEE J. Solid-State Circuits, vol. 25, pp. 388-395, April, 1990.

[3] Heller, L. G., et al., "Cascade Voltage Logic: A Differential CMOS Logic Family," ISSCC Digest of Techical Papers, pp. 16-17, Feb., 1984.

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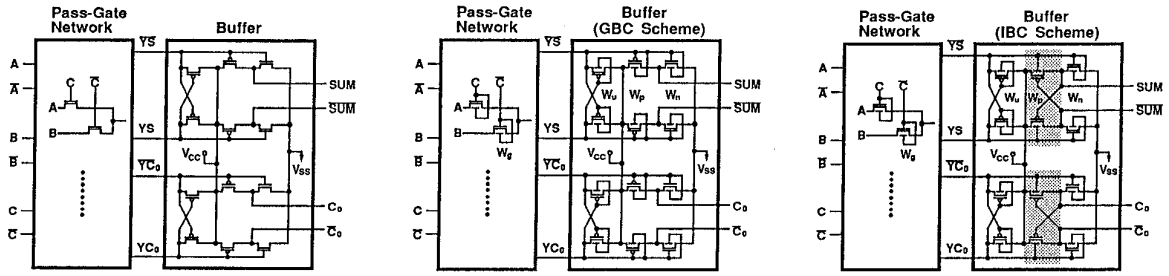

Figure 1: Conventional and proposed pass-gate logic. (a) CPL, (b) Type A, (c) Type B.

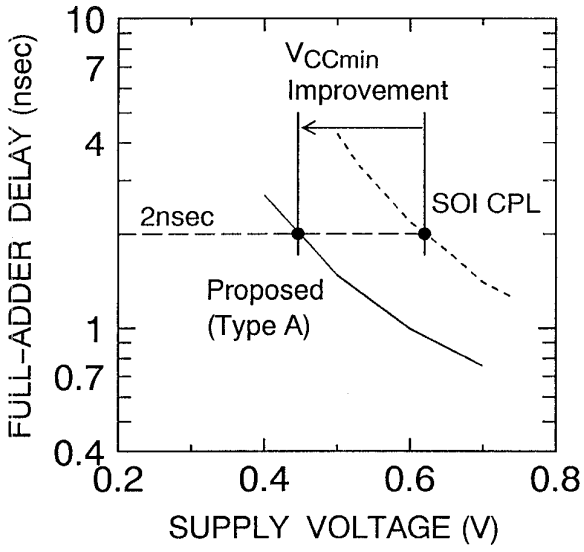

Figure 2: Simulated full-adder delay vs. supply voltage.

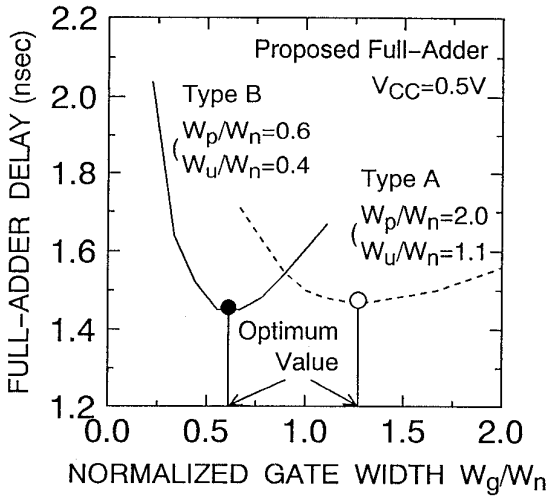

Figure 3: Gate-width optimization for pass-gate logic.
Figures 4 and 5: See page 424.

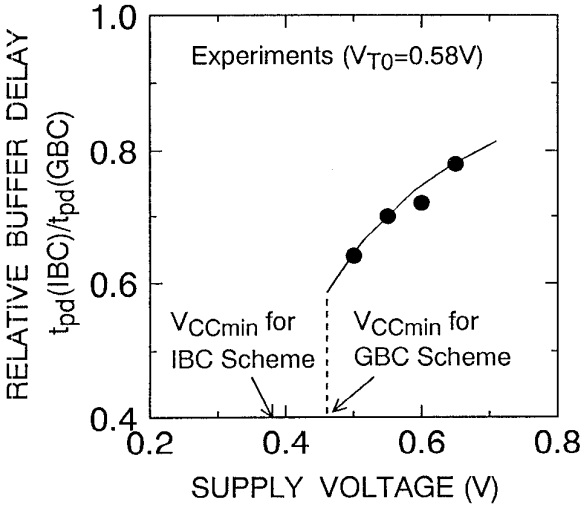

Figure 6: Measured buffer delay vs. supply voltage.

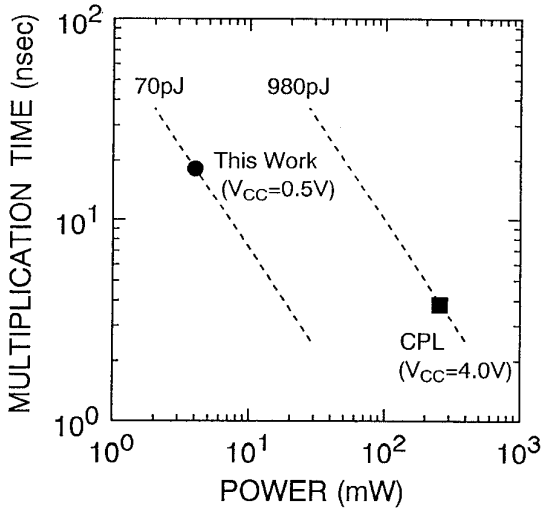

Figure 7: 16x16b multiplier power-delay product.

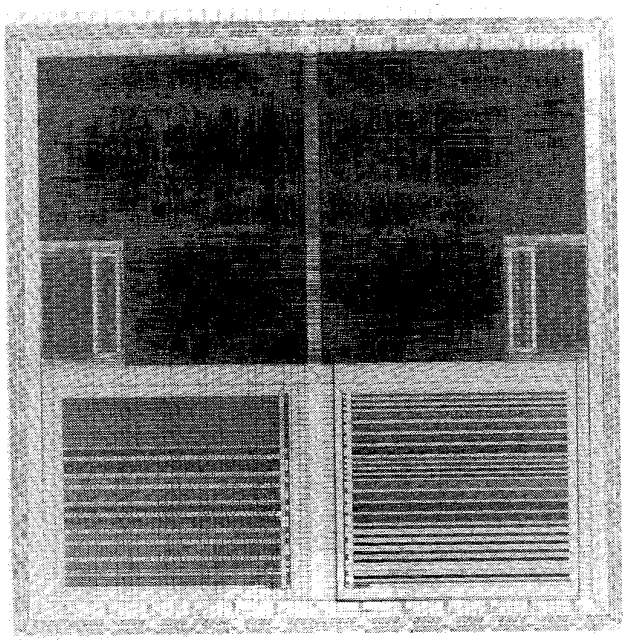

Figure 3: 10mm² 3M-transistor gate array LSI micrograph. upper: gate array(120kgate 8.7kb 2-port sRAM) lower: test circuits.

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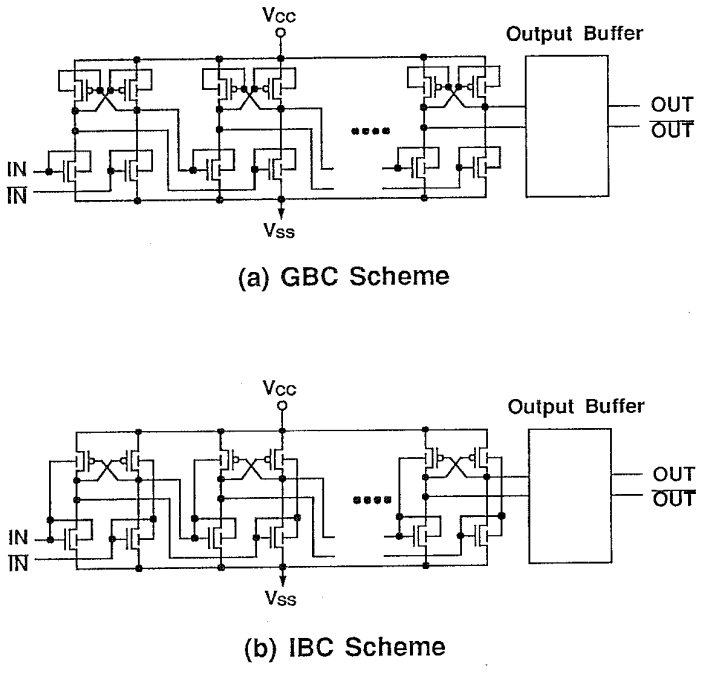

Figure 4: Buffer chain schematics: (a) GBC (b) IBC .

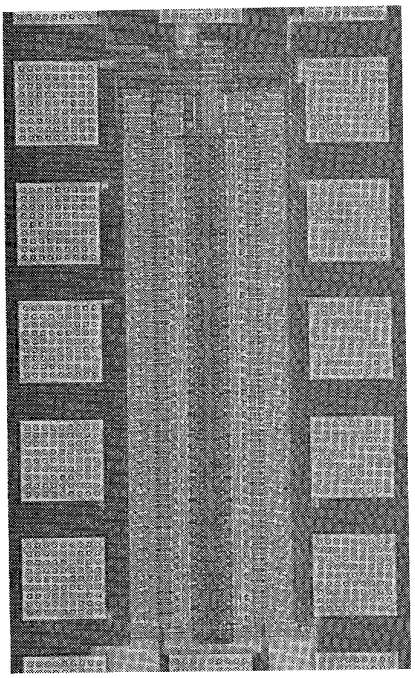

Figure 5: Chip micrograph.