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Power Analysis of a Programmable DSP for Architecture/Program Optimization

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Introduction

Power consumption has become one of the primary metrics in CMOS LSI design. A high level power estimation model will be indispensable to evaluate architectures and programming styles for performance and power consumption optimization. A model was proposed in which a constant energy was used for every module but data dependency was not taken into account[1,2]. The purpose of this paper is to quantify the module break down and the data dependency of the power consumption and to find a key for high level power estimation. We analyzed power consumption of a 24bit fixed point DSP, HX24, which we developed previously[3]. We have found that the buses don't consume as much power as we originally expected while the data operation modules consume much power and the data dependency caused about 30% variation in worst case chip power. This is the first paper that describes how large the data dependency of data operation is and how low the bus power consumption is in a DSP of an extended Harvard architecture.

Switch level and Cell based power simulation

We analyzed power using a switch level and cell based simulation. The simulation causes errors by (a) ignoring power caused by short circuit current, (b) ignoring power caused by switching capacitance inside cells, and (c) regarding intermediate swings as full swings. The extreme case of (a) is signal conflict, but we assume that signal conflict never occurs in a correct design. We estimate that an error of -7 to -10% is caused by ignoring the short circuit current. We compensate error (b) by increasing the simulated power by a factor that is derived from the load capacitance inside cells. With this compensation, the error is between -10% and -20%, while it is -30% to -40% without.

Module breakdown power

Fig. 1 shows the block diagram of HX24 and Fig. 2 shows a module break down of the power consumption with many test programs. Power consumption is normalized by the worst case chip power. We focus on the power of the data operation, clocking and buses in this paper.

'Data operation' consists of a register file, an ALU and a multiplier, and it consumes 3-33% . The data dependency is as large as 30% of the worst case power. Thus, ignoring the data dependency causes an error of as much as 30% in high level power estimation. Clock and bus circuits are dominant power consuming components in general. We separately evaluated the power consumed by clocking and bus driving, though they are already included in the modules. Clocking power is calculated by summing up all the load capacitance on the clock line from the source to a control gate that enables/disables the clock. The total is 17%. Bus power is calculated by multiplying the number of transitions and load capacitance on each bit of the buses. The bus power consumption is less than 5%, while it was reported that the bus power was 9% in a microprocessor[4].

Bus transition activity

In order to confirm the unexpected result of bus power, we evaluated the bus activity with two speech CODEC programs. Fig. 3 shows the activity on each bit of the buses. The activity here is defined as the average number of transitions per cycle. The activity of the address buses shown in (a), (b), and (c) is significantly small because successive accesses often refer successive memory locations. The activity of the data buses shown in (d), (e), and (f) is at most 2 because the data buses are precharged. If the data is white noise, the activity is 1. Fig. 3 demonstrates that the activity on the X and Y data buses is less than white noise, but the instruction activity is higher. The bus power is not dominant in an extended Harvard architecture because of less activity on address buses, while it is higher in von Neumann architecture because the bus is multiplexed.

Data dependency of data operation

Since the data operation modules consumed as much as 33% of the worst case chip power, we investigated more about the data path power. Fig. 4 and 5 show the data dependency of the ALU power for addition and the register file power respectively. The ALU power is in proportion to the number of transitions of the input data. The register file power is in proportion to the number of zero's, which is because the register file employs precharged circuit. Fig. 6 and 7 show the data dependency of the multiplier power. Two random data series are fed in to each input of the multiplier and there is no correlation between the power and the number of transitions of the input nor output(Fig. 6). When one of the inputs is fed by a constant value, we observe a good correlation between the power and the number of transitions of the other input(Fig. 7). In Summary, we found noteworthy hints for data path power estimation: 1) the register file power can be estimated by observing number of zero's of the input and output data, 2) the ALU power can be estimated by observing the number of transitions of the input, and 3) a constant value can be used to estimate the multiplier power as long as the both input change.

Conclusion

We demonstrated a module break down of a DSP power. We have found that the bus power is significantly small while the data path power is large. We obtained some noteworthy hints for high level power estimation of DSPs, which we believe useful for architecture and program optimization of DSP's in terms of power consumption.

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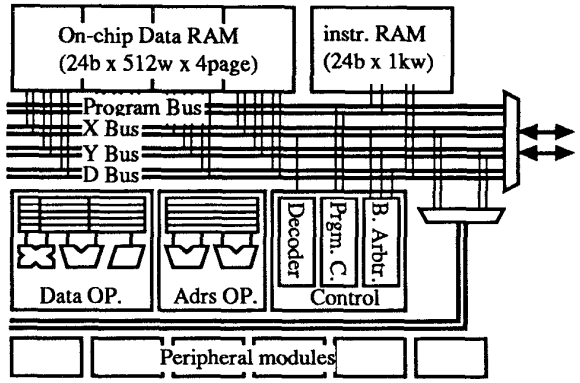

Fig. 1: Block diagram of HX24, a DSP under test[3].

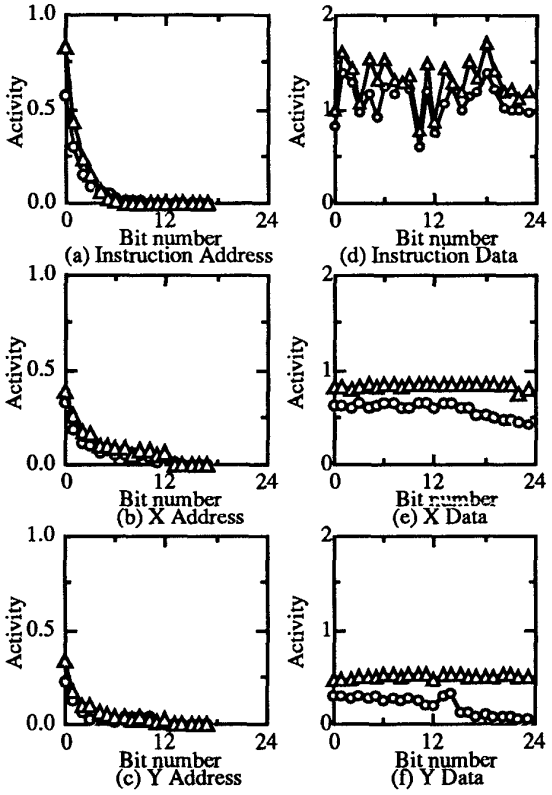

Fig. 3: Bus transition activity with application programs, calculated as the average number of transitions on each bit of the buses.

References

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[2] Ping-Wen Ong and Ran-Hong Yan, "Power-conscious Software design - a framework for modeling software on hardware," Symposium on Low Power Electronics, pp. 36-37, Oct. 1994.

[3] T. Baji, et al., "HX24 24-bit Fixed Point Digital Signal Processor," the International Conference on Signal Processing Applications and Technology, pp. 622-629, Oct. 1993.

[4] S. Kawasaki, "SH2: A low power RISC micro for consumer applications," Hot Chips IV, pp. 97-103, Aug. 1994.

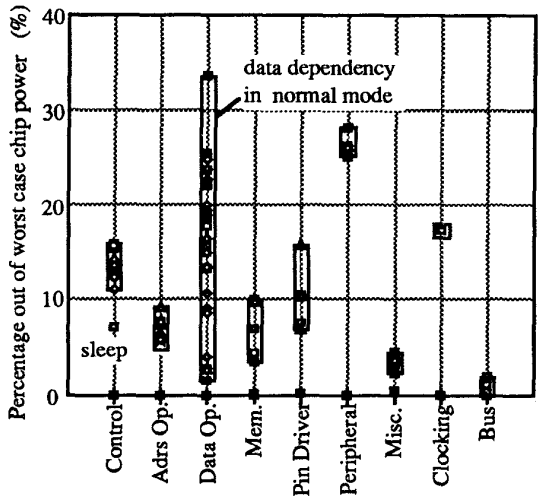

Fig. 2: Module break down of power analysis. Each plot represents a test program, and a white square on each category represents the range in use.

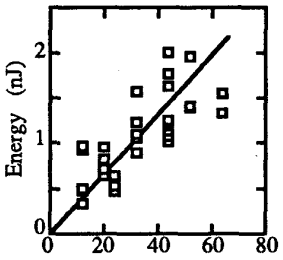

Fig. 4: Data dependency of ALU power for addition.

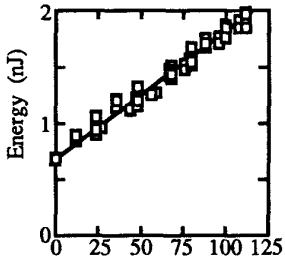

Fig. 5: Data dependency of register file power.

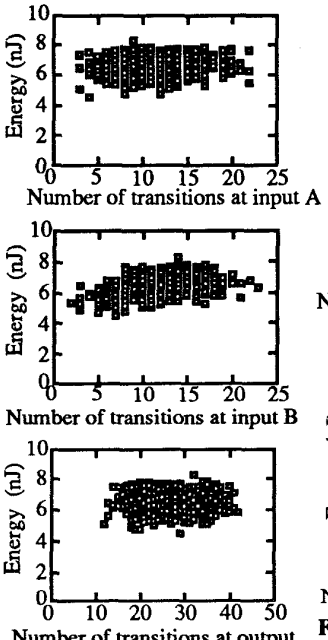

Fig. 6: Data dependency of multiplier power. Random data was fed to both inputs.

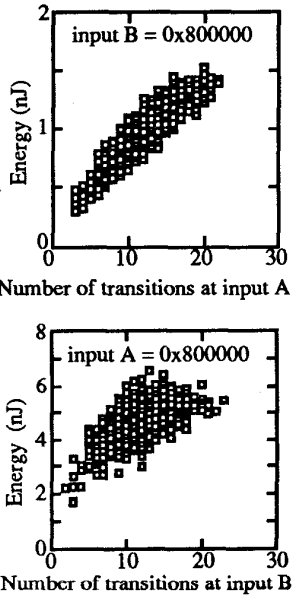

Fig. 7: Data dependency of multiplier power. Random data was fed to one of the inputs and the other input was constant.