UNIVERSITY OF CALIFORNIA, DAVIS
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

EEC280: Prof. Vojin G. Oklobdzija Fall 2004

YOUR NAME:

Quiz No.2

Circle the correct answers.

1. Moore's Law is limited by:

a) Technology Scaling
b) Interconnect RC-Delay
c) Power
d) Fabrication Cost

2. Leakage power is reduced using:

a) Strained Silicon devices
b) Tri-Gate Transistors
c) Adaptive Body Biasing

3. Impact of Variations in Circuit Design diminishes with:

a) Deeper Pipelined Architectures
b) Low-Vt Usage
c) Larger Transistor Sizes

4. Future Design Techniques are based on:

a) Multi-Variable Optimization
b) Freelance Layout
c) Minimizing area of the design

5. Testing and Verification challenges are faced with:

a) Exponential Increase of the test cost per tranisistor
b) Number of test transistors allowed on the chip
c) High-Speed and on-die "self-testing"
d) none of the above

6. Which technology first crossed the extreme UV lithography :

a) 180 nm
b) 130 nm
c) 65 nm
d) 45 nm
e) none of the above