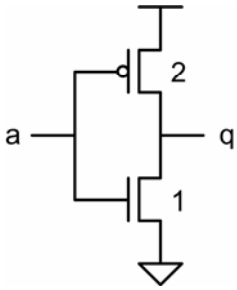
EEC280 **Fall 2005** **Homework #2**
Prof. Vojin G. Oklobdzija **Due: November 1, 2005**

For problems 1-5, normalize each answer for g and p to following reference inverter. Use equal pull-up and pull-down sizing unless stated otherwise.



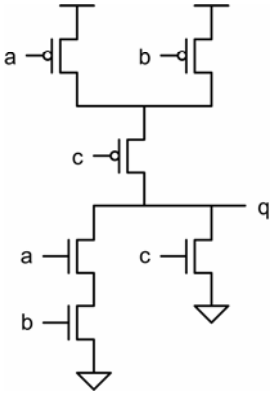
$$g = \frac{R_{gate} C_{in-gate}}{R_{inv} C_{in-inv}}$$

$$p = \frac{R_{gate} C_{p-gate}}{R_{inv} C_{in-inv}}$$

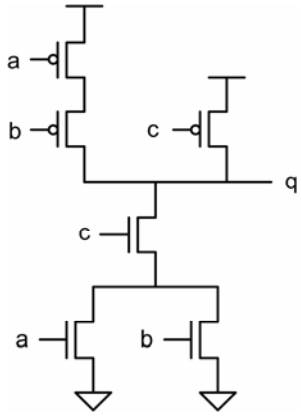
For the reference inverter:
$g_{up\text{-}inv} = g_{down\text{-}inv} = 1$
$p_{up\text{-}inv} = p_{down\text{-}inv} = 1$

Problem 1:
Size each gate to have the same pull up and pull down resistance as the reference inverter. Calculate the logical effort (g_{up}, g_{down}, g_{avg}) and parasitic delay (p_{up}, p_{down}, p_{avg}) for each input of the following gates.

Note: $g_{avg} = ½(g_{up}+g_{down})$
$p_{avg} = ½(p_{up} + p_{down})$

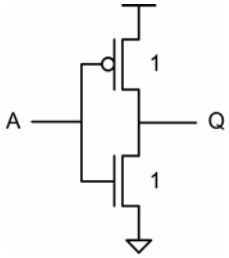


(a)

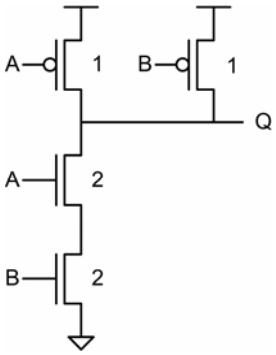


(b)

Problem 2:
Calculate the logical effort (g_{up}, g_{down}, g_{avg}) for each input of the following asymmetric gates.



(a)



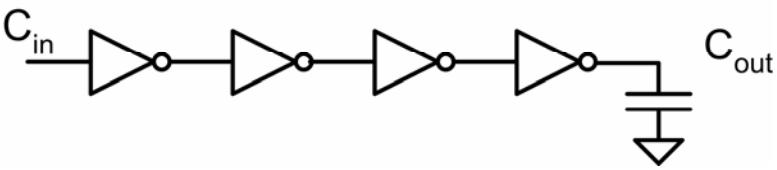
(b)

Problem 3:

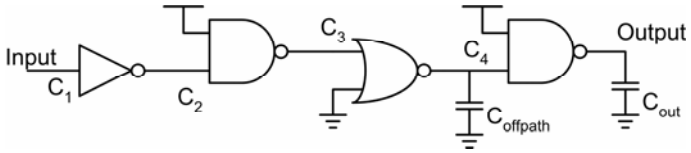
Find the p/n ratio for the inverter which gives the best delay for the following path.

Note: Use g_{avg} and p_{avg} for your calculation

$C_{out} = 256C_{inv}$, $C_{in} = C_{inv}$.



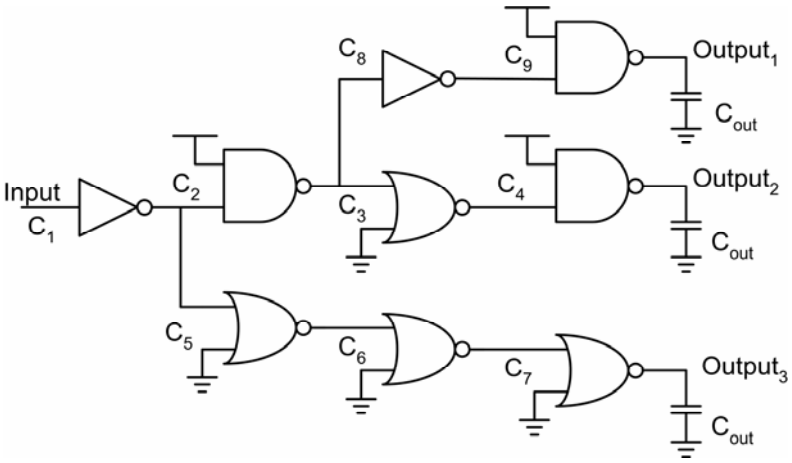
Problem 4:



Given the following path, with $C_{out} = 64C_{inv}$, $C_{in} = C_1 = C_{inv}$. Size the circuit using LE and determine the total delay for (See Horowitz's slides):
a. $C_{offpath} = 0\ C_{inv}$
b. $C_{offpath} = 5\ C_{inv}$
c. $C_{offpath} = 30\ C_{inv}$
d. $C_{offpath} = 120\ C_{inv}$

Comment on each case.

Problem 5:



Assume $C_{out} = 64\ C_{inv}$ and $C_{in} = C_1 = C_{inv}$.

a. Size the following circuit using simple branching. Report the total delay.

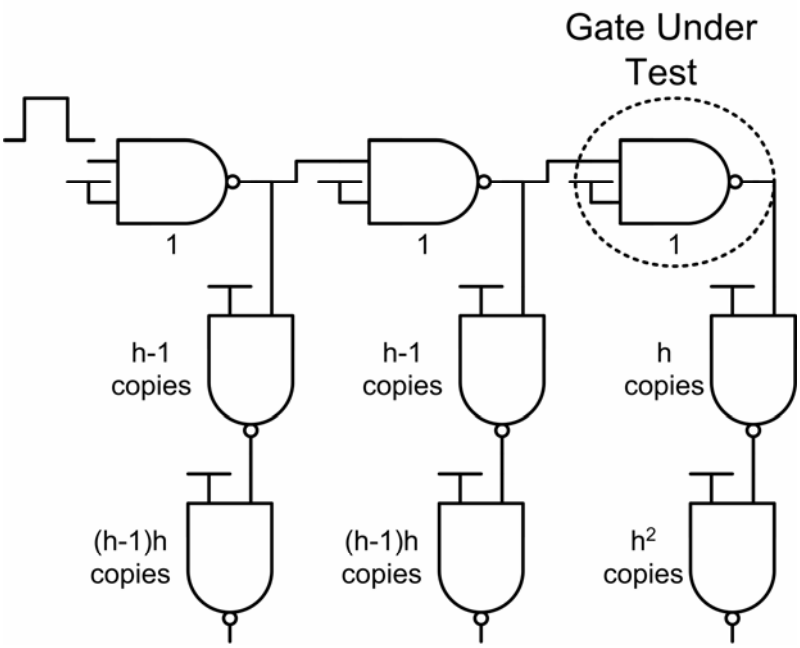
b. Size the circuit using exact branching and report the total delay.

c. Identify the critical path on the schematic. Explain your selection.

d. Comment on what would happen if the load at $Output_1$, $Output_2$ and $Output_3$ differ. Would the critical path change?

Problem 6:

Use the following characterization setup (shown for a nand2).



Note: For Inverter characterization, replace each gate in the setup with Inverters, for NOR2 replace each gate in the setup with NOR2.

(a) Find the p/n ratio for an inverter where $g_{up} = g_{down}$

(b) Characterize an Inverter, NAND2, and NOR2 using HSPICE. Plot the delay vs. h relationship for each gate and input (for h = 2 to 10)

(c) Normalize the delay to τ-inv and plot the delay vs. h relationship (for h = 2 to 10)

(d) Report the *g* and *p* for each input of each gate normalized to the *g* and *p* of the inverter. Do the values for *g* and *p* differ for each input? If yes, explain.

(e) Do the values of g_{up} and g_{down} for *Input a* on the NAND2 differ? *Input b*? If yes, explain.

(f) Do the values obtained for *g* and *p* differ from the hand estimates? If yes, explain.