ISSCC2000 SESSIONS

HIGHLIGHTS

- Microprocessors running at 1GHz
- 12b and 14b ADC without trimming or self-calibration
- Alternative storage technique that uses scanning probe techniques (SPT) and polymethylmethacrylate (PMMA) medium, achieving 200Gb/in^2 (compare with today's HDD with 6Gb/in^2) and comparable speed at lower power levels (IBM)
- 10ns read and write non-volatile memory (IBM)
- Analog filters with supply voltage close to or at 1V
- DRAM's with access time <4ns and usage of pipelining to meet 1GHz operation

Session: High-Frequency Microprocessors

TRENDS

- Clock Frequency boosting (1GHz)
- Cu interconnections instead of Al with up to 7 metal layers
- Emergence of SOI
- Further lowering of VDD and miniaturization (0.18u technology)
- Incorporation of low-Vt devices
- Balancing the clock distribution network to minimize skew
- Integration of L2 cache

1-GHz Alpha Microprocessor, Compaq Computer Corp

- 1GHz frequency
- 1.65V VDD
- 0.18um Leff
- 7 Al metal layers
- 65W dissipation
- Low-Vt utilization
- 6-way out-of-order issue
- 64kB 2-way set-associative I-cache and 64kB 2-way set-associative dual-ported data cache

64b SOI Processor with Cu Interconnects, *IBM Corp.*

- 660MHz frequency
- 1.5V VDD
- 0.18um Leff
- 7 Cu metal layers
- Dynamic circuits usage (convenient in SOI)
- 18W dissipation
- 20% frequency improvement, from device scaling and wiring capacitance reduction
- L2 bus clock modified to maintain L2 bus timing by programmable delay clock macro of 80ps delay increment

A 780-MHz PowerPC Microprocessor with Integrated L2 Cache, *Motorola Inc.*

- 780MHz frequency, 1.5V VDD, 0.18um Leff twin-well process, 6 Cu metal layers
- Dynamic circuits usage with 2-phase clocking
- On-chip 256KB L2 cache with tags and logic for L3 back-side cache (up to 2MB)
- dispatch 3 instructions/cycle, execute 3 simple IU + 1 complex IU + 1 FU + 1 Ld/St unit + 1 branch processing unit + 4 AltiVec execution units
- 32 entry GPR and FPR, 32-entry 128b-wide vector registers (VR) file (for AltiVec units)
- core pipeline with one additional cycle for IF and one for instruction issue
- a 2048-entry branch history table, a 128-entry 4-way set associative branch target I$, a 12-entry instruction buffer, 16 completion buffers, 16 rename registers each for GPR, FPR and VR fiels, a separate 8-way set-associative 32kB I$ and D$

A 1-GHz Single-Issue 64b PowerPC Processor, *IBM Corp.*

- 1GHz frequency, 1.87V VDD, 112W dissipation
- Improved clock generation and distribution
- On-chip 64kB 2-cycle caches and 256KB L2 cache with tags and logic for L3 back-side cache (up to 2MB)
- 64-entry Register file with 6 read ports and 4 write ports
- Single Fixed-Point and Floating-Point units
- 5-cycle branch penalty
- fully pipelined, 4 exec-stage IEEE double-precision FU with fused multiply-add; sum-addressed memory management units,; dynamic PLA-based control; delayed-reset dynamic circuits

A 600-MHz PA-RISC Microprocessor, *Hewlett-Packard Co.*

- 600MHz frequency, 0.25u Ldrawn, 2.0V VDD, 5 metal layers
- Quasi-Least Recently Used (LRU) replacement algorithm to reduce cache miss rate
- Quad-Issue
- 1.2X performance increase in the same process
- 1MB D$, dual ported, 4-way set associative

760-MHz G6 S/390 Microprocessor Exploiting Multiple Vt and Copper Interconnects, *IBM Corp.*

- 760MHz frequency
- 6 Cu metal layers plus additional layer for local interconnects
- 1.9V VDD, 33W dissipation at 637MHz
- 12 user processors plus 2 I/O dedicated processors, 8 L2 cache chips, 4 I/O interface chips, 2 cryptographic processors and clock/service chip on Multi-Chip Module (MCM)
- Selective use of low-Vt devices
- Duplicated Floating-Point Unit, Fixed-Point Unit and Instruction Unit
- 27% frequency improvement with
    - 14% from technology scaling and Cu interconnect
    - 10% from selective use of low Vt devices (90mV lower)
    - 3% on circuit tuning

1-GHz IA-32 Microprocessor Implemented on 0.18um Technology with Aluminum Interconnect, *Intel Corp.*

- 1GHz frequency
- 6 Al layers
- 0.18u CMOS process
- Dual-Vt design
- Attention to wire-engineering
- 0.18um interconnect uses Al and SiOF low-K dielectric

Session: Clock Generation and Distribution

HIGHLIGHTS

- Emphasis on minimization of clock jitter and skew (brought to few tens ps)
- Attention given to growing impact of inductance in VLSI interconnects – model proposed
- Distributed clock generation network (system of distributed PLL's) proposed with cycle-to-cycle jitter less than 10ps
- Technique for generating low-skew, variable duty-cycle multiphase clock (Intel, used in IA-64)

Session: Logic and Systems
HIGHLIGHTS

TREND: Minimizing power consumption while maintaining comparable circuit speed

- SOI technology use in arithmetic circuits
- Flip-flop design for total power dissipation reduction (conditional capture feature)
- Dynamic Voltage Scaling technique - technique for dynamic frequency and supply voltage control with the goal to reduce total power consumption
- Clock-Powered Logic usage in CMOS VLSI Graphics Processor
- Adaptive Power Supply regulation

Session: Next Generation Microprocessors

TRENDS

- Increasing of integration
- Higher level of parallelism
- Low-Power optimization

The Architecture of a 3rd Generation 64b SPARC Microprocessor, Sun Microsystems Inc

- f=800MHz; VDD=1.5V; Pd=60W0.15u process; 7-layer metal; 23M transistors
- 4-issue superscalar processor
- 64KB 4-way associative data cache, 32KB 4-way associative instruction cache, 2KB 4-way associative data prefetch cache
- Clock rate is prioritized over IPC improvements (1.5X the clock rate compared to previous design; 1.15X for both IPC and compiler)
- 8 static gates per pipeline stage
- 14 pipeline stages
- Capable to launch up to 6 instruction at a time
    - 2 integer operations
    - 2 FP operations
    - 1 load/store
    - 1 control transfer instruction

The Architecture of a 3rd Generation 64b SPARC Microprocessor, Sun Microsystems Inc (continued)

- Branch prediction scheme uses *gshare*
- Branch resolution in E-stage (early in the pipeline)
- Introduction of mispredict queue integrated with 20-entry instruction queue
- 8 integer register windows – WRF (32 registers, 7 read ports, 3 write ports), ARF (160 registers, 3 write ports)
- Overall skew <80ps, jitter<62ps

450MHz 64b RISC Processor Using Multiple Threshold Voltage, Hitachi Ltd.

- VDD=1.8V; 0.25u process; 7-layer metal; 28.3M transistors
- Multiple-threshold-voltage design applied to clock distribution drivers, register files and both static and dynamic logic
- Precise clock skew control and jitter minimization
- Out-of-order execution
- 4 FP operations, 2 quad word loads per cycle
- Critical paths:
  - Register renaming
  - Branch control
  - TLB hit check

1GIPS 1W Multiprocessor with Architecture Support for Multiple Control Flow Execution NEC Corp.

- f=125MHz; VDD=1.3V; Pd=1W
- Tightly-coupled multiprocessor architecture
- Targeted to high-performance low-power embedded systems
- Architecture based on multiple control flow execution model, *fork-once parallel execution* (FOPE)
- 4 processing elements – in-order two-way issue superscalars with two ALU pipelines
- Support for register sharing realized by utilization of local Register Map Tables (RMT)
- 256-word 16-read/8-write port register file
- Store-Reservation Buffers (SRB) provide data caching in multiprocessing environment
- Architectural power reduction achieved by Power Management Unit (PMU)

1000 MIPS/W Microprocessor Using Speed Adaptive Threshold Voltage CMOS with Forward Bias, Hitachi Ltd.

- Substrate bias controlled to compensate for fabrication fluctuations, supply voltage variations and temperature variation – Speed-Adaptive Threshold Voltage CMOS (SA-Vt CMOS)
- Pd=320-380mW with VDD=1.5V-1.8V and f=220MHz
- 4.3M transistors, 0.2u process, standby current 30uA
- 2-way superscalar architecture
- 8KB I-cache, 16KB data cache

The First-Generation IA-64 Microprocessor, Intel Corp.

- 0.18u CMOS process; 6 metal layers; 25.4M transistors
- Uses *speculation*
  - Control speculation (execution of operation before the condition governing its execution)
  - Data speculation (execution of memory load prior to store that might change its value)
- Uses *predication* (conditional execution of instruction that removes need for branching)
- 10 pipeline stages
- 128 integer and FP registers, 64 one-bit predication registers and 8 branch registers
- On-chip L1 and L2 cache

The First-Generation IA-64 Microprocessor, Intel Corp. (continued)

- 11 execution units
  - 4 integer units
  - 2 FP units – up to 6Gflops; single, double and double-extended (80b) data types
  - 3 branch units
  - 2 load/store units
- binary compatibility with previous design (IA-32)
- Use of skew-tolerant domino logic
- Differential clock