18-747 Lecture 24: Quiz 2 and Course Review

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November 28, 2001

Reading Assignments: Review past reading assignments

Announcements: Quiz on Monday 12/3
HW4 due today
Project 3 due Friday 12/7 (for bonus) or Friday 12/10
Guest Lecture: Energy aware computing: Prospect for the present and future by Diana Marculescu

Handouts: *HW4 Solution, Practice Exam2 Solutions, Grade HW3*

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Project 3 Wrap-up

- Early reports for bonus points are due Friday 12/7
- Presentation Slides for bonus due Friday 12/7
  - Approximately 25 minutes + 5 minutes Q&A
  - A PowerPoint or Framemaker presentation (10 slides maximum) must be emailed to (akrol@ece.cmu.edu) by 11:59PM, 12/7
- Selected groups make presentations on Mon 12/10
- All final reports are due on Mon 12/10
- What should be discussed in the project report?
  - Tell us what you did and why you choose to do it that way
  - Tell us something new and original
    - What problems did you encounter?
    - What problems were you able to solve? (or why not)
    - Did you learn anything interesting in the process?

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Format of the Quiz

- Same as described on L13-2, except,
- Cover all lectures (upto and including Lecture 23), projects, HWs, assigned readings (textbooks and papers)
- Emphasis on materials not covered by the 1st Quiz
- Emphasis on materials covered during lecture
- How to review for the first half of the course?
  - Start after you are comfortable with the 2nd half
  - Start with the emphasized materials
    - Exam 1 questions
    - Problem set questions
    - Selected Slides
  - Materials related to and required by the 2nd half of the course

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What was the course all about?

Answer: how to run programs faster

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1st Half

What if the ISA and the binaries have been chosen for you?

1. Make use of available ILP
   - Pipelining ⇒ reduce cycle time
   - Superscalar execution ⇒ increase IPC
2. Creating more ILP
   - Renaming ⇒ eliminate false dependence
   - Out-of-order execution ⇒ find ILP across RAW data dependence
   - Branch Prediction ⇒ find ILP across control flow
   - Value Prediction ⇒ optimistically cross data flow
3. Build efficient structures to support high ILP
   - Memory Hierarchies ⇒ increased memory bandwidth
   - Prefetching ⇒ increased data bandwidth
   - Trace Caching ⇒ increased instruction bandwidth

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State of the Art

	Alpha 21264	AMD Athlon MP	Intel P4	MIPS R14000	IBM Power3 -II	HP PA-8600	SUN Ultra-III	Intel Itanium
Clock (GHz)	1.001	1.2	1.8	0.5	0.450	0.552	0.9	0.8
Issue Rate	4	3 (x86)	3 (rop)	4	4	4	4	6
# Fxn Units	9	9	7		8			
Pipe. int/fp	7/9	9/11	22/24	6	7/8	7/9	14//15	10
Inst in Flight	80	72 (rop)	126 (rop)	48	32	56	in-order	in-order
Rename Reg	48+41	36+36	128	32+32	16+24	56	in-order	328
Mem GB/sec	2.66	2.1	3.2	0.539	1.6	1.54	4.8	2.1
Process µm/M	0.18/6	0.18/6	0.18/6	0.25/4	0.22/6	0.25/2	0.15/7	0.18/6
Trans (10^6)	15.4	37.5	42	7.2	23	130	29	25
Power (W)	95	66	67	30	36	60	75	130
SPECint 2000	561	495	599	397	286	417	439	314
SPECfp 2000	585	433	615	362	356	400	369	703

Microprocessor Report, August 2001

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2nd Half

What else is there? Or what if anything goes . . . . . .

1. Back to fundamentals (compiler code generation)
   - generate optimized code with more ILP to begin with
   - generate optimized code that are amenable to ILP structures
   - use profiling to guide code generation
2. Alternative architectures and paradigms
   - VLIW
   - EPIC
   - Virtualized architectures (dynamic binary translation)
3. Exploit other forms of parallelisms
   - Multi-threaded processors
   - Symmetric Multiprocessors

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Reality Check:

What else might be useful to know?

- Computer Architecture, i.e. everything outside of the processor core
  - Memory subsystem, I/O Subsystem, Storage, Busses . . . .
  - Multiprocessors, Parallel Processing
  - Application specific and embedded processor design
- Computer Science, i.e. interaction with software
  - What are the needs of compiler, OS and applications?
- Electrical Engineering
  - Circuit design, semiconductor technologies, manufacturability
  - Low-power, reliability
  - Verification
- Real-world problems that companies must worry about
  - ISA design and binary compatibility
  - Managing design complexity, time and cost
  - Economics (competition, alliances, product line planning. . .)

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More Information

- CPU Information Center
  http://bwrc.eecs.berkeley.edu/CIC
- *Microprocessor Report*
  http://www.mdronline.com
  Engineering & Science Library
- 18-742 Parallel Computer Architecture (Spring, 02)
- 18-744 Hardware Systems Engineering (Spring, 02)
- Lot's of research opportunities at CMU!

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