UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180B **DIGITAL SYSTEMS II** **Fall 1999**

LAB 1: USING RAM IN THE ALTERA FLEX10K

Overview

This lab will cover several advanced topics related to using the Altera Flex10K programmable logic device (PLD). In particular, it will focus on using internal RAM within a Flex10K PLD.

Preparation

You must have a solid understanding of the two Altera tutorials used in EEC180A. (These tutorials have been posted on the EEC180B course web page.) In addition, you should thoroughly read this lab and the data sheets that are referenced in this write-up. Also, answer the following questions:

- How many EABs are required to implement a 256x16 RAM? Justify your answer.
- How many EABs are in an EPF10K20?

Background

As you know from the 180A tutorials, Altera devices do not have internal tri-state buses. Consequently, logic inside an Altera device cannot communicate via bi-directional lines. However, MAX+PLUS II can often use multiplexers to emulate tri-state buses.

An interesting example of bi-directional bus emulation occurs with the Altera lpm_ram_io Megafunction. This part is described as a “Parameterized RAM with a Single I/O Port”. In the description of the ports, the dio[] port is described as a “bi-directional data port for the memory”. In reality, however, the dio[] port of the lpm_ram_io function is not implemented using bi-directional signals. The lpm_ram_io function is implemented using Embedded Array Blocks (EABs) in Flex10K devices or level-sensitive latches in other device families. The Altera Flex10K datasheets show that the RAM block in the EAB has separate “Data In” and “Data Out” ports rather than a bi-directional data port. Thus, although the lpm_ram_io component can be used as if it had a bi-directional data port, it actually has separate ports for data input and data output.

The Flex10K devices do have tri-state buffers in the I/O elements. Thus, if the dio[] port of the lpm_ram_io component is connected to BIDIR pins, the external signals which connect to these pins can be bi-directional. However, inside the Altera device these signals are not bi-directional, but connect to separate input and output lines.

The lpm_ram_io component can be used to implement either synchronous RAM or asynchronous RAM. It can be quite difficult and intimidating to use the lpm_ram_io or other RAM Megafunctions because of the wide range of configuration options. In this lab, you will investigate various ways of configuring the lpm_ram_io function and verifying that you understand its operation.

In order to understand the operation of the EAB and the RAM Megafunctions, you should study the following references:

- Help on LPM_RAM_IO – accessible through MAX+PLUSII by selecting the lpm_ram_io Megafunction from the mega_lpm library and clicking on the Help button.

- The Flex10K data sheet – available on-line at http://www.altera.com/document/ds/dsf10k.pdf. There are several sections that focus on the operation of the EAB. See p. 9-12, 58-59, 62-63, and 66-67. The timing waveforms for EAB asynchronous read and write operations and EAB synchronous read and write operations are especially important.

- The Altera web site also has a few examples of using tri-state components to emulate bi-directional buses inside an Altera device. For example, the article "Graphic Editor: Tri-State Buses Connected to a Bidirectional Bus" (http://www.altera.com/html/atlas/examples/ged/g_tri_bb.html) shows a useful example. You can also search Altera's web site for "tri-states" and find many other example circuits.

LAB SPECIFICATIONS

In this lab, you will simulate four different configurations of the lpm_ram_io Megafunction: 1) Asynchronous RAM connected to BIDIR pins, 2) Asynchronous RAM connected to internal logic, 3) Synchronous RAM connected to BIDIR pins, and 4) Synchronous RAM connected to internal logic. The goal of the lab is for you to understand how the EAB functions in asynchronous and synchronous operation.

The two circuits with the lpm_ram_io component connected to the Altera device pins are shown in the simple block diagram in Figure 1.

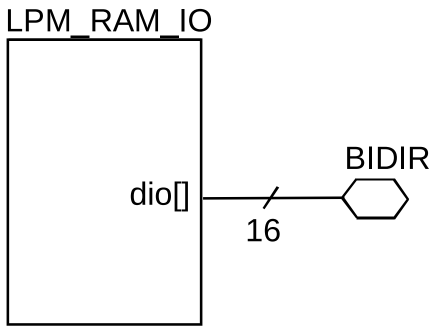

Figure 1: RAM connected to bi-directional pins

The two circuits with the lpm_ram_io component connected to internal logic are shown in the simple block diagram in Figure 2.

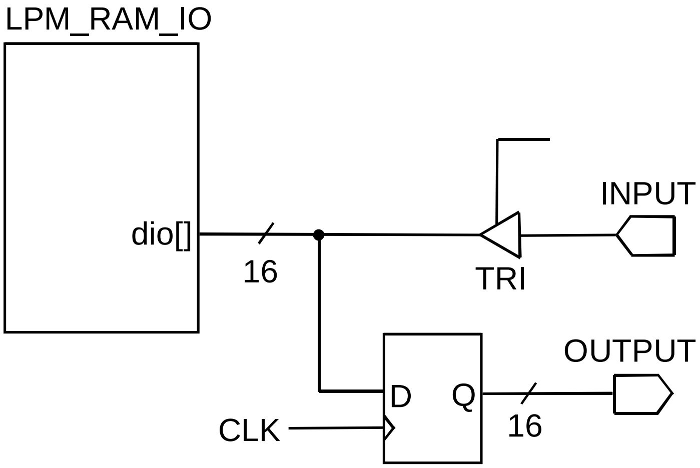

Figure 2: RAM connected to internal logic

For each of the four cases, the RAM should be 256 words by 16 bits. In each case, you should perform the following steps:

1. Draw a schematic using the Altera Graphic Editor.
2. Configure the lpm_ram_io Megafunction for asynchronous or synchronous operation. You will need to understand the various configuration parameters for the lpm_ram_io.
3. Compile your circuit for timing simulation.
4. Develop a simulation test case that writes unique values to at least five different RAM locations and later reads them back.
5. Run the timing simulation and verify that the RAM functions correctly.

Lab Report Requirements

You will demonstrate your simulations to your TA. Your TA will also ask you to explain the operation of the RAM component. Your TA should sign a verification sheet when he has verified your lab. For the lab report, turn in the following for each of the four circuits:

1. Schematic
2. Simulation Waveforms
3. An explanation of the simulation waveforms. Explain what causes each write to take place when it does. Also explain how the read operations work.