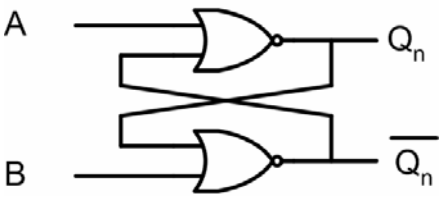
PROBLEM 1

(1) Complete the excitation table for the following storage element:



Q_n	Q_{n+1}	A	B
0	0		
0	1		
1	0		
1	1		

SOLUTION

Q_n	Q_{n+1}	A	B
0	0	-	0
0	1	0	1
1	0	1	0
1	1	0	-

(2) Write the characteristic equation for this storage element.

Q_{n+1} =

SOLUTION

$Q_{n+1} = B + A'Q_n$

PROBLEM 2

The following characteristic table describes a storage element A-B

A	B	Q_{n+1}	Operation
0	0	Q_n	Hold
0	1	0	Reset
1	0	Q_n	Hold
1	1	$\overline{Q_n}$	Toggle

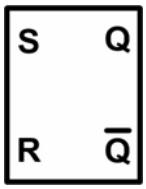
(1) Write the characteristic equation for the storage element A-B.

Q_{n+1} =

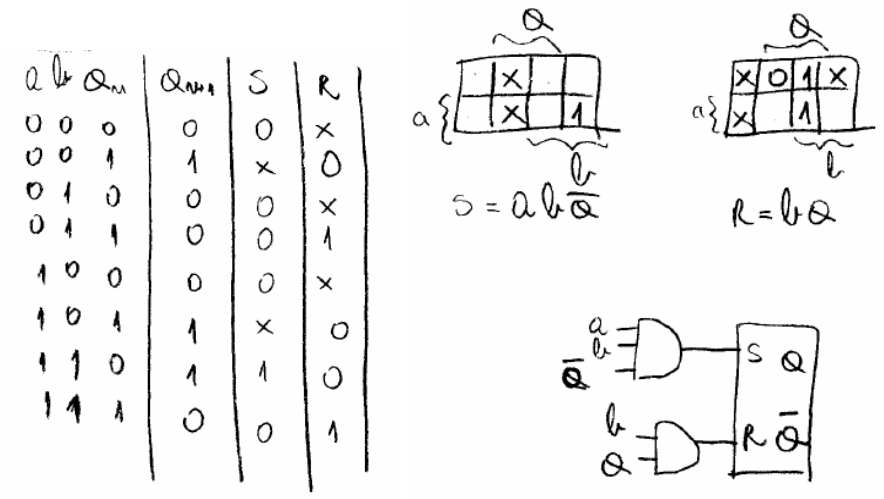
SOLUTION

$$Q_{n+1} = a\,b\,\overline{Q}_n + \overline{b}\,Q_n$$

(2) Implement the A-B storage element using additional gates and an S-R Latch. Show your schematic diagram and derivation process.



SOLUTION



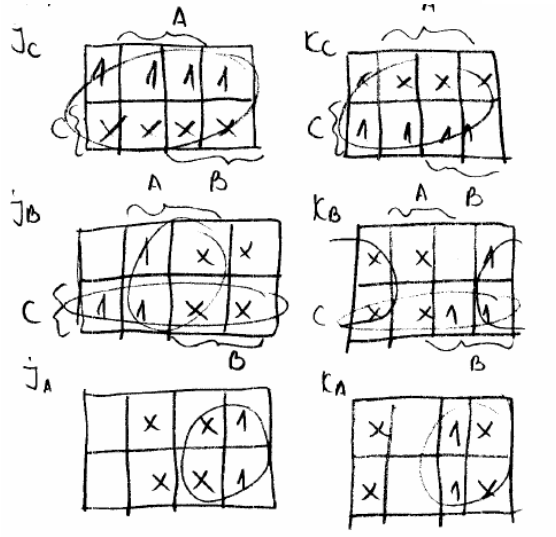
PROBLEM 3

Design a 3-bit counter which counts in the sequence:
010, 101, 011, 110, 001, 111, 000, 100, 010, …

Implement the 3-bit counter using J-K Flip-Flops. Draw the state transition table, appropriate K-maps and derive the J-K flip-flop input equations

SOLUTION

CBA	$C^+B^+A^+$	$J_C K_C$	$J_B K_B$	$J_A K_A$
000	100	1 x	0 x	0 x
001	111	1 x	1 x	x 0
010	101	1 x	x 1	1 x
011	110	1 x	x 0	x 1
100	010	x 1	1 x	0 x
101	011	x 1	1 x	x 0
110	001	x 1	x 1	1 x
111	000	x 1	x 1	x 1



$J_C = 1 \quad K_C = 1$

$J_B = C + A \quad , K_B = \bar{A} + C$

$J_A = B \quad , K_A = B$

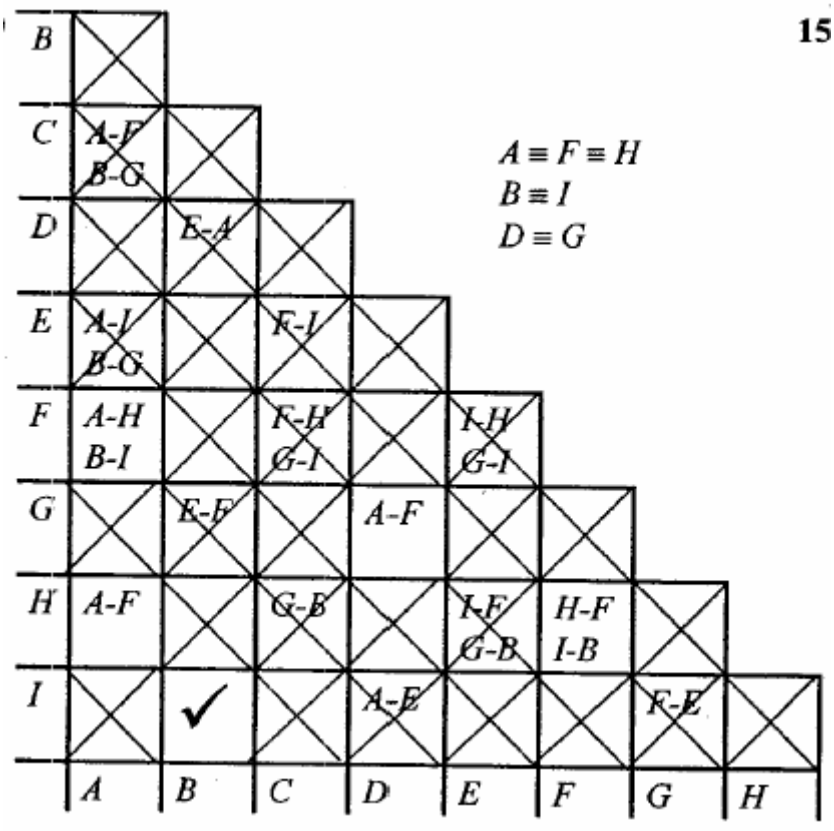
PROBLEM 4

Reduce the following state table to a minimum number of states.

Present State S_n	Next State S_{n+1} X=0	X=1	Output Z
a	a	b	1
b	c	e	0
c	f	g	1
d	c	a	0
e	i	g	1
f	h	i	1
g	c	f	0
h	f	b	1
i	c	e	0

(1) Write the resulting state table. Determine the equivalent states – show them.

SOLUTION



[extra space for Problem 4]

(2) Draw the resulting state diagram with all states, transitions and outputs.

SOLUTION

State	Next State $X=0$	Next State $X=1$	X
A	A	B	1
B	C	E	0
C	A	D	1
D	C	A	0
E	B	D	1

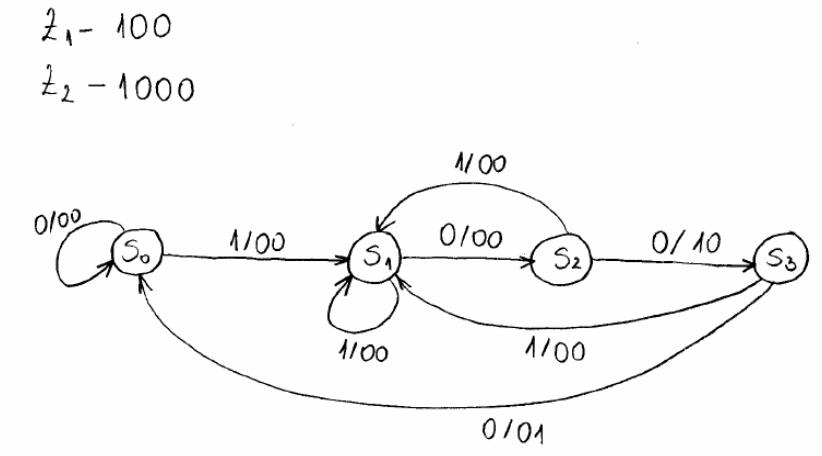
PROBLEM 5

Design a Mealy sequential circuit which has one input (X) and two outputs (Z_1 and Z_2) which meets the following specifications:

1) Output Z_1 is 1 when the sequence 100 is detected, otherwise it is 0.
2) Output Z_2 is 1 when the sequence 1000 is detected, otherwise it is 0.

(1) Draw the state diagram

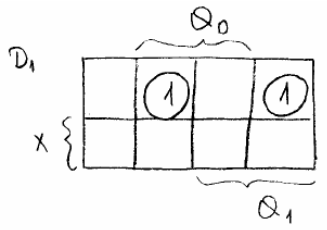
SOLUTION



(2) Derive the input equations for an implementation using D Flip Flops.

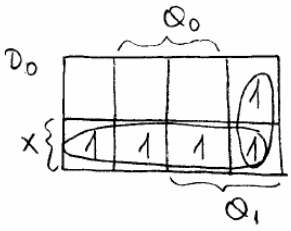
SOLUTION

X	Q_1	Q_0	Q_1^+	Q_0^+	Z_1	Z_2	D_1	D_0
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0
0	1	0	1	1	1	0	1	1
0	1	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1
1	0	1	0	1	0	0	0	1
1	1	0	0	1	0	0	0	1
1	1	1	0	1	0	0	0	1

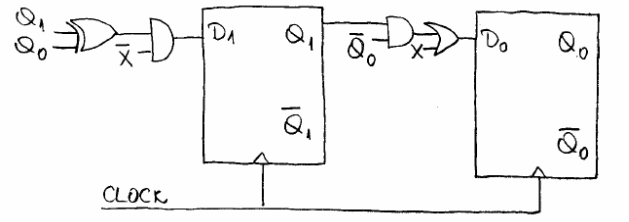


$D_1 = \bar{X}\,\bar{Q}_1 Q_0 + \bar{X}\,Q_1 \bar{Q}_0 =$

$= \bar{X}\,(Q_1 \oplus Q_0)$



$D_2 = X + Q_1 \bar{Q}_0$



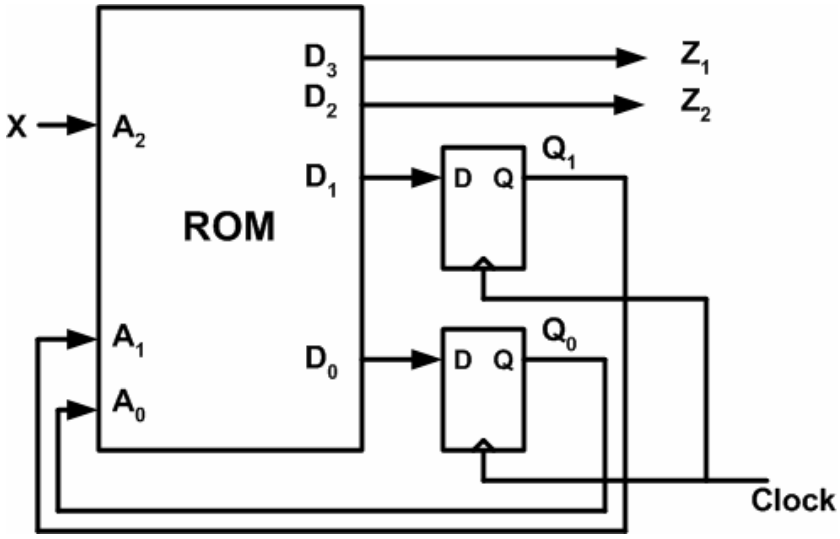
(3) Determine the output equations for Z_1 and Z_2.

Z_1 =
Z_2 =

SOLUTION

$Z_1 = X'Q_1Q_2'$
$Z_2 = X'Q_1Q_2$

(4) Implement the FSM using ROM and D-Latch Registers



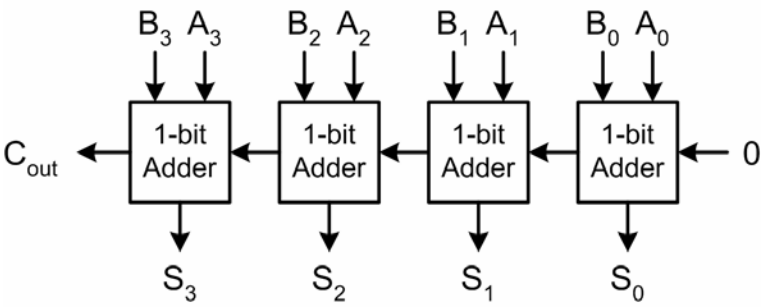
Address $A_2 A_1 A_0$	Content of ROM $D_3 D_2 D_1 D_0$
000	
001	
010	
011	
100	
101	
110	
111	

SOLUTION

Address $A_2 A_1 A_0$	Content of ROM $D_3 D_2 D_1 D_0$
000	0 0 0 0
001	0 0 1 0
010	1 0 1 1
011	0 1 0 0
100	0 0 0 1
101	0 0 0 1
110	0 0 0 1
111	0 0 0 1
XQ_1Q_0	$Z_1Z_2D_1D_0$

PROBLEM 6

Analyze the following 2's complement 4-bit Ripple Carry Adder

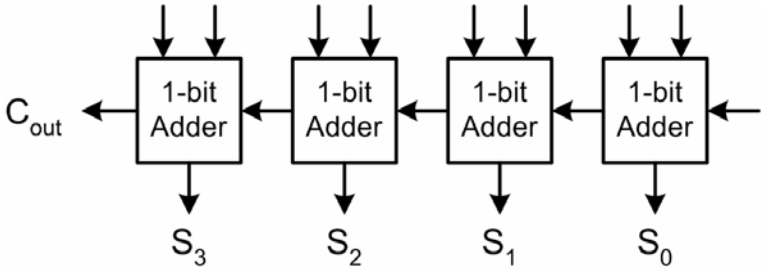


(1) Draw the critical path on the adder.

(2) Show a sequence of input vectors that creates this critical path.

SOLUTION
Vector1 [A,B] = [0000 , 0000]
Vector2 [A,B] = [1111 , 0001]

(3) Using only XOR gates, modify the four-bit ripple carry adder below to perform 2's complement addition when a control signal X = 1, and 2's complement subtraction (A-B) when X = 0.



(4) Draw the critical path.
SOLUTION