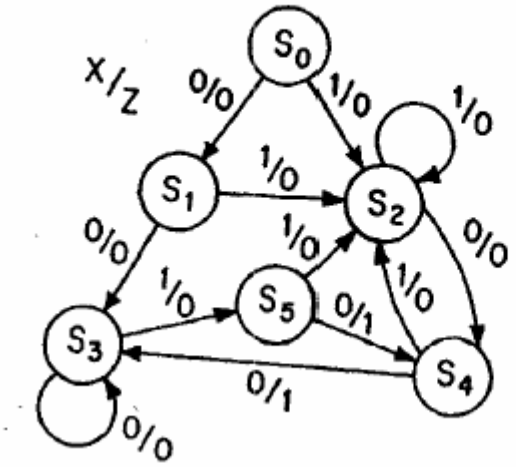
EEC180A DIGITAL SYSTEMS I Winter, 2006.

Solutions for Homework # 9

16.1



	X = 0	1	X = 0	1
S_0	S_1	S_2	0	0
S_1	S_3	S_2	0	0
S_2	S_4	S_2	0	0
S_3	S_3	S_5	0	0
S_4	S_3	S_2	1	0
S_5	S_4	S_2	1	0

Assignment by guidelines:

I. (1, 3, 4) (2, 5) (0, 1, 2, 4, 5)

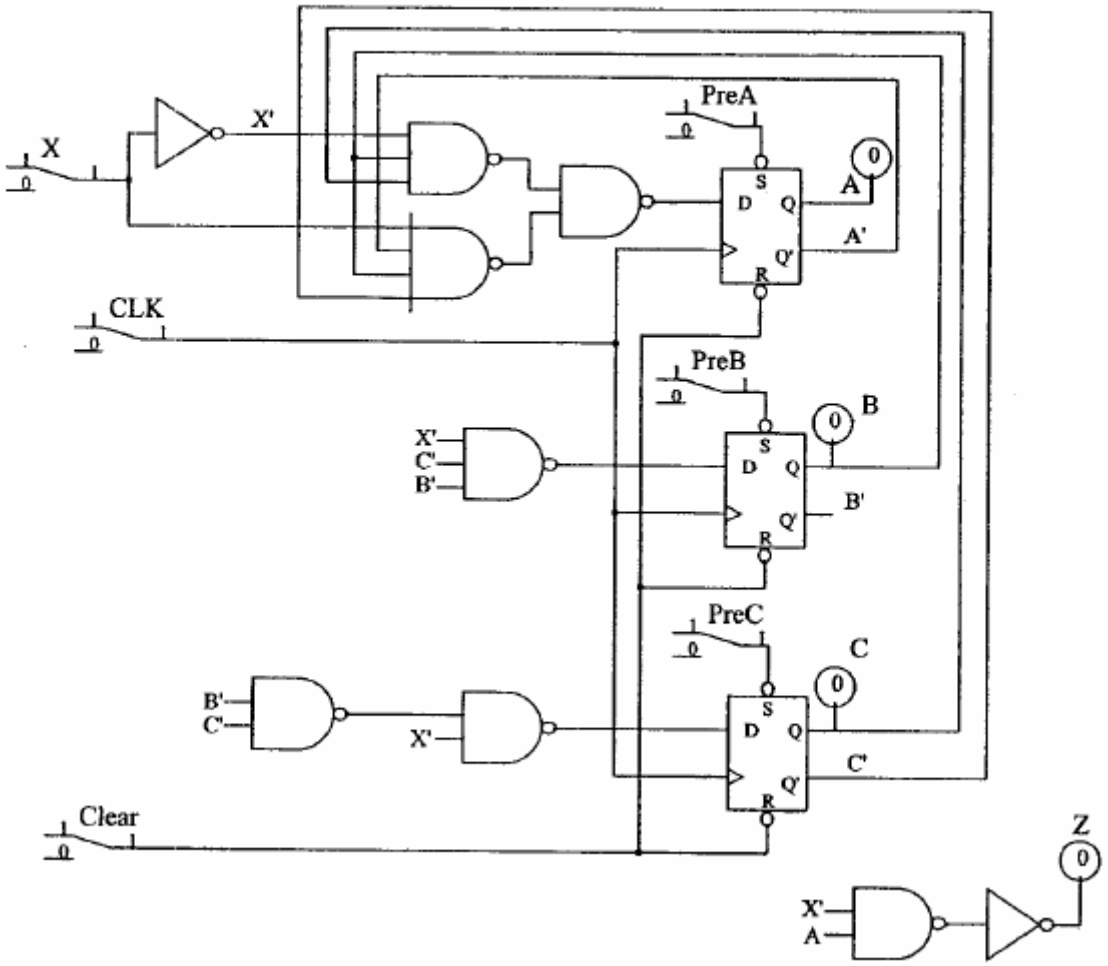
II. (1, 2) $(2, 3)_2$ $(2, 4)_2$ (3, 5)

III. (0, 1, 2, 3) (4, 5)

B C \ A	0	1
00	S_0	
01	S_1	
11	S_2	S_5
10	S_3	S_4

From Q^+ maps:

$A^+ = X'BC + XA'BC'$ $B^+ = X + C + B$ $C^+ = B'C' + X$ $Z = X'A$



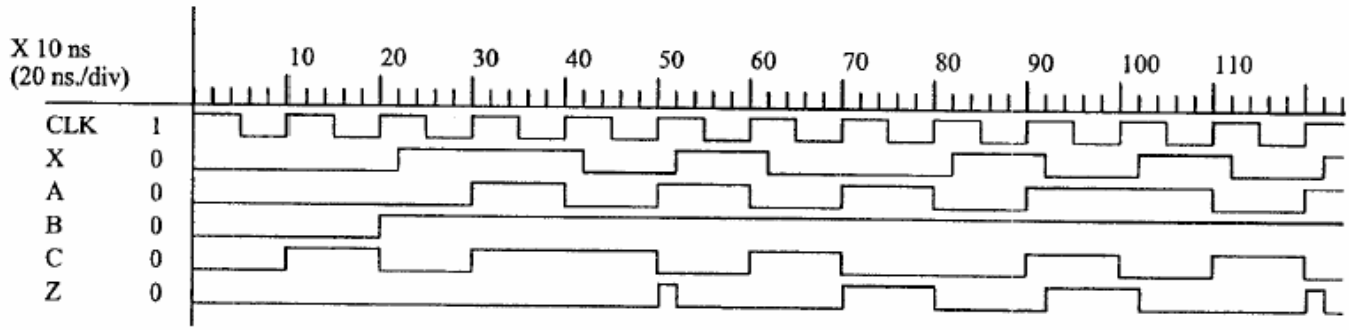
Test sequences:

a) X = 00110100101010001001001O

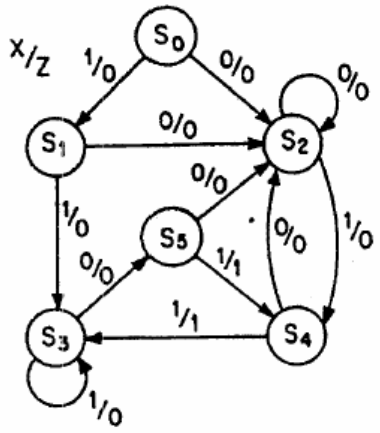
Z = 000000010100001001101101

b) X = 11001100101010010101001O

Z = 000100010100001010000101



16.2



	X = 0	1	X = 0	1
S_0	S_2	S_1	0	0
S_1	S_2	S_3	0	0
S_2	S_2	S_4	0	0
S_3	S_5	S_3	0	0
S_4	S_2	S_3	0	1
S_5	S_2	S_4	0	1

Guidelines and state assignments are the same as for16.1

Flip-flop and output equations and logic circuit are the same as 16.1, except interchange X and X' throughout

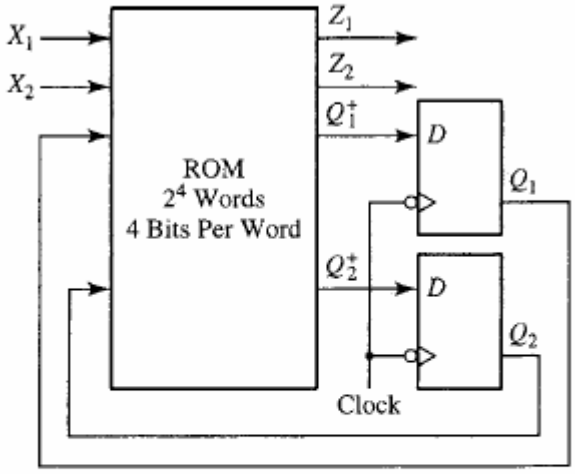
Test sequences a) X = 110010110101011101101101

Z = 000000010100001001101101

b) X = 001100110101011010101101

Z = 000100010100001010000101

16.15



X_1	X_2	Q_1	Q_2	Q_1^+	Q_2^+	Z_1	Z_2
0	0	0	0	1	1	0	0
0	0	0	1	0	0	1	0
0	0	1	0	1	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	1	0	1	0
0	1	0	1	0	1	1	0
0	1	1	0	0	0	1	0
0	1	1	1	1	0	0	0
1	0	0	0	0	1	1	1
1	0	0	1	1	0	1	1
1	0	1	0	0	1	1	1
1	0	1	1	0	1	0	1
1	1	0	0	0	0	0	1
1	1	0	1	1	1	1	1
1	1	1	0	0	1	0	1
1	1	1	1	0	0	0	1

16.16 (a) Same as Figure 16-10 with ROM replaced by PLA.
(b)

X	A	B	C	Z	D_A	D_B	D_C
0	-	-	-	0	1	0	0
0	-	-	0	0	0	1	0
-	0	-	1	0	0	1	0
-	0	1	-	0	0	1	0
-	1	-	-	0	0	0	1
1	-	0	-	0	0	0	1
0	1	0	1	1	0	0	0
1	0	1	0	1	0	0	0

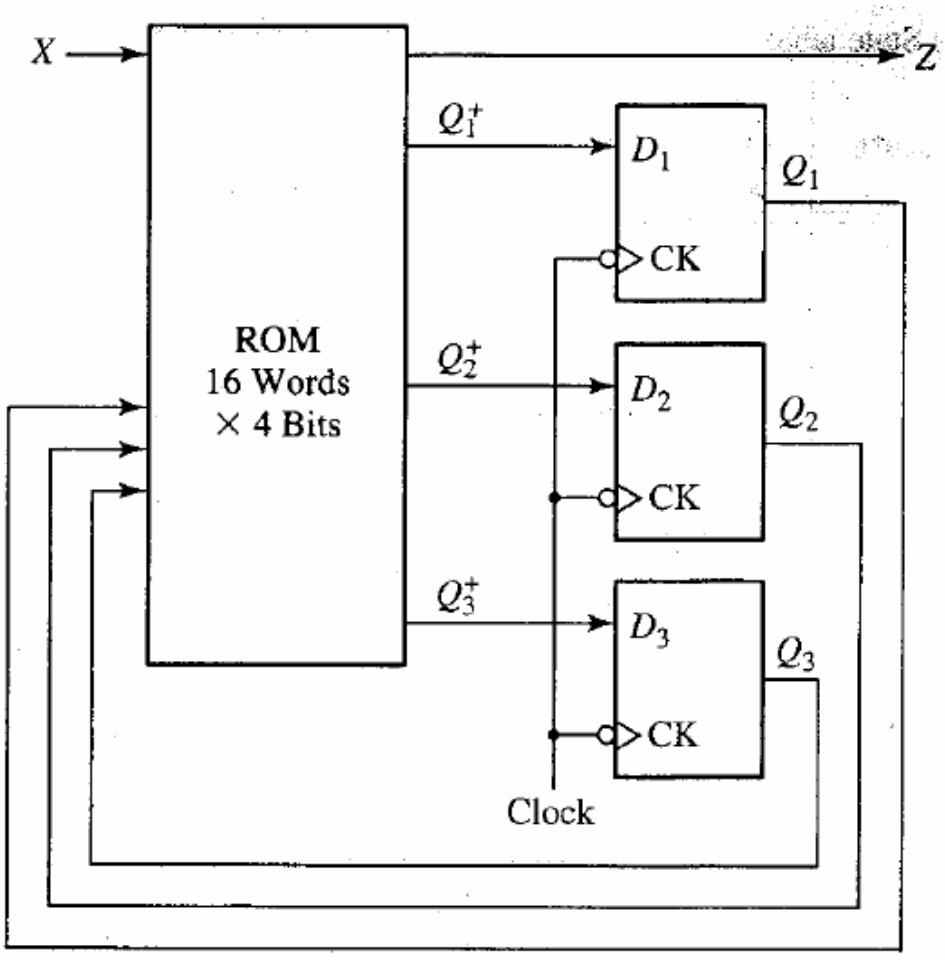


FIGURE 16-10
Realization of Table 16.6(a) Using a ROM