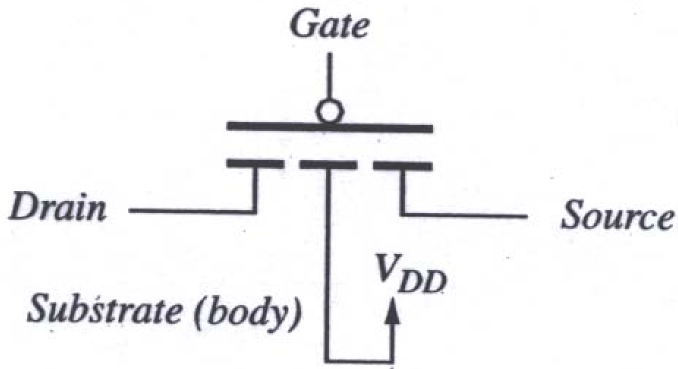
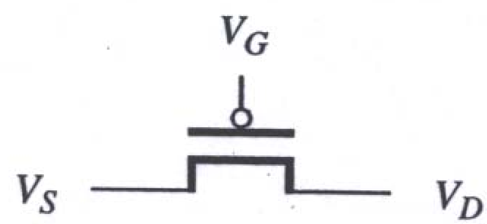
(a) A switch with the opposite behavior of Figure 3.2(*a*)



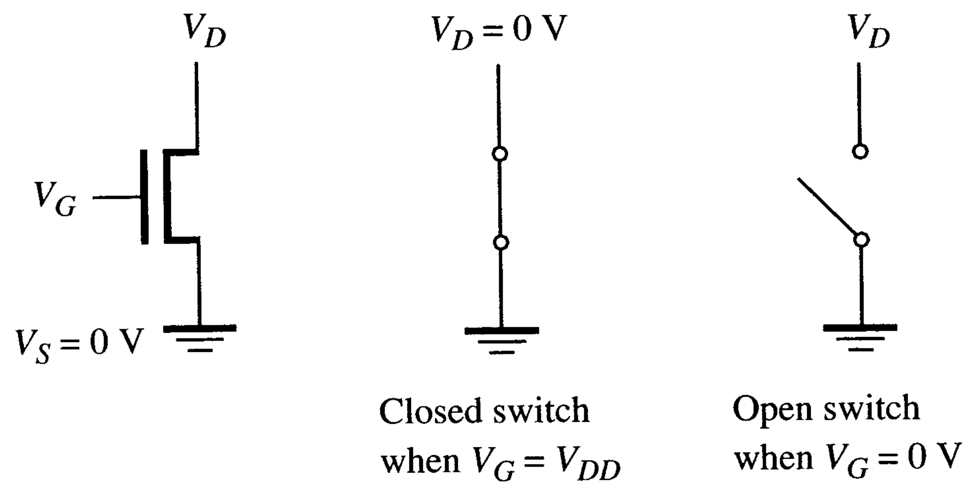
(b) PMOS transistor



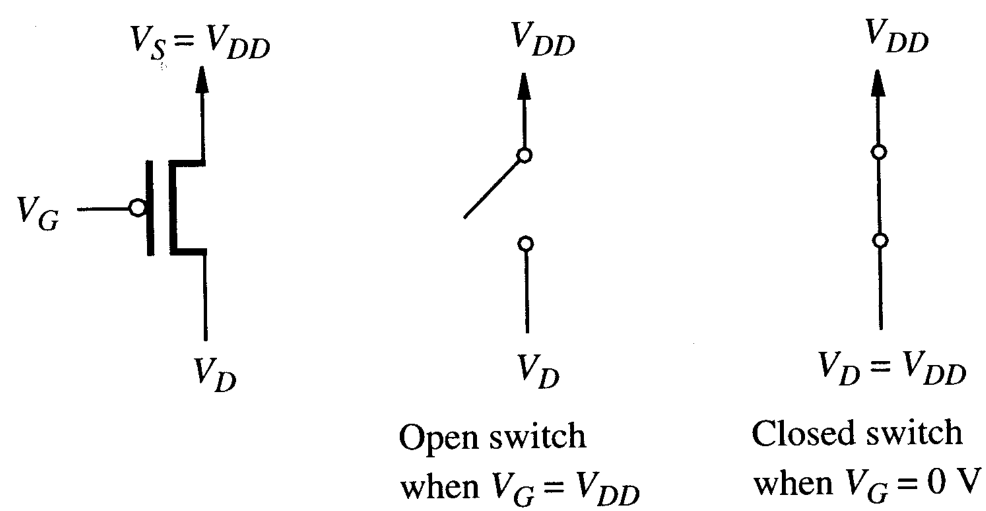
(c) Simplified symbol for an PMOS transistor

Figure 3.3 PMOS transistor as a switch.

McGraw, Hamacher, Zacky

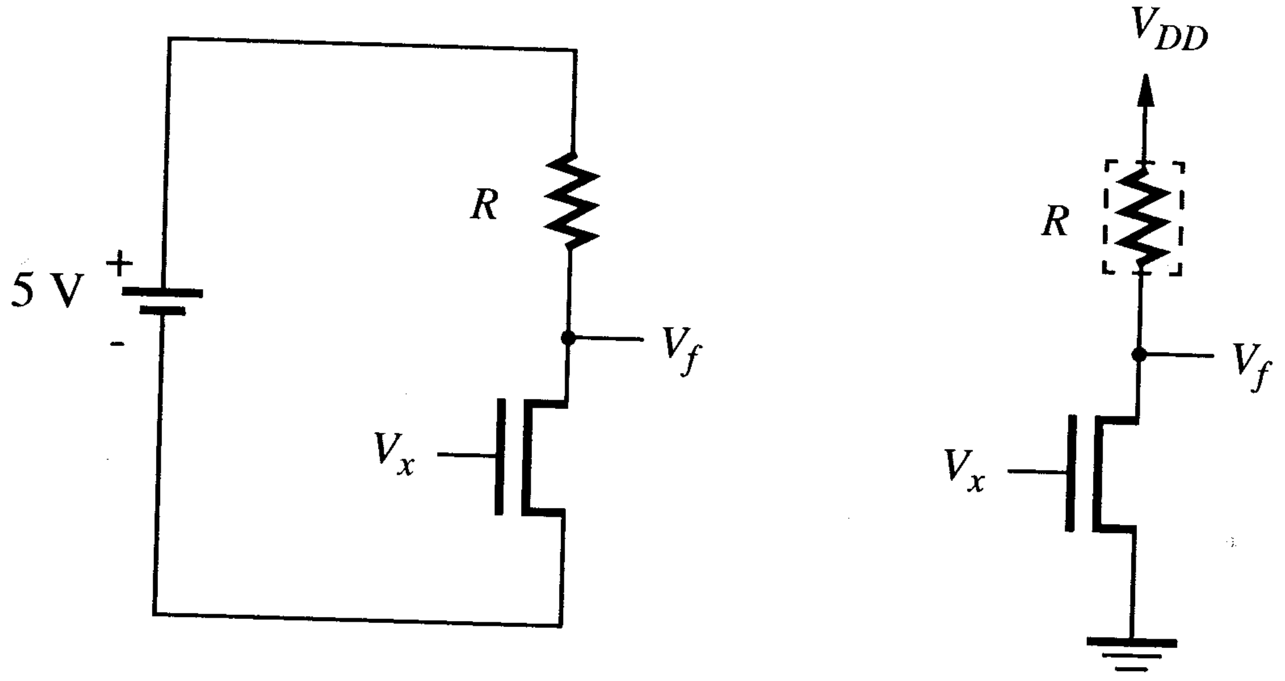


(a) NMOS transistor



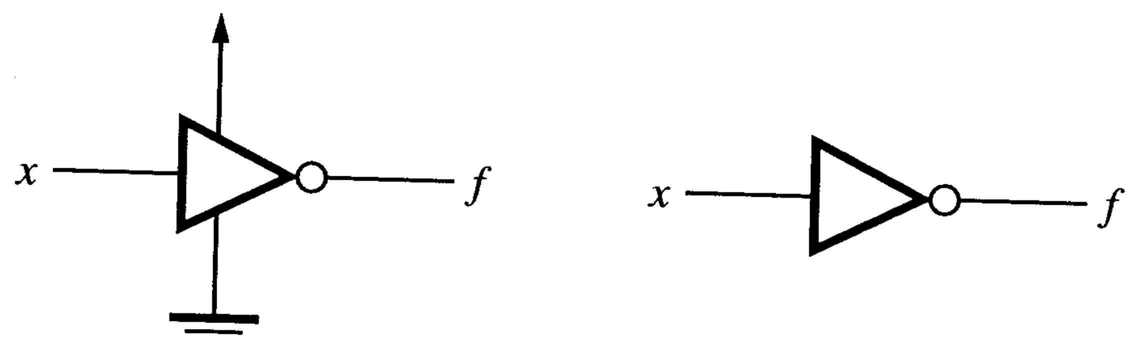
(b) PMOS transistor

Figure 3.4 NMOS and PMOS transistors in logic circuits.



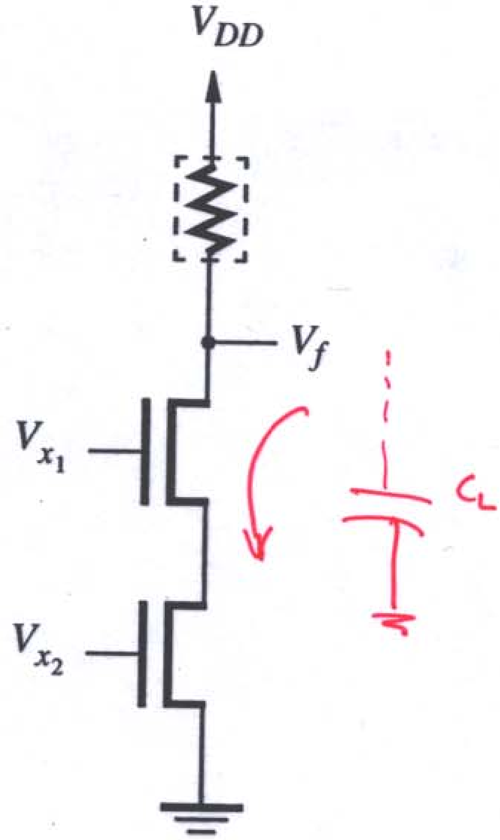
(a) Circuit diagram

(b) Simplified circuit diagram



(c) Graphical symbols

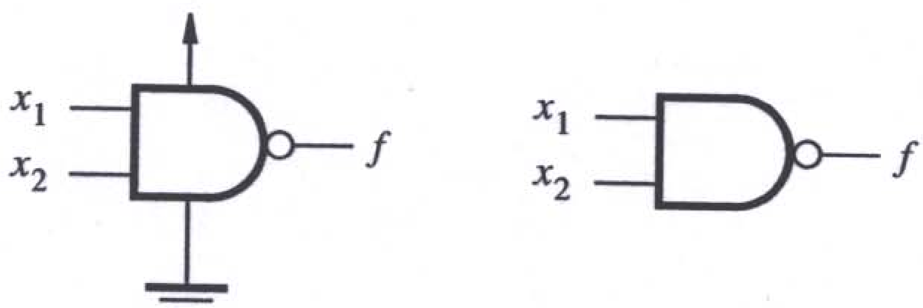
Figure 3.5 A NOT gate built using NMOS technology.



(a) Circuit

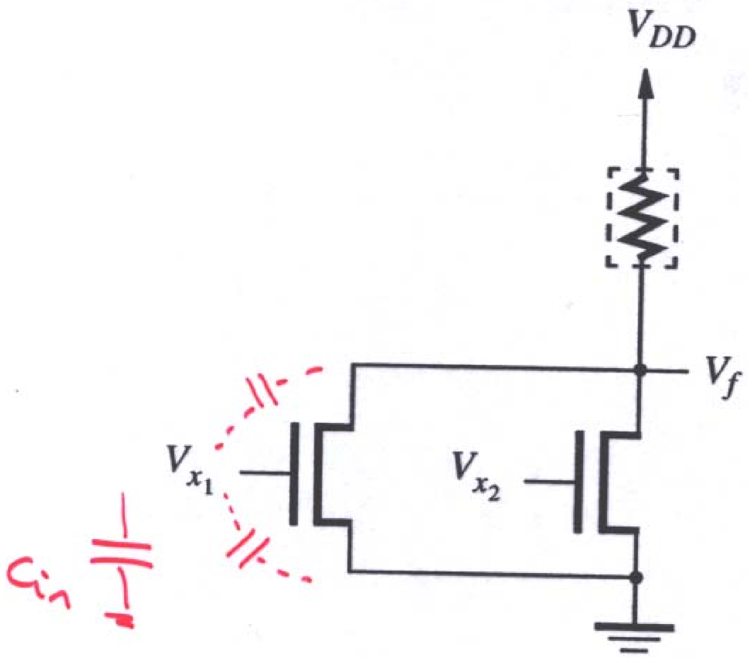
x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(b) Truth table



(c) Graphical symbols

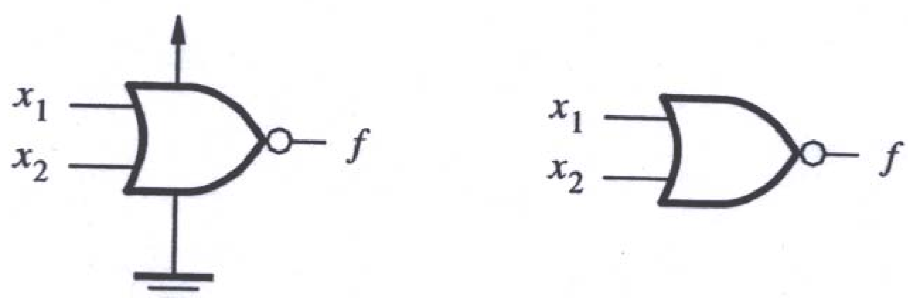
Figure 3.6 NMOS realization of a NAND gate.



(a) Circuit

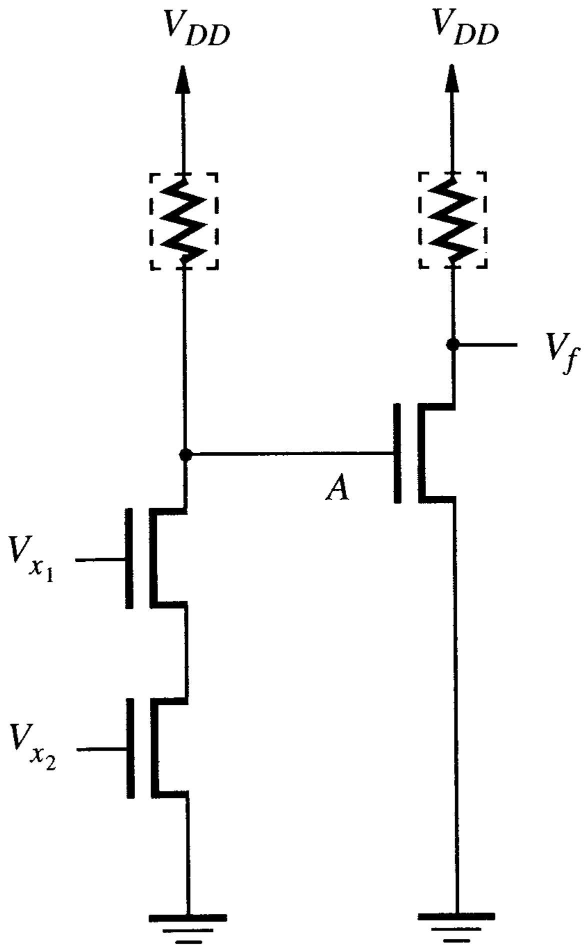
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table



(c) Graphical symbols

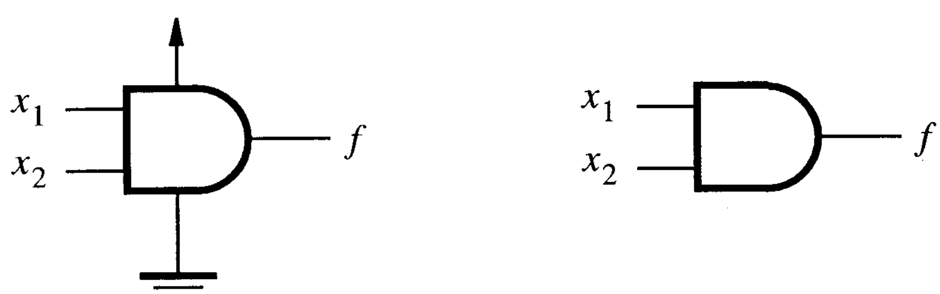
Figure 3.7 NMOS realization of a NOR gate.



(a) Circuit

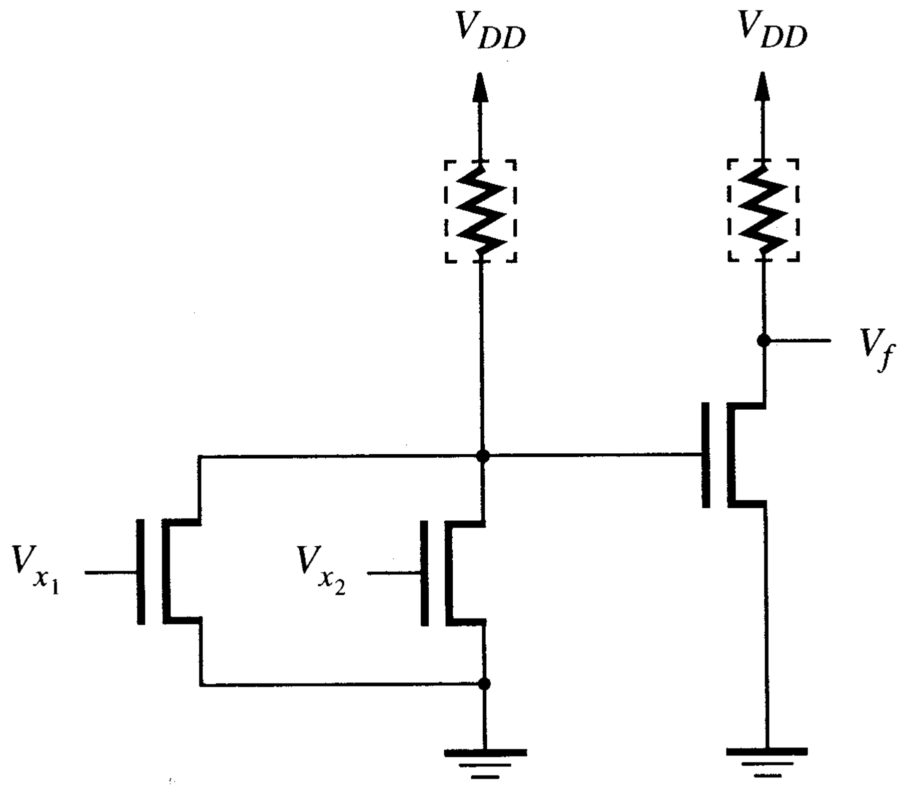
x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table



(c) Graphical symbols

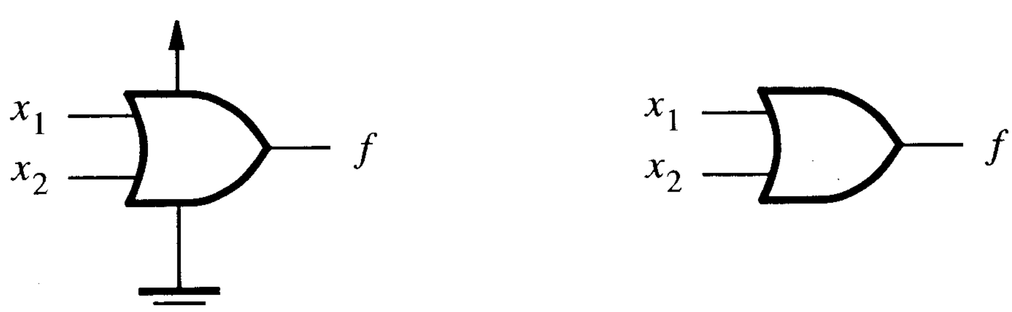
Figure 3.8 NMOS realization of an AND gate.



(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table



(c) Graphical symbols

Figure 3.9 NMOS realization of an OR gate.

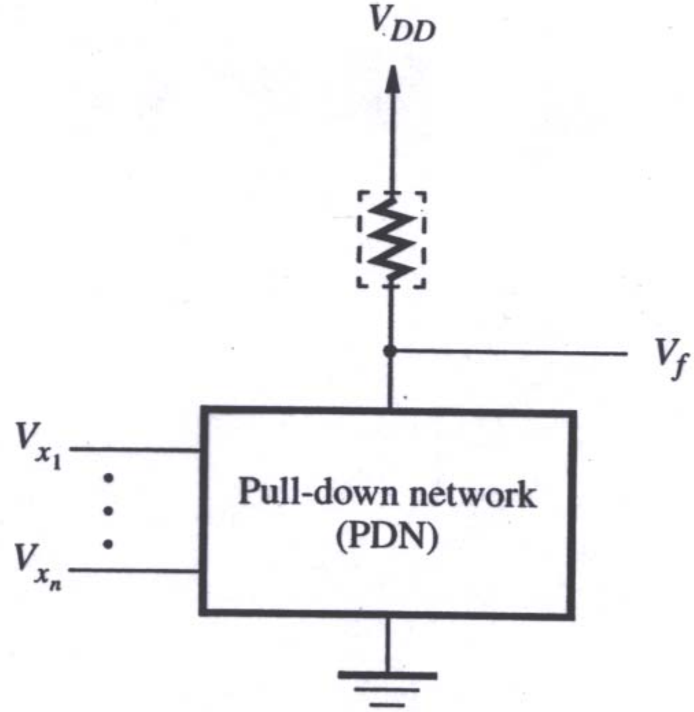


Figure 3.10 Structure of an NMOS circuit.

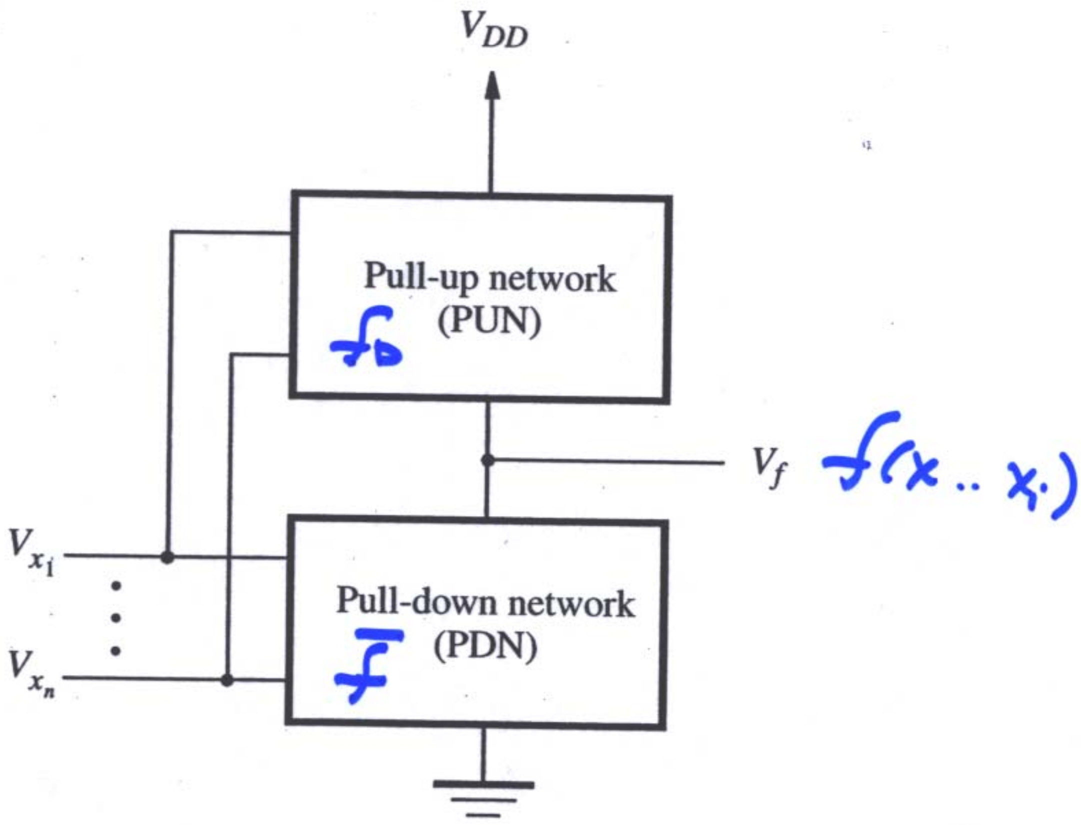
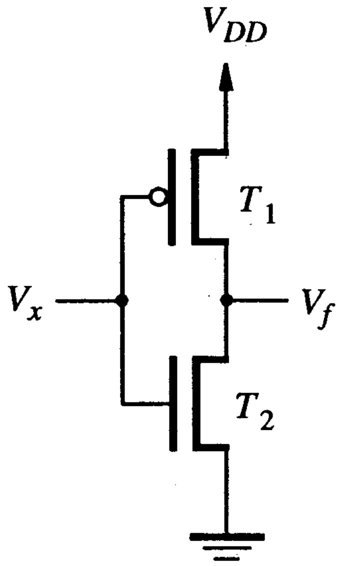


Figure 3.11 Structure of a CMOS circuit.



(a) Circuit

x	T_1	T_2	f
0	on	off	1
1	off	on	0

(b) Truth table and transistor states

Figure 3.12 CMOS realization of a NOT gate.

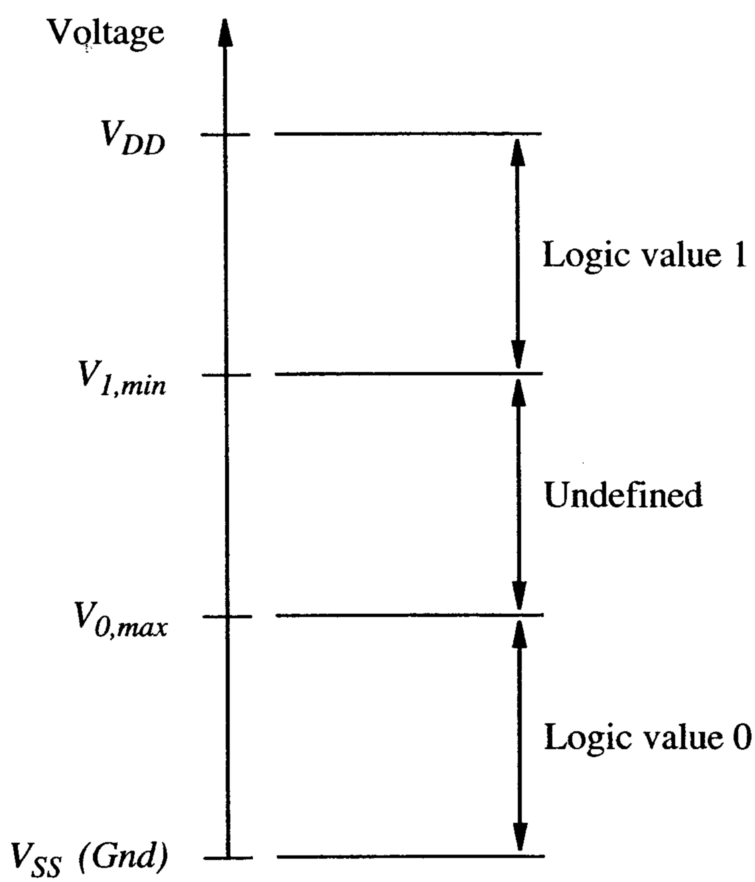
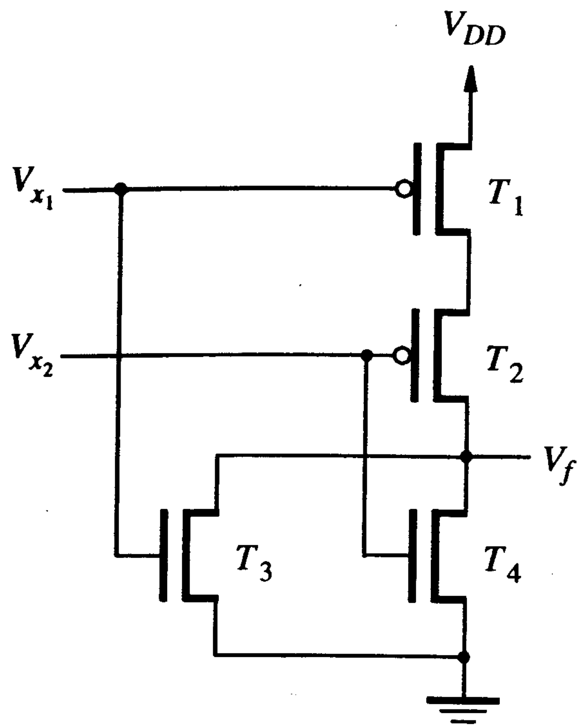


Figure 3.1 Representation of logic values by voltage levels.

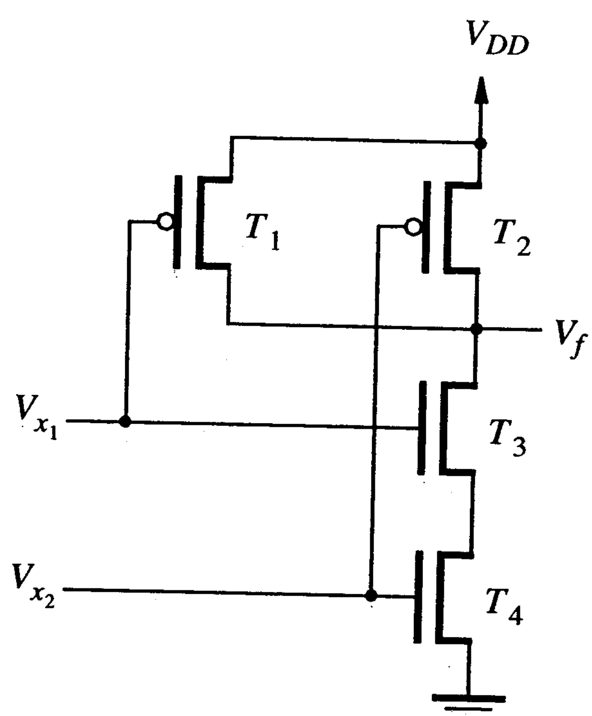


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states

Figure 3.14 CMOS realization of a NOR gate.



(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

Figure 3.13 CMOS realization of a NAND gate.

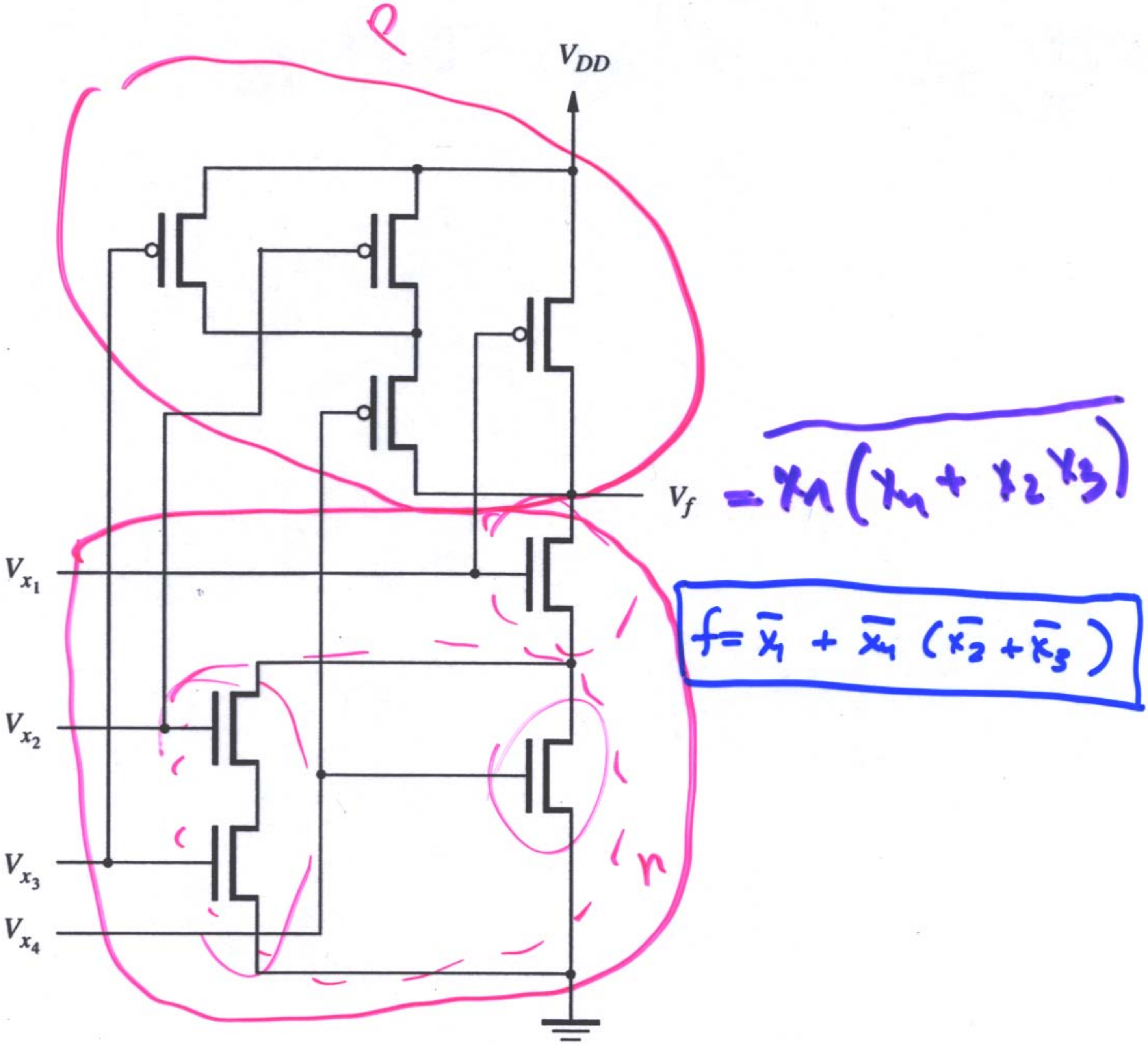
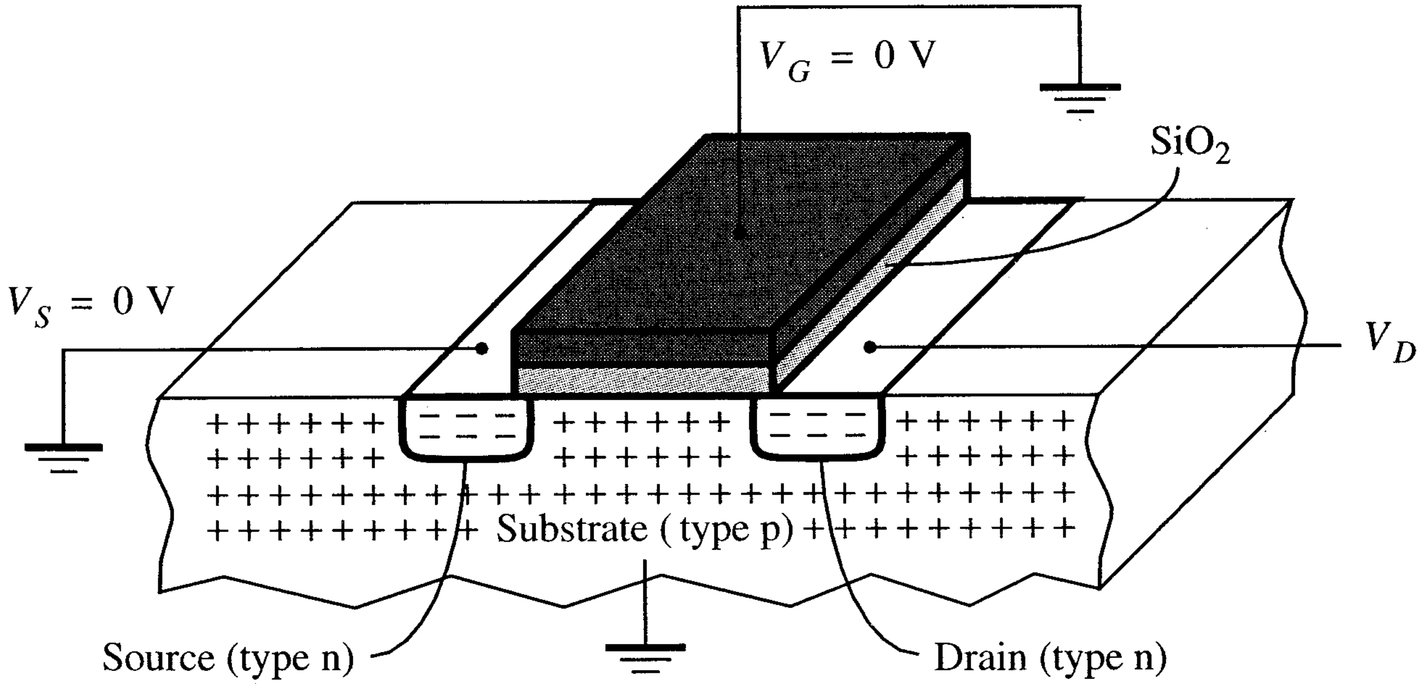
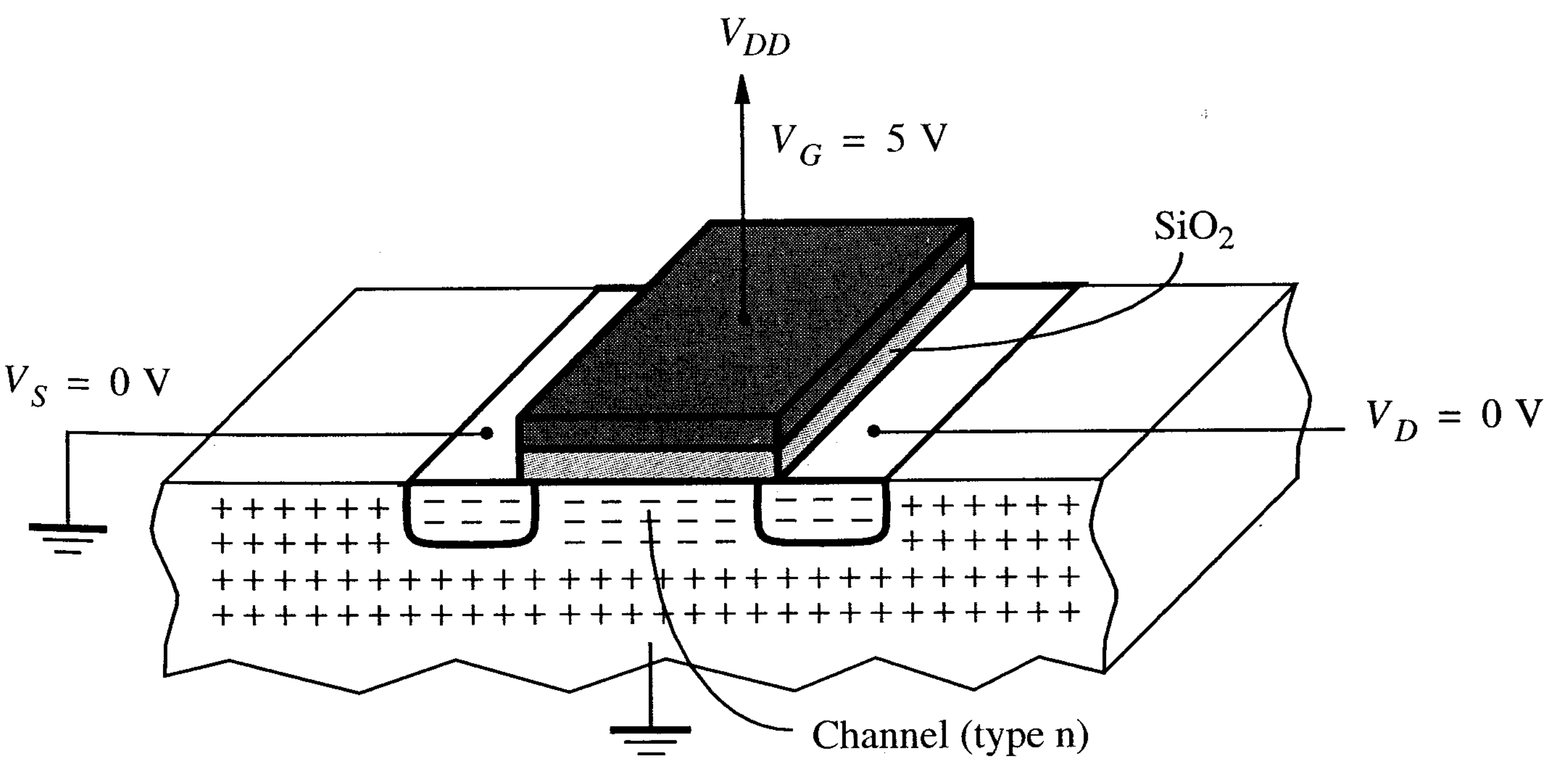


Figure 3.17 The circuit for Example 3.2.



(a) When $V_{GS} = 0$ V, the transistor is off



(b) When $V_{GS} = 5$ V, the transistor is on

Figure 3.43 Physical structure of an NMOS transistor.

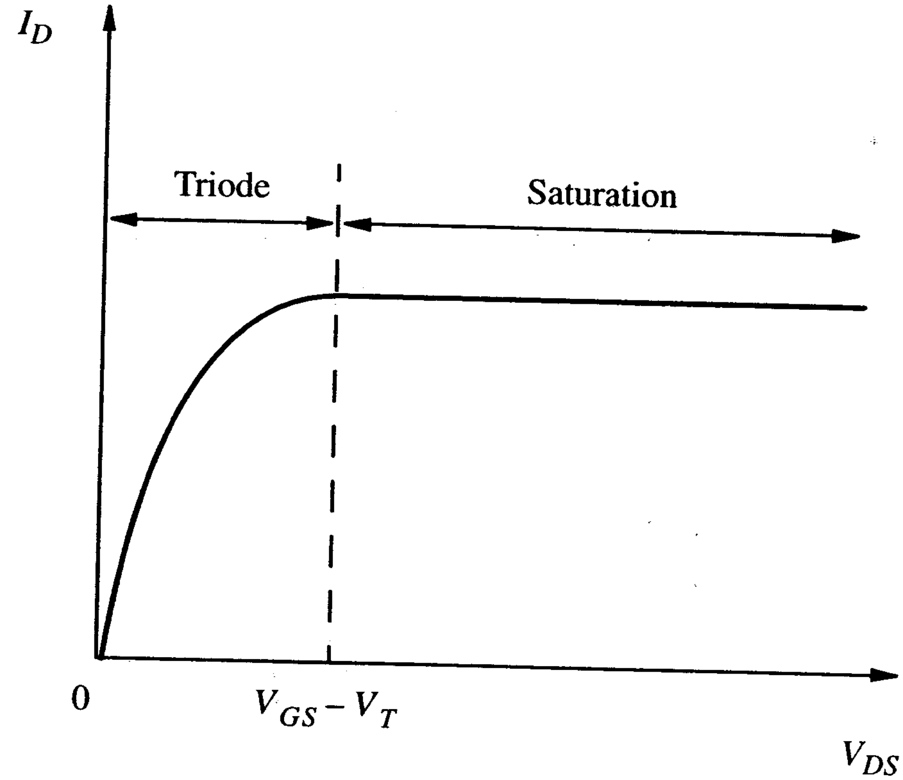
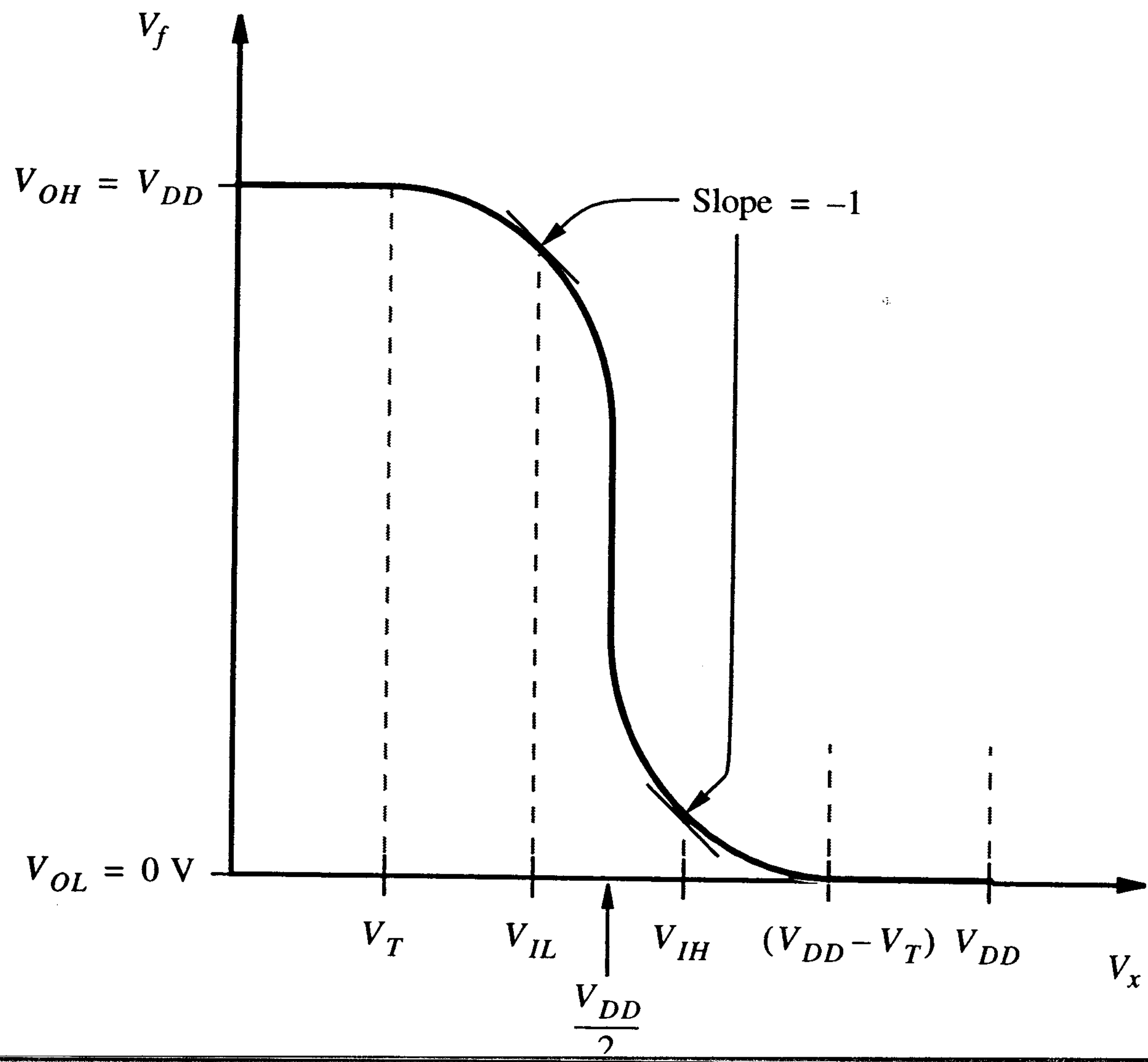


Figure 3.44 The current-voltage relationship in the NMOS transistor.

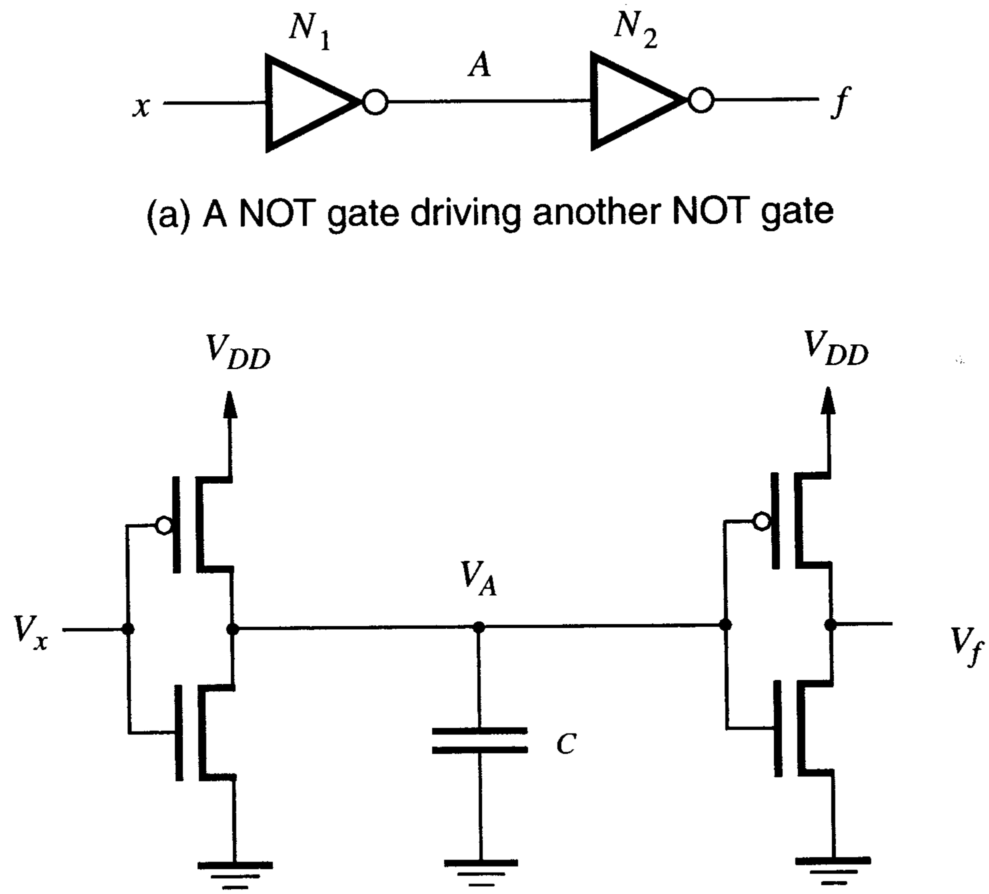


define the low *noise margin* as

$$NM_L = V_{IL} - V_{OL}$$

A similar situation exists when N_1 produces its high output voltage V_{OH}. Any existing noise in the circuit may alter the voltage level, but it will be interpreted correctly by N_2 as long as the voltage is greater than V_{IH}. The high noise margin is defined as

$$NM_H = V_{OH} - V_{IH}$$



(a) A NOT gate driving another NOT gate

(b) The capacitive load at node A

Figure 3.47 Parasitic capacitance in integrated circuits.

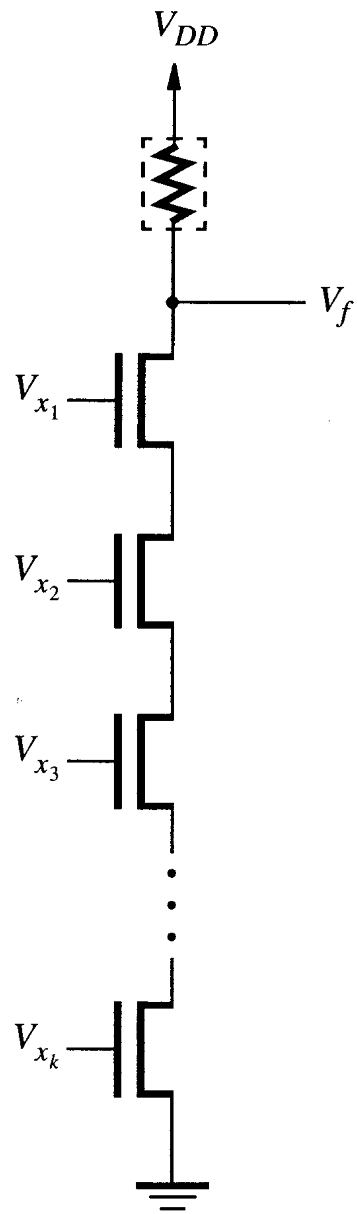
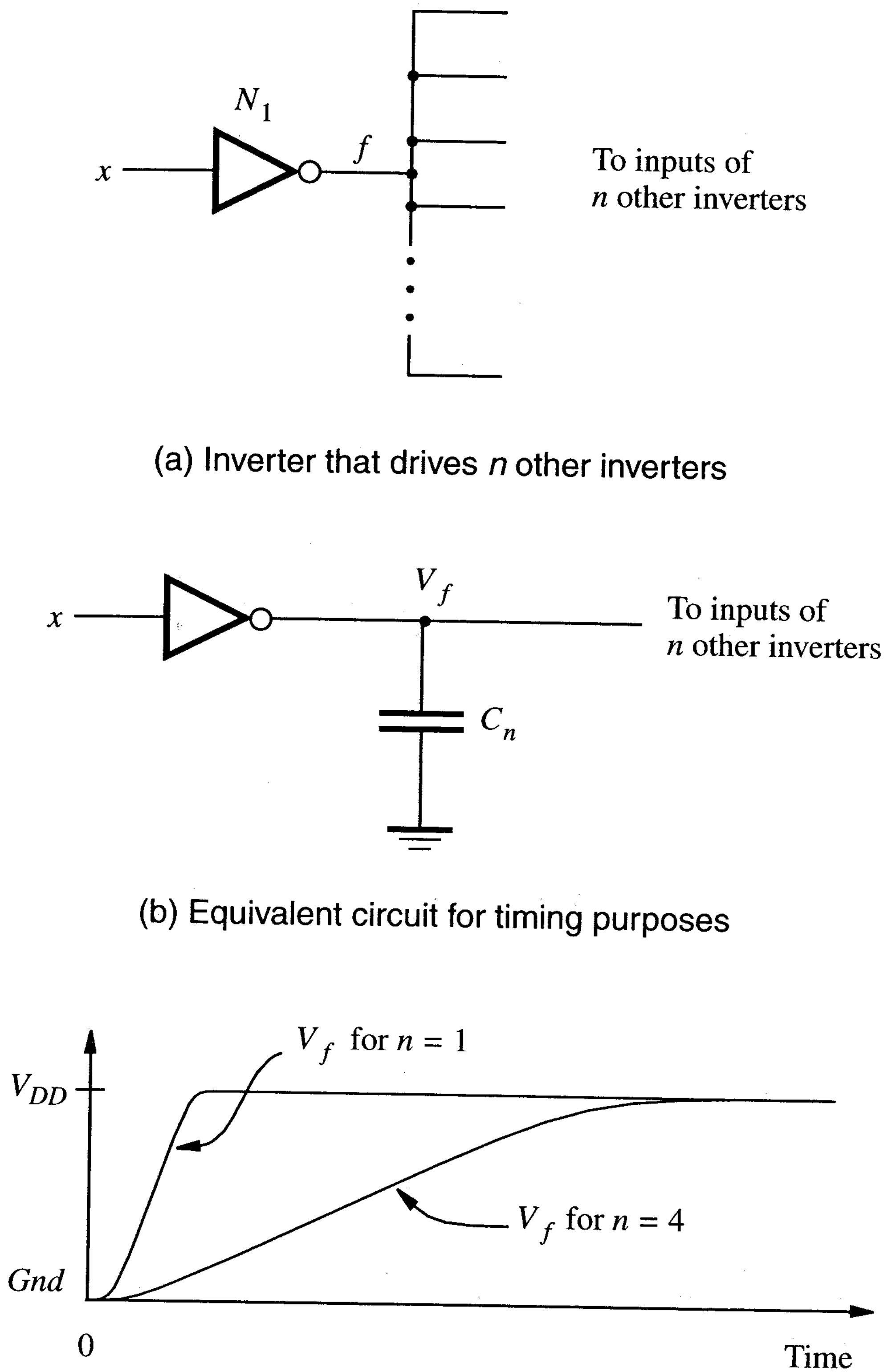


Figure 3.53 High fan-in NMOS NAND gate.

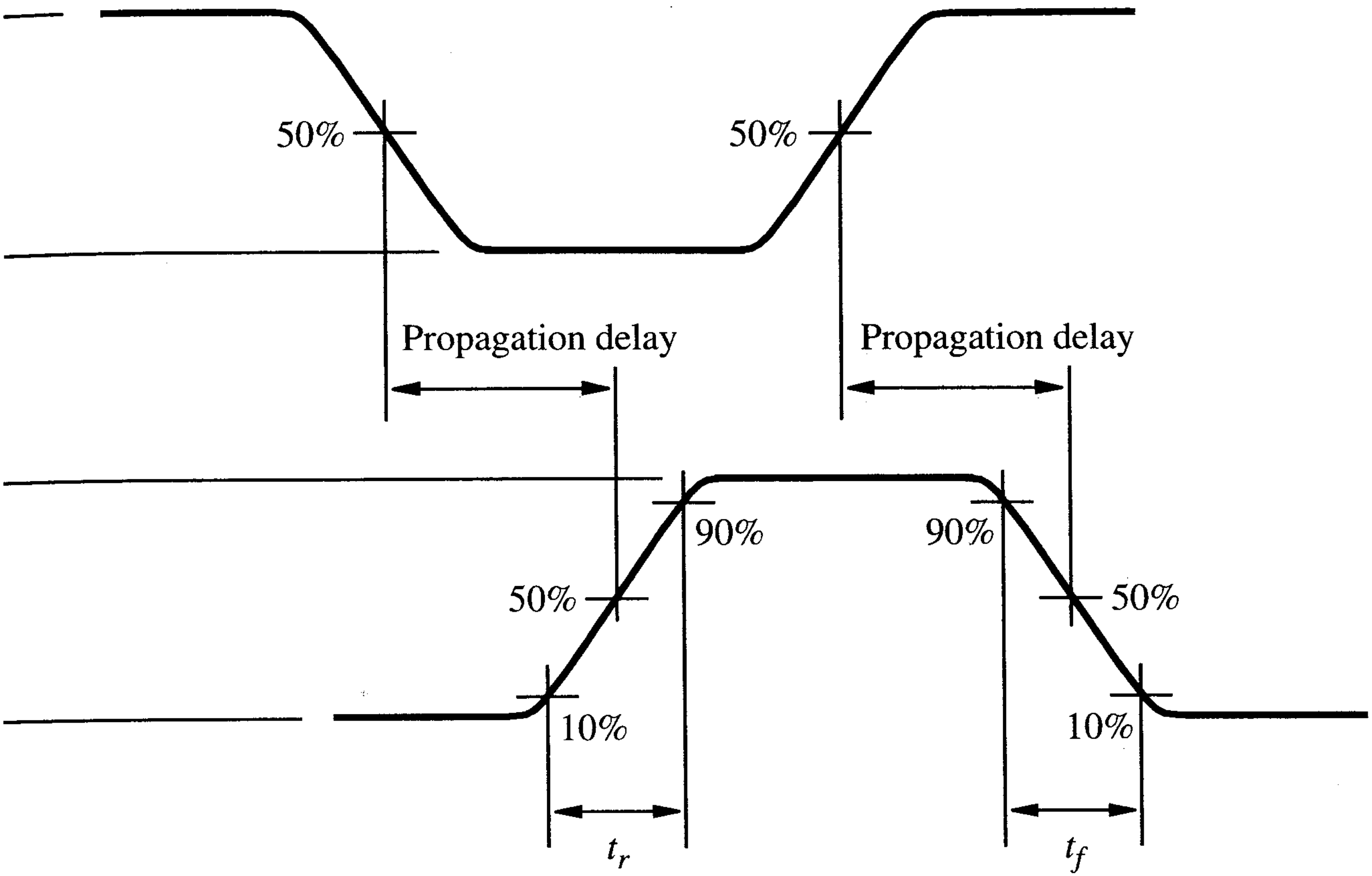


(a) Inverter that drives n other inverters

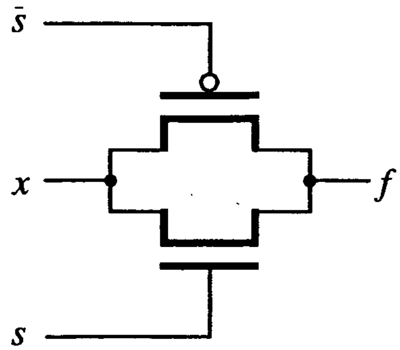
(b) Equivalent circuit for timing purposes

(c) Propagation times for different values of n

Figure 3.55 The effect of fan-out on propagation delay.



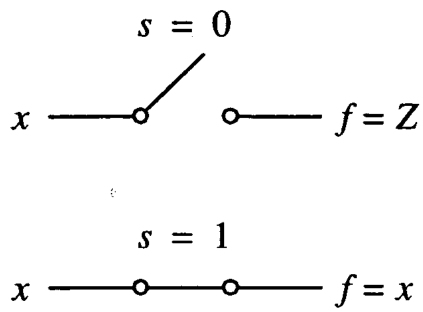
.48 Voltage waveforms for logic gates.



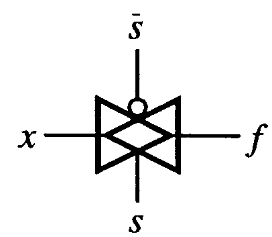
(a) Circuit

s	f
0	Z
1	x

(b) Truth table



(c) Equivalent circuit



(d) Graphical symbol

Figure 3.60 A transmission gate.

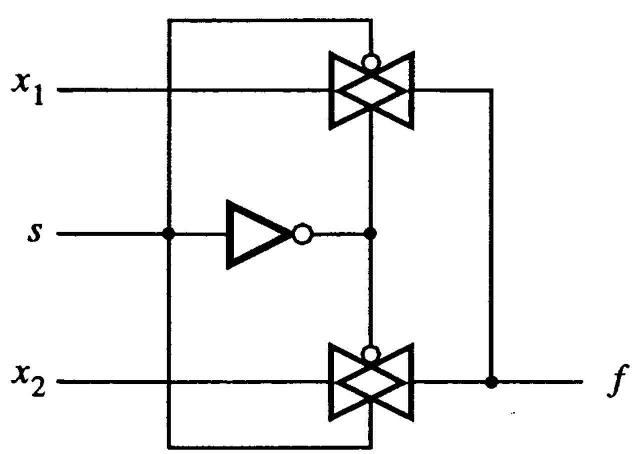
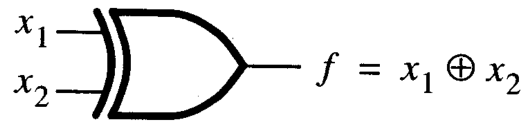


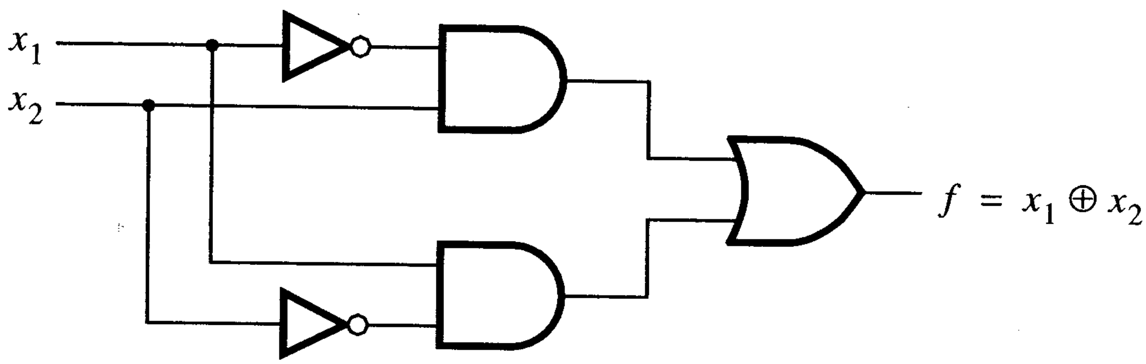
Figure 3.62 A 2-to-1 multiplexer built using transmission gates.

x_1	x_2	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

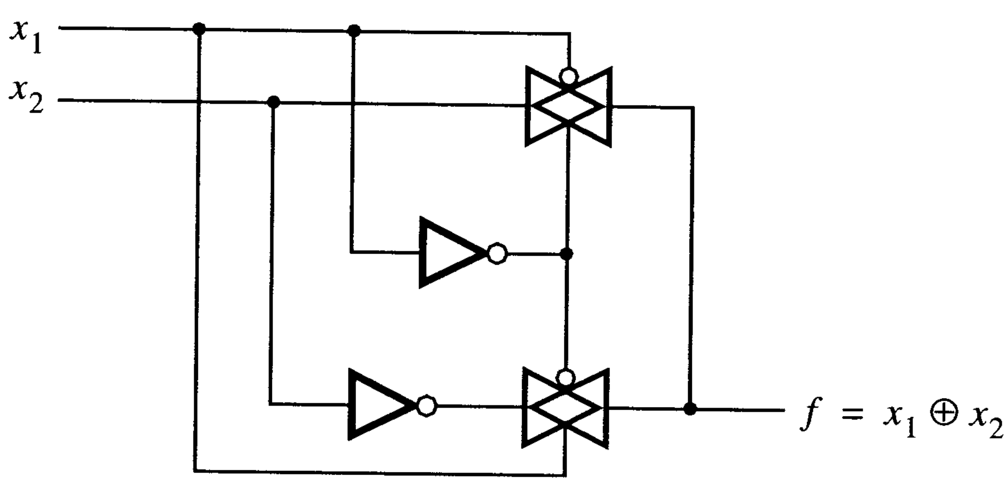
(a) Truth table



(b) Graphical symbol



(c) Sum-of-products implementation



(d) CMOS implementation

Figure 3.61 Exclusive-OR gate.

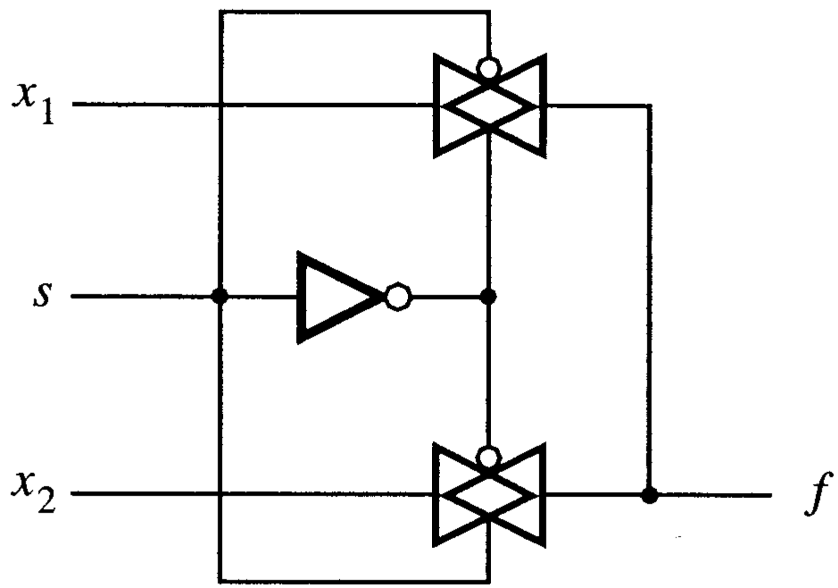


Figure 3.62 A 2-to-1 multiplexer built using transmission gates.