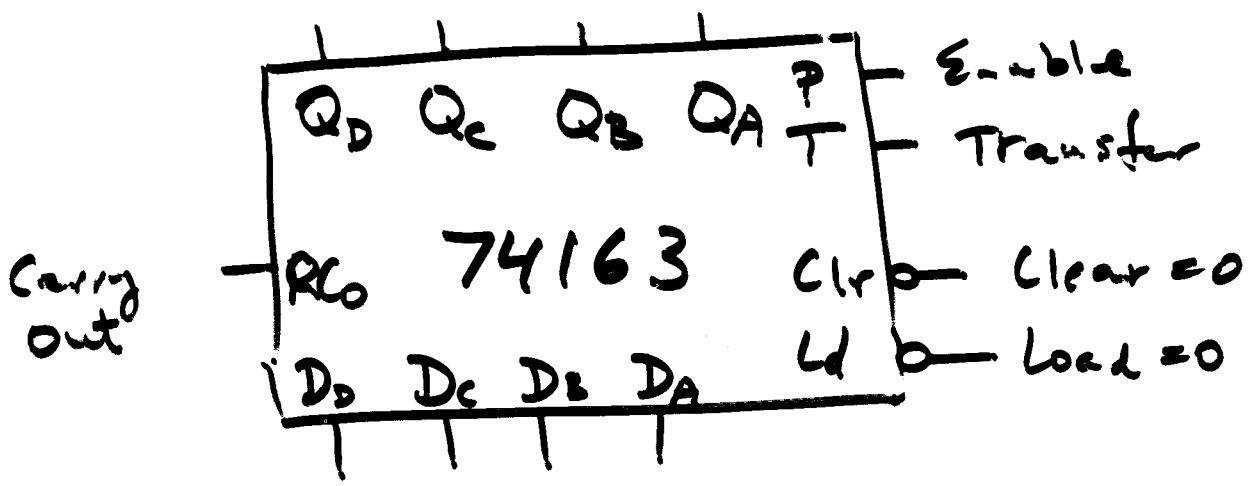
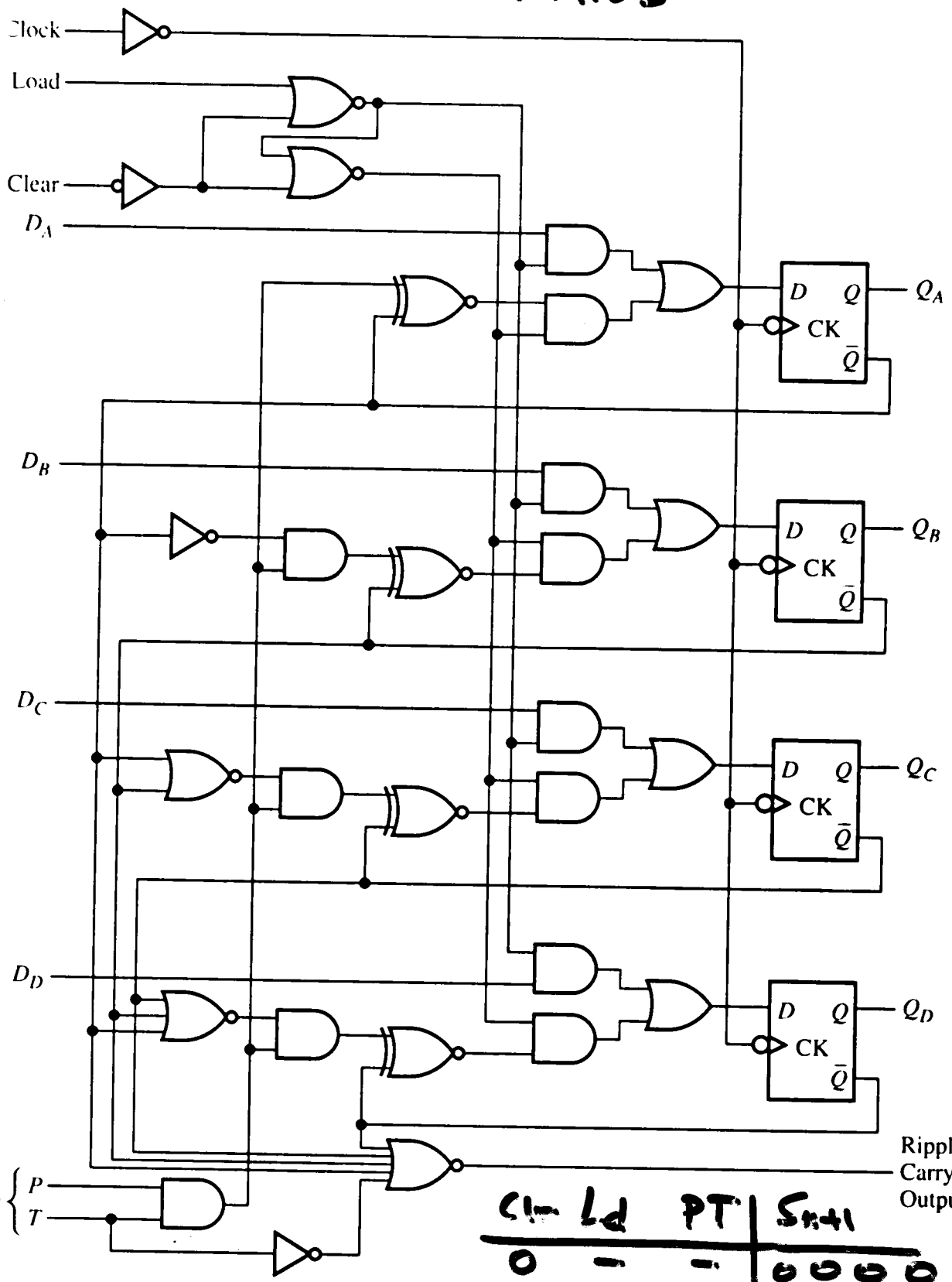
FSM Design Using Counters
(example TI: 74163)



TI 74163

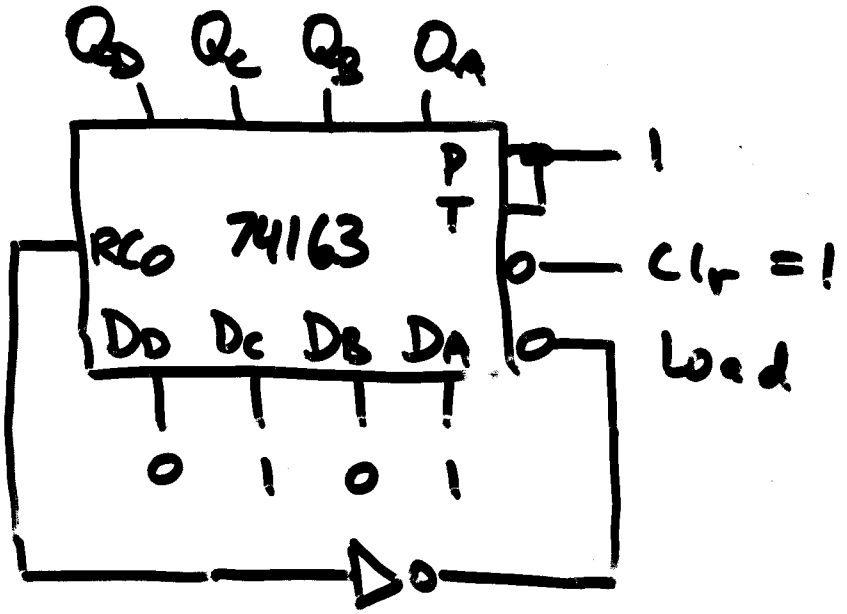


Clr	Ld	PT	S_{n+1}
0	–	–	0 0 0 0
1	0	–	D_0 D_C D_B D_A
1	1	0	D_0 D_C D_B D_A No. Clks
1	1	1	S_{n+1}

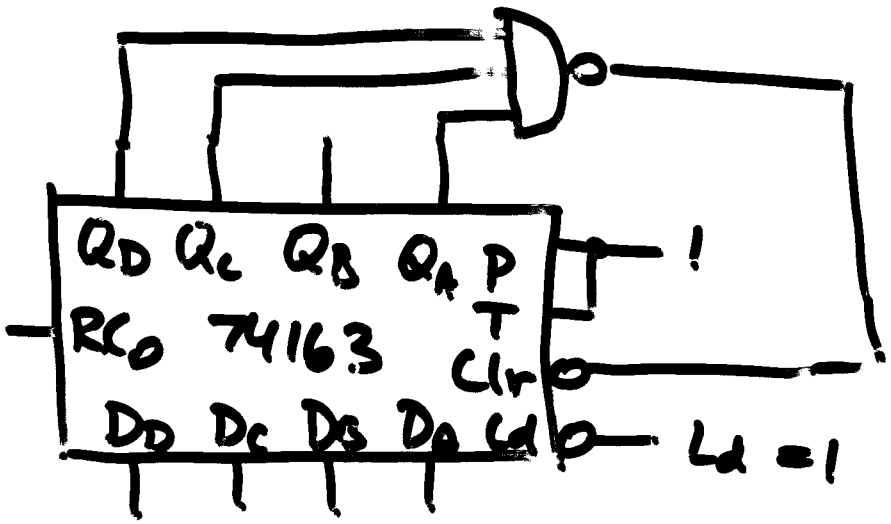
: 18–7
›3 4-Bit Counter Logic Diagram
tesy of Texas Instruments)

Use of Counters in FSM Design

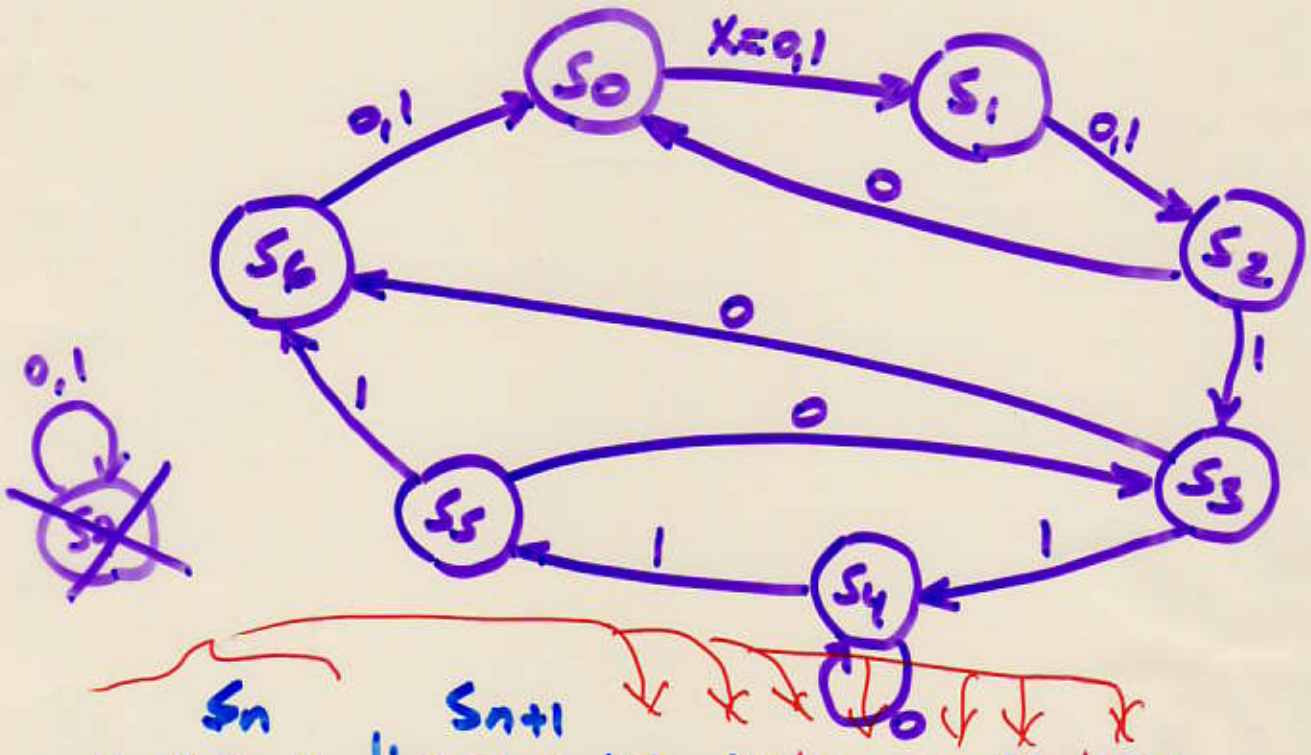
Count: 5, 6, 7, 8, 9 .... 14, 15, 5, 6, 7 ....



Count: 0, 1, 2, 3 .... 11, 12, 13, 9 1, ...

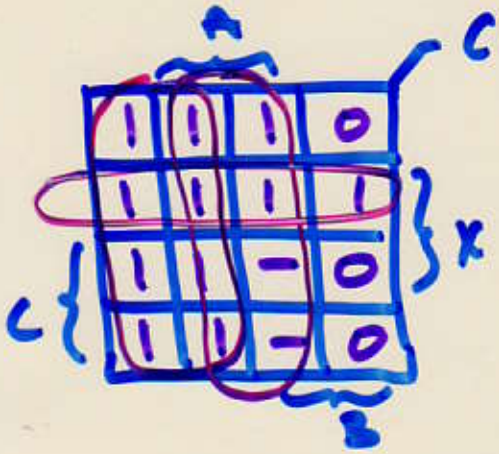


Design FSM using TI 74163 Counter:

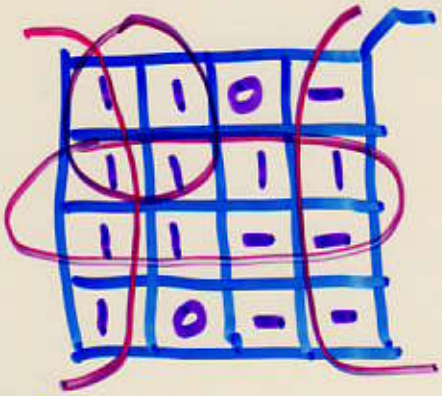


S_n				S_{n+1}									
X	C	B	A	C	B	A	Clr	Ld	D_C	D_B	D_A	PT	
0	0	0	0	0	0	1	1	1	-	-	-	1	
0	0	0	1	0	1	0	1	1	-	-	-	1	
0	0	1	0	0	0	0	0	-	-	-	-	-	
0	0	1	1	1	1	0	1	0	1	1	0	-	
0	1	0	0	1	0	0	1	1	-	-	-	0	Inhibit Cnt.
0	1	0	1	0	1	1	1	0	0	1	1	-	
0	1	1	0	0	0	0	0	-	-	-	-	-	
0	1	1	1	-	-	-	-	-	-	-	-	-	
1	0	0	0	0	0	1	1	1	-	-	-	1	
1	0	0	1	0	1	0	1	1	-	-	-	1	
1	0	1	0	0	1	1	1	1	-	-	-	1	
1	0	1	1	1	0	0	1	1	-	-	-	1	
1	1	0	0	1	0	1	1	1	-	-	-	1	
1	1	0	1	1	1	0	1	1	-	-	-	1	
1	1	1	0	0	0	0	0	-	-	-	-	-	
1	1	1	1	-	-	-	-	-	-	-	-	-	

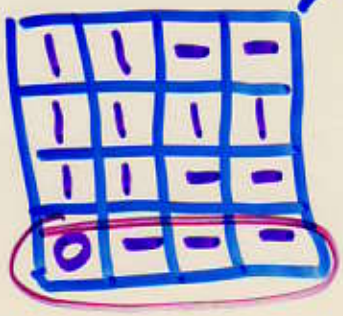
Design FSM using TI 74163 Counter



$Clr = Q_A + Q_{\bar{B}} + X Q_{\bar{C}}$



$Ld = Q_{\bar{A}} + X + Q_{\bar{B}\bar{C}}$



$PT = X + \bar{C}$

$D_C = B$

$D_B = 1$

$D_A = C$