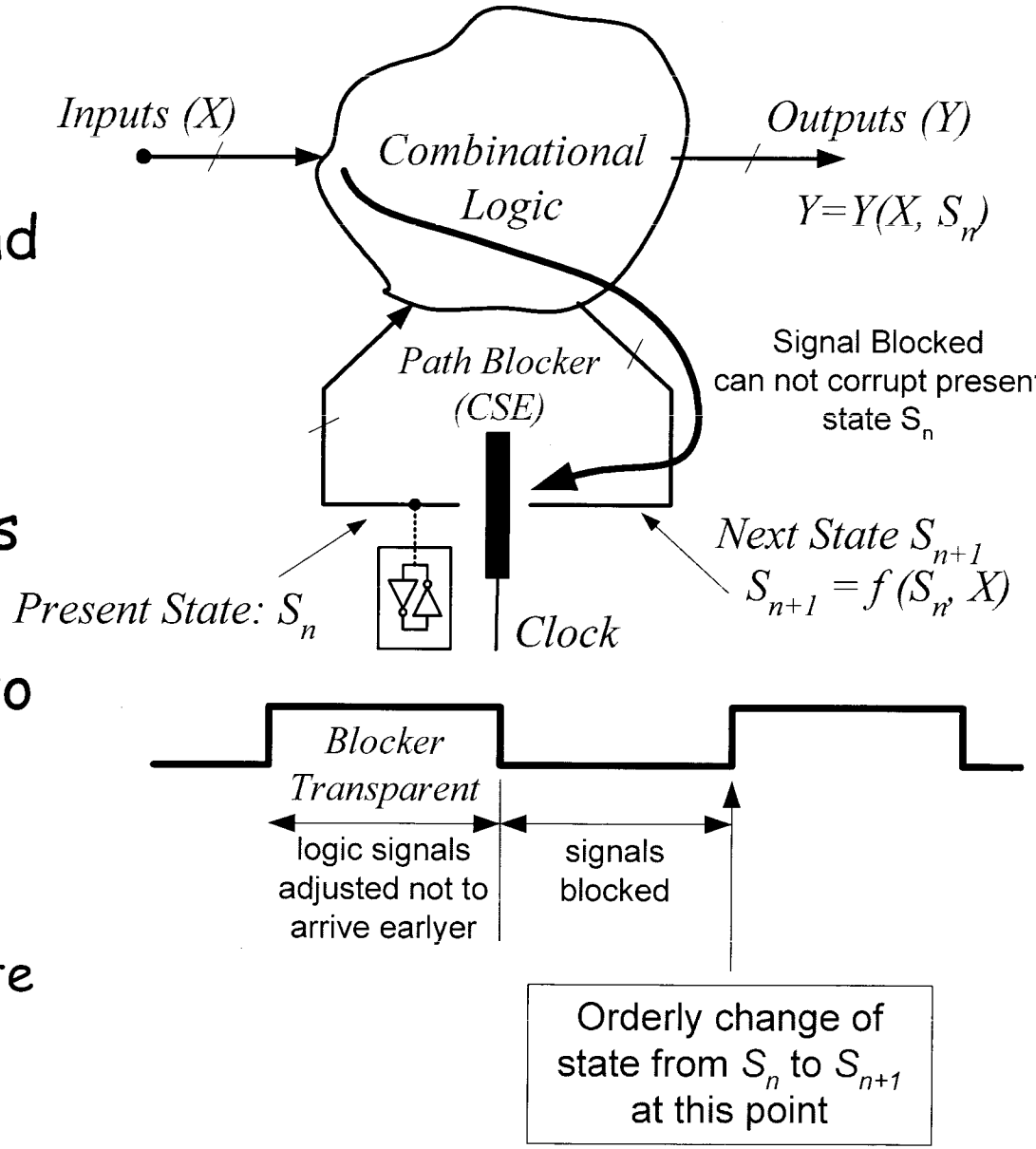
Clock Frequency of Selected Historic Computers and Supercomputers

System	Intro Date	Technology	Class	Nominal Clock Period (nS)	Nominal Clock Frequency (MHz)
Cray-X-MP	1982	MSI ECL	Vector Processor	9.5	105.3
Cray-1S,-1M	1980	MSI ECL	Vector Processor	12.5	80.0
CDC Cyber 180/990	1985	ECL	Mainframe	16.0	62.5
IBM 3090	1986	ECL	Mainframe	18.5	54.1
Amdahl 58	1982	LSI ECL	Mainframe	23.0	43.5
IBM 308X	1981	LSI TTL	Mainframe	24.5, 26.0	40.8,38.5
Univac 1100/90	1984	LSI ECL	Mainframe	30.0	33.3
MIPS-X	1987	VLSI CMOS	Microprocessor	50.0	20.0
HP-900	1982	VLSI CMOS	Micro-mainframe	55.6	18.0
Motorola 68020	1985	VLSI CMOS	Microprocessor	60.0	16.7
Bellmac-32A	1982	VLSI CMOS	Microprocessor	125.0	8.0

Another Representation of FSM

- Clocked Storage Elements: Flip-Flops and Latches should be viewed as synchronization elements, not merely as storage elements !
- Their main purpose is to synchronize fast and slow paths:
  - prevent the fast path from corrupting the state



State Changes in the Finite-State Machine

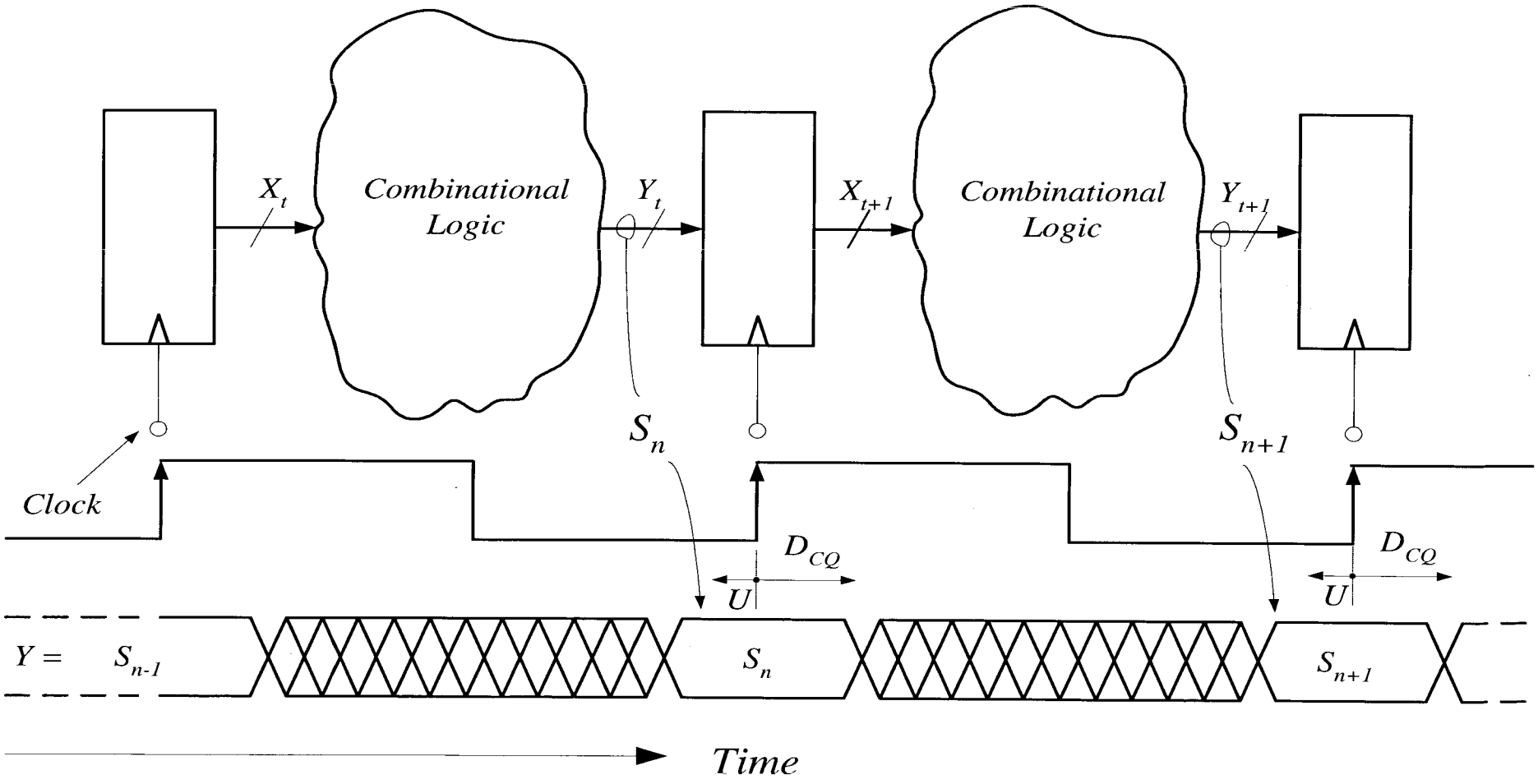
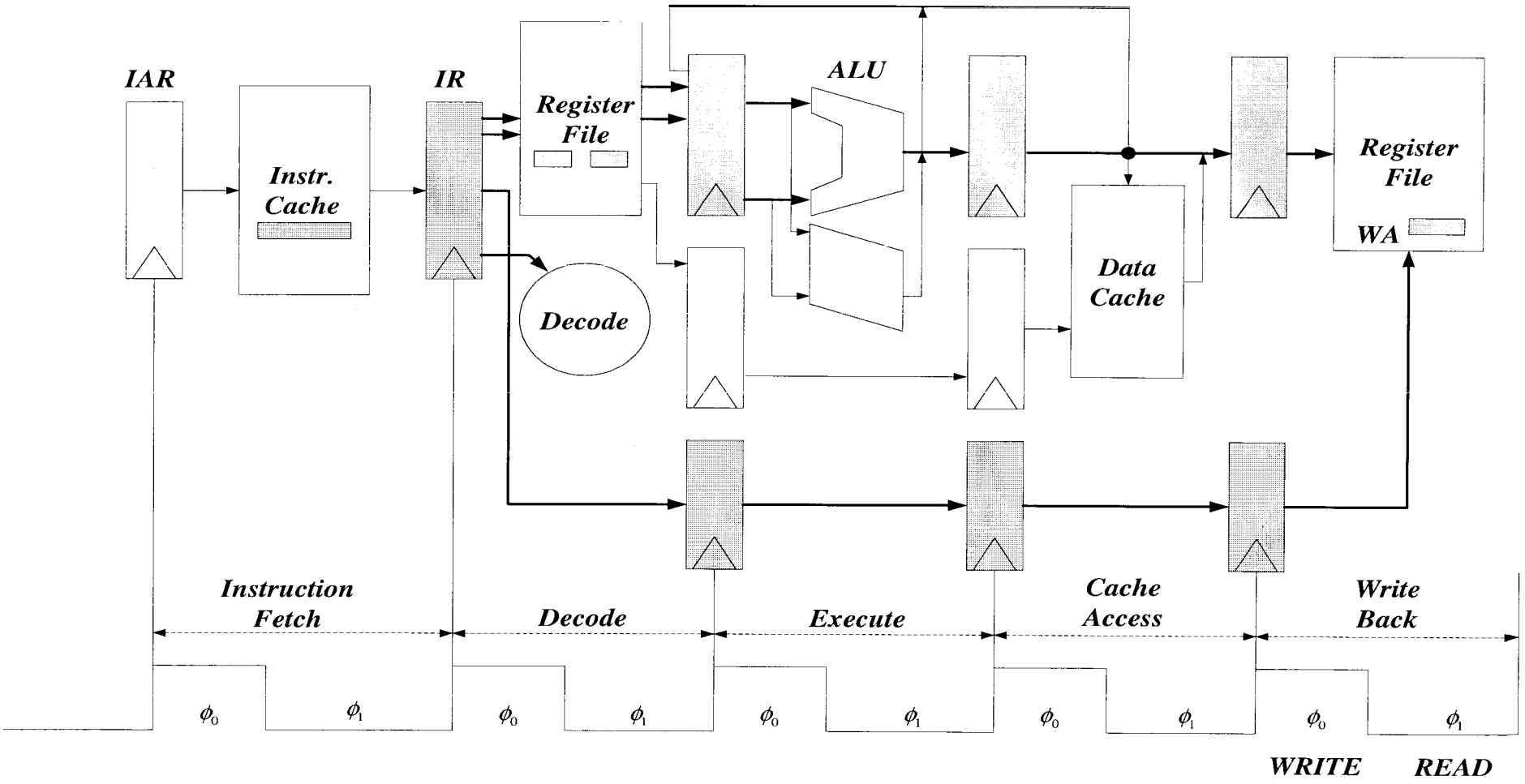
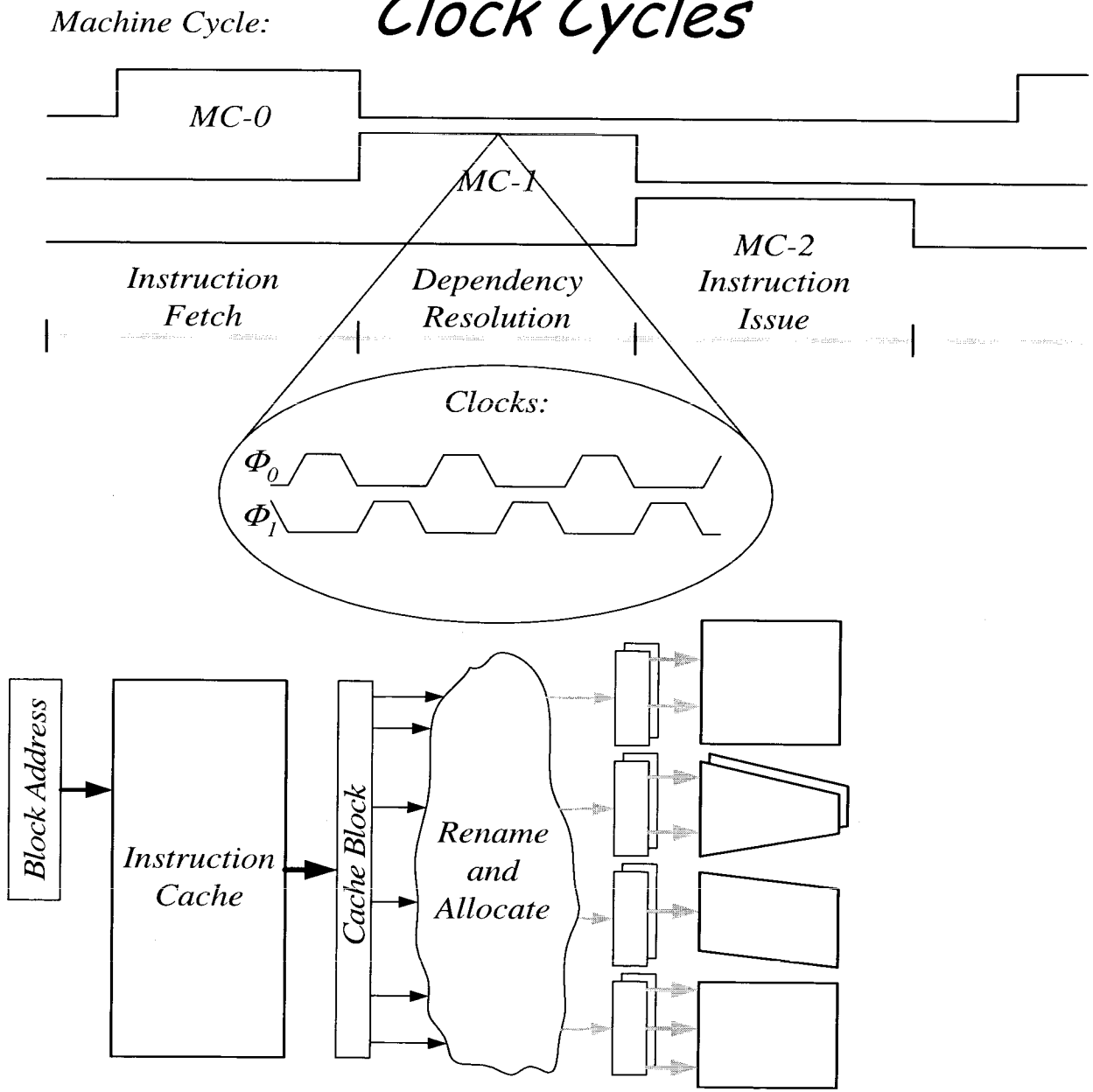


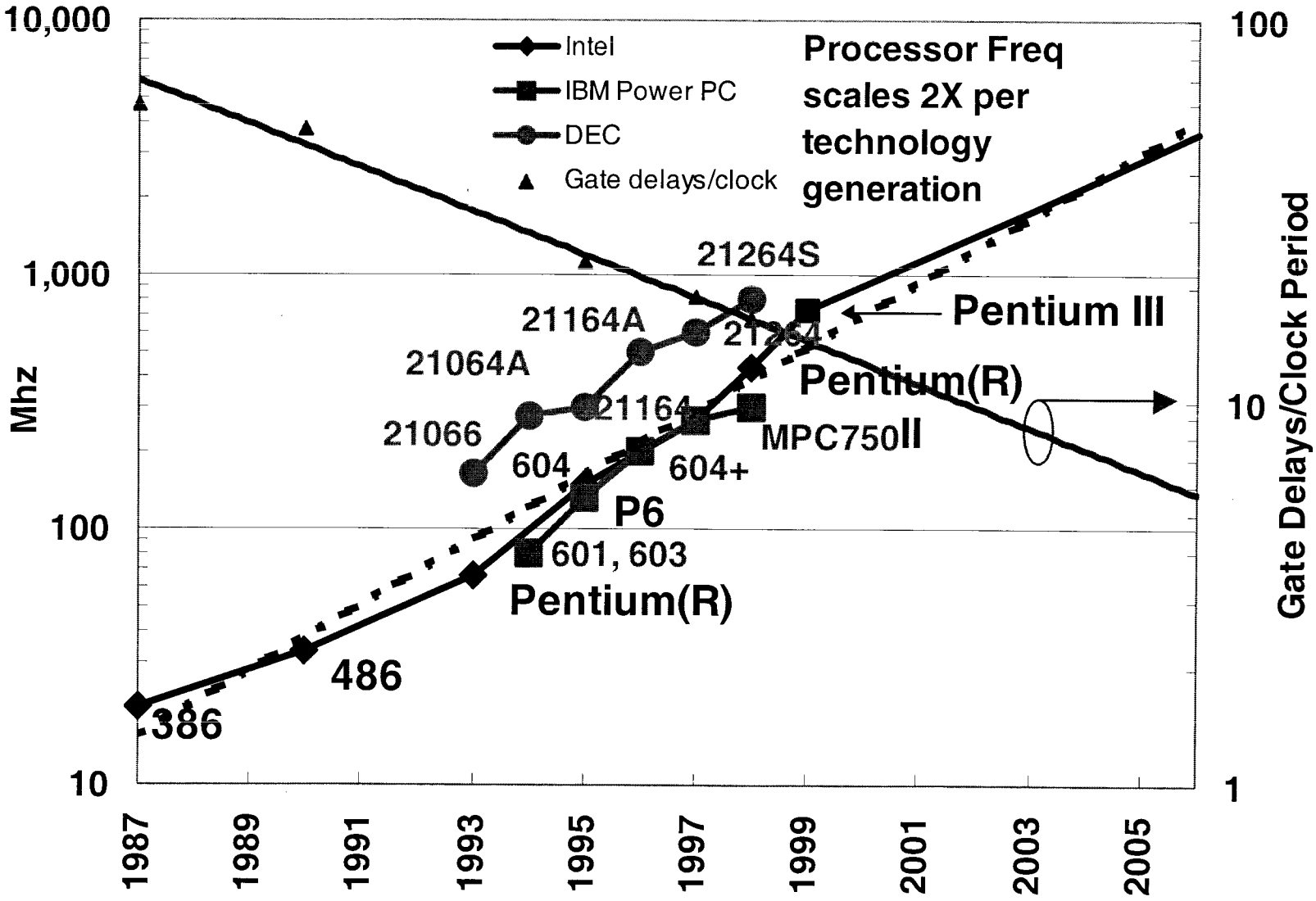
Diagram of a Pipelined System



Machine Execution Phases with Respect to the Clock Cycles



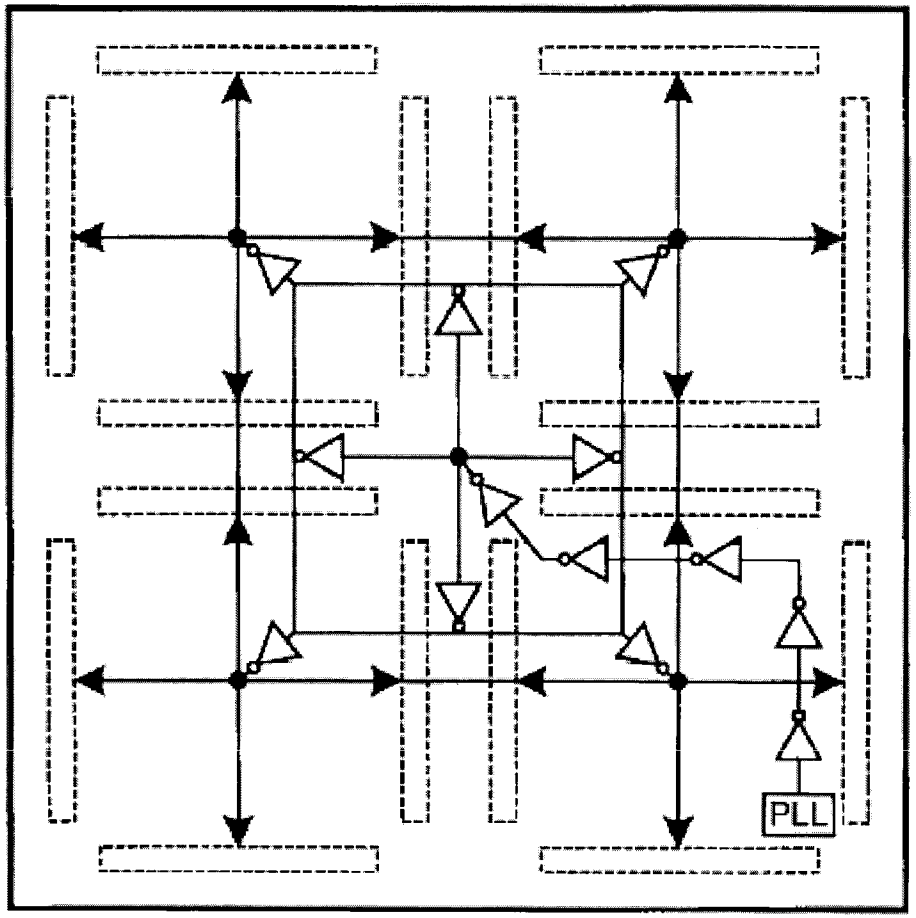
Increase in the Clock Frequency and Decrease in the Number of Logic Levels

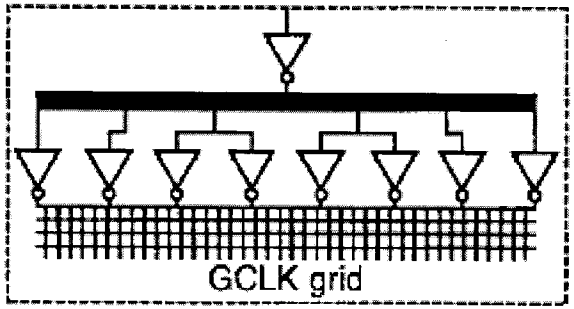


Clock distribution methods:

(a) an RC matched tree, and (b) a grid

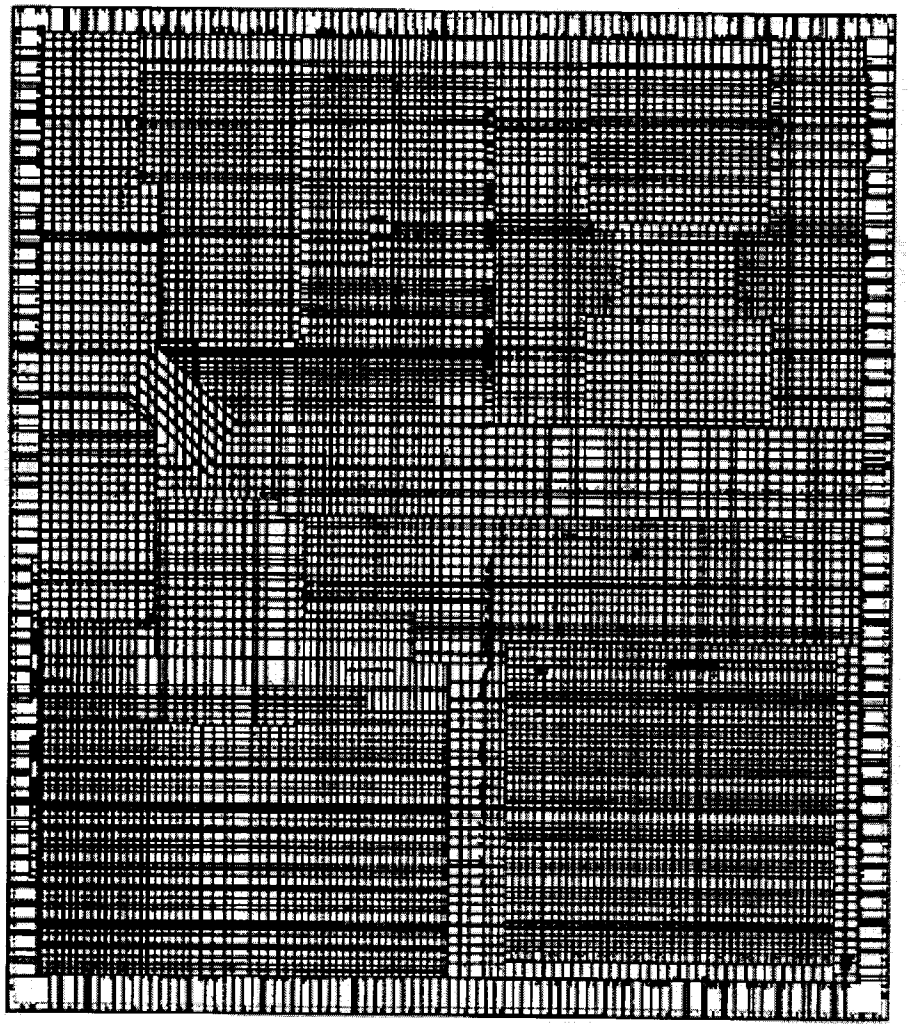
(Bailey and Benschneider 1998), Copyright © 1988, IEEE



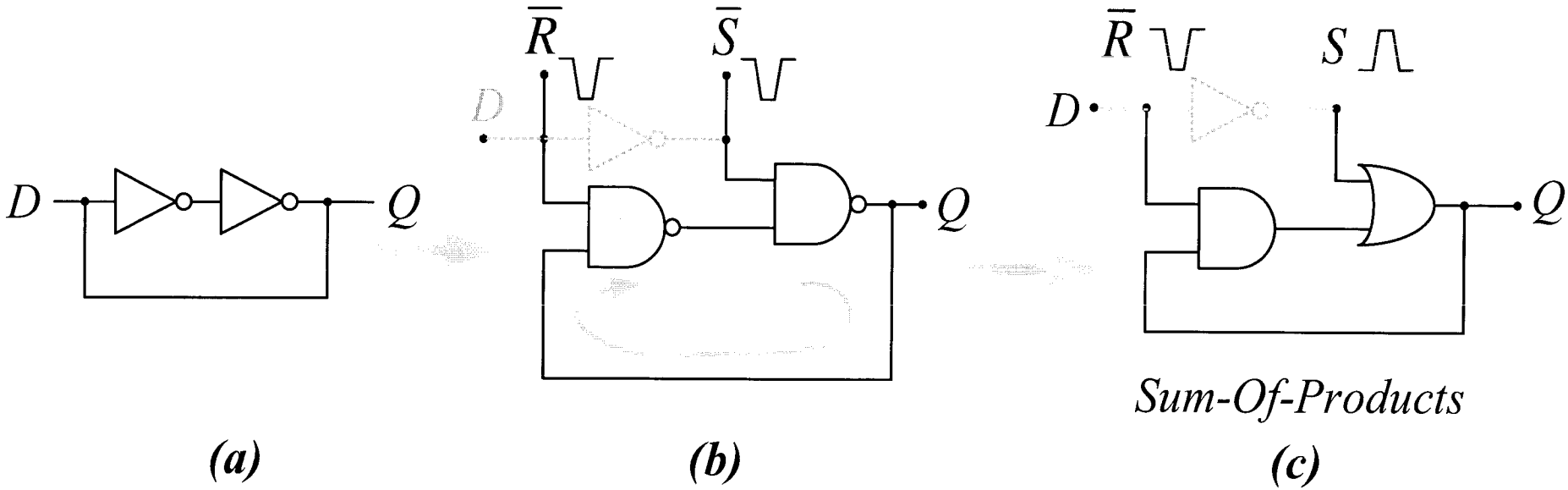


Clock distribution grid used in a DEC Alpha 600-MHz processor

(Bailey and Benschneider 1998), Copyright © 1988, IEEE



Evolution of a Latch :

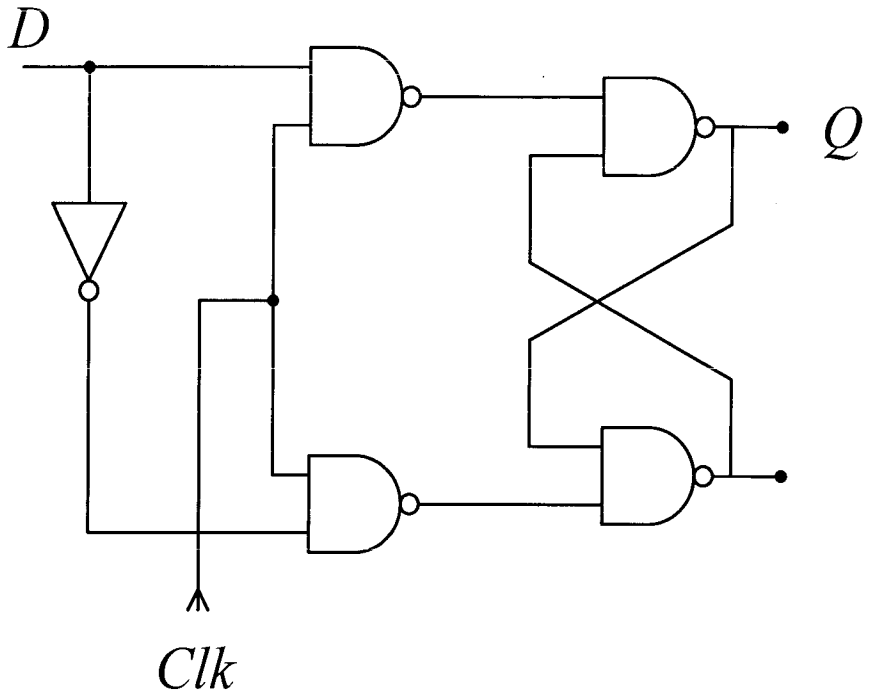


(a) keeper; information is latched

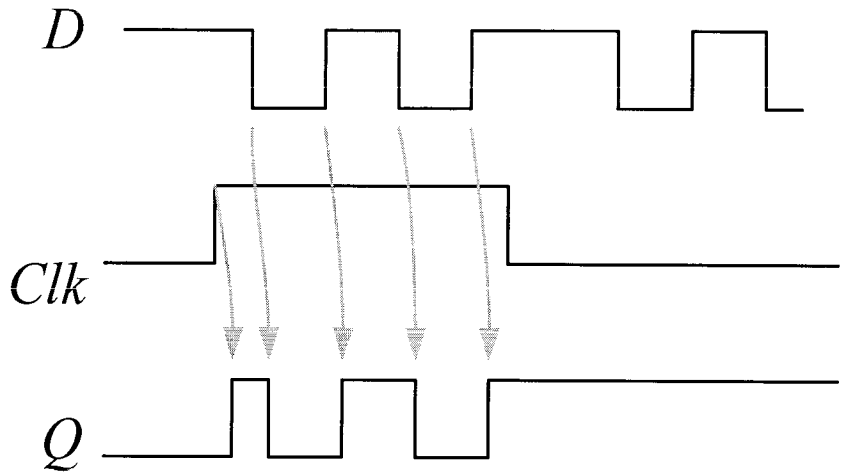
(b) S-R latch; information can be modified

(c) S-o-P latch; S-R latch that can implement a function – IMPORTANT !

Adding Clock Control to a Latch



(a)

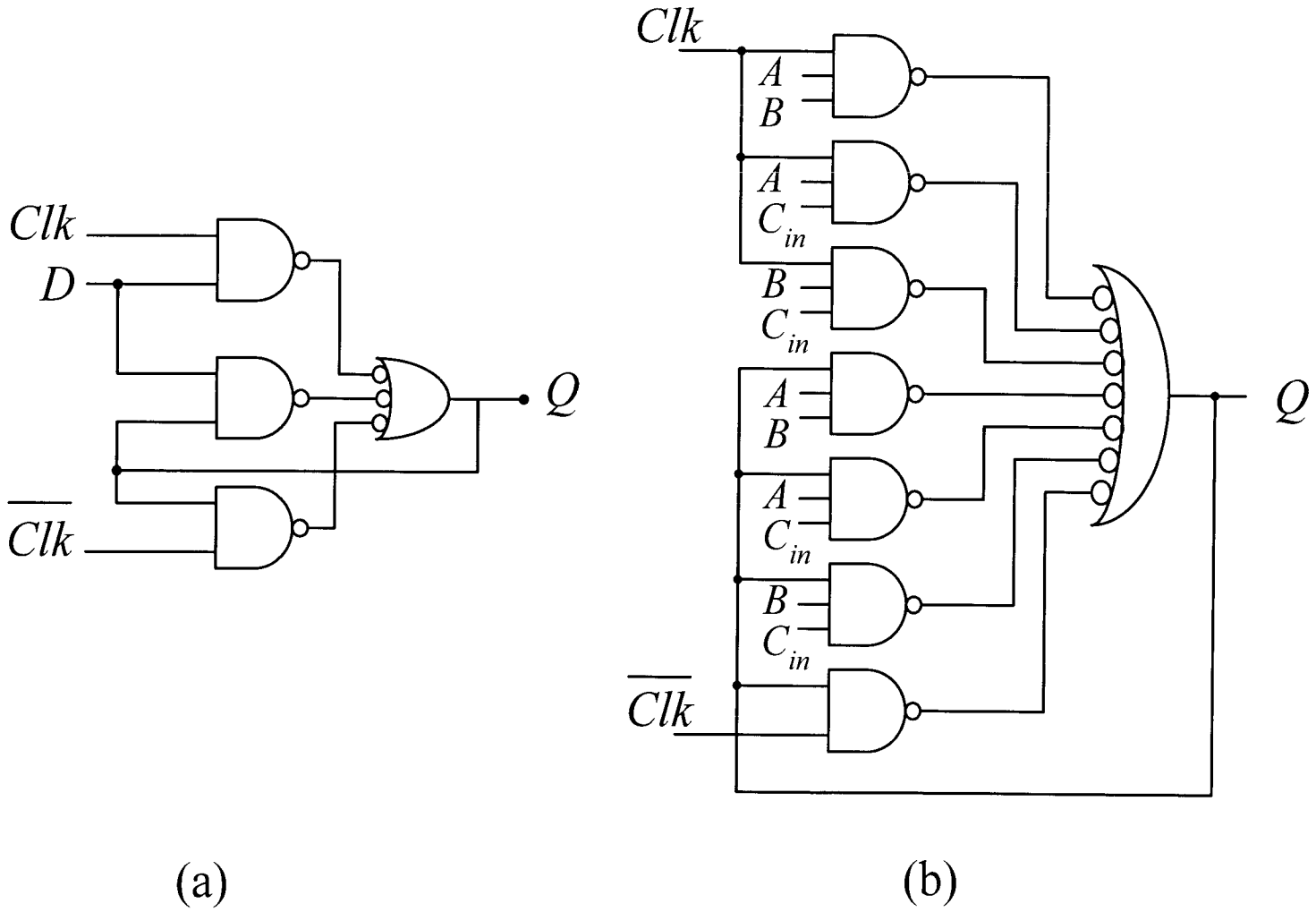


(b)

Latching can be done only when clock is active, otherwise no change is allowed:

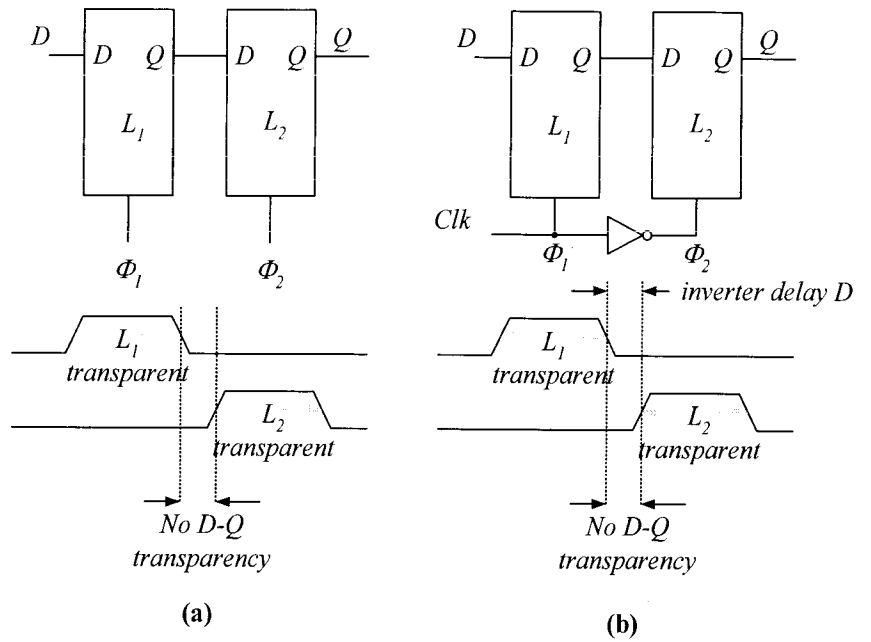
(a) Clocked D-latch; (b) timing diagram of clocked D-latch

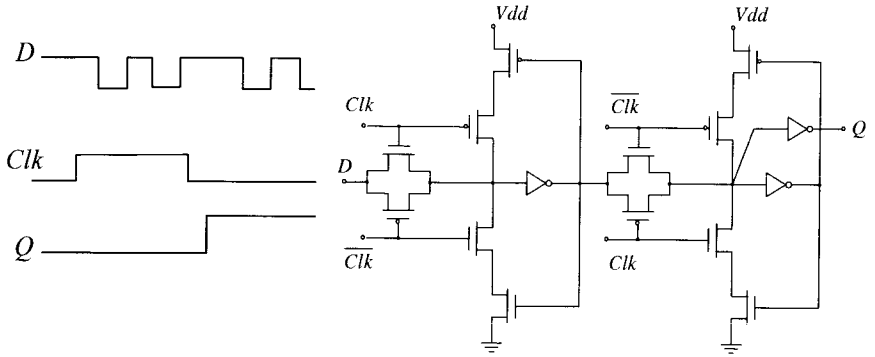
Importance of Latch S-o-P Configuration



(a) Basic Earl's Latch; (b) Implementing the Carry function

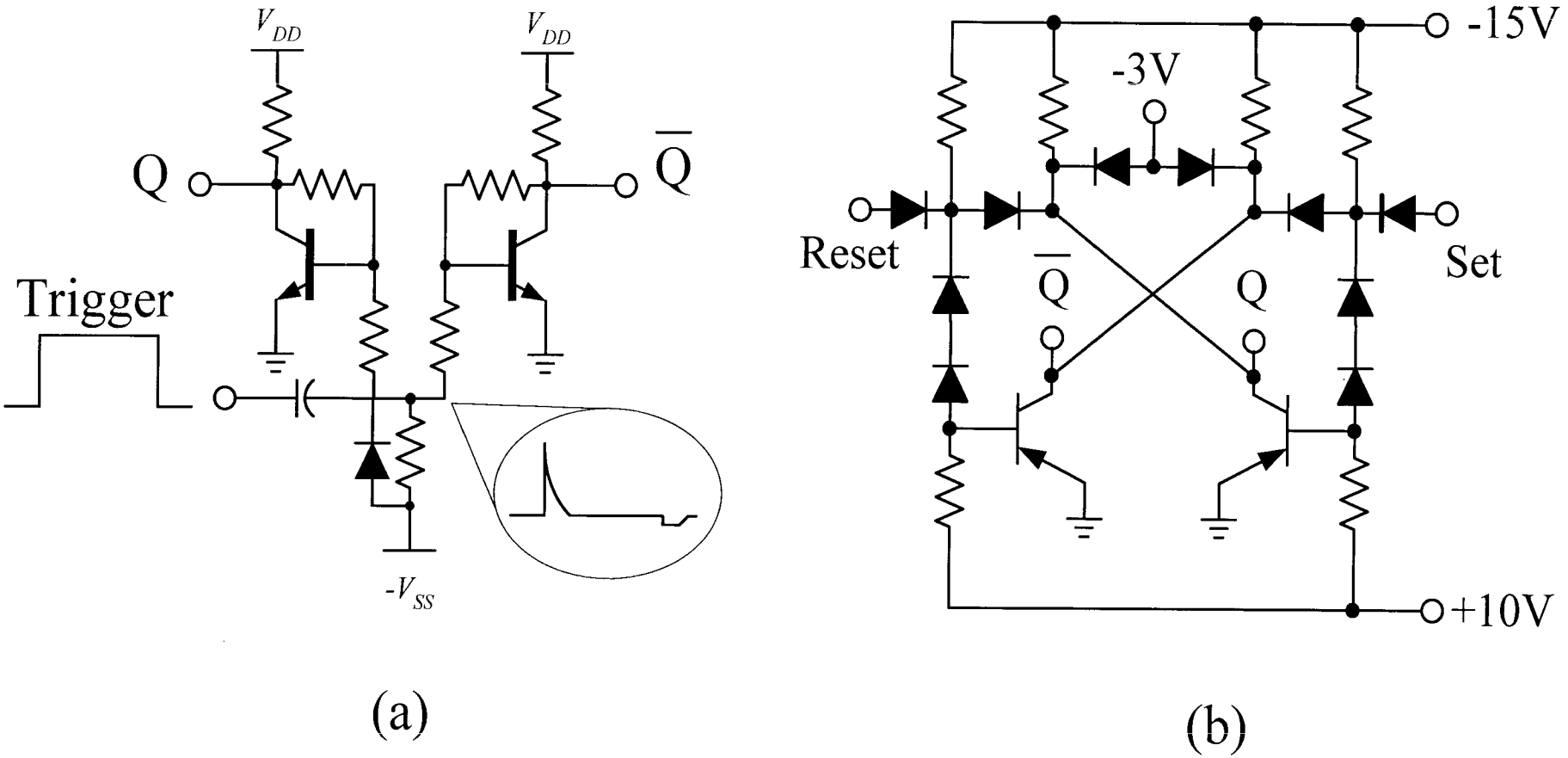
Master-Slave Latch





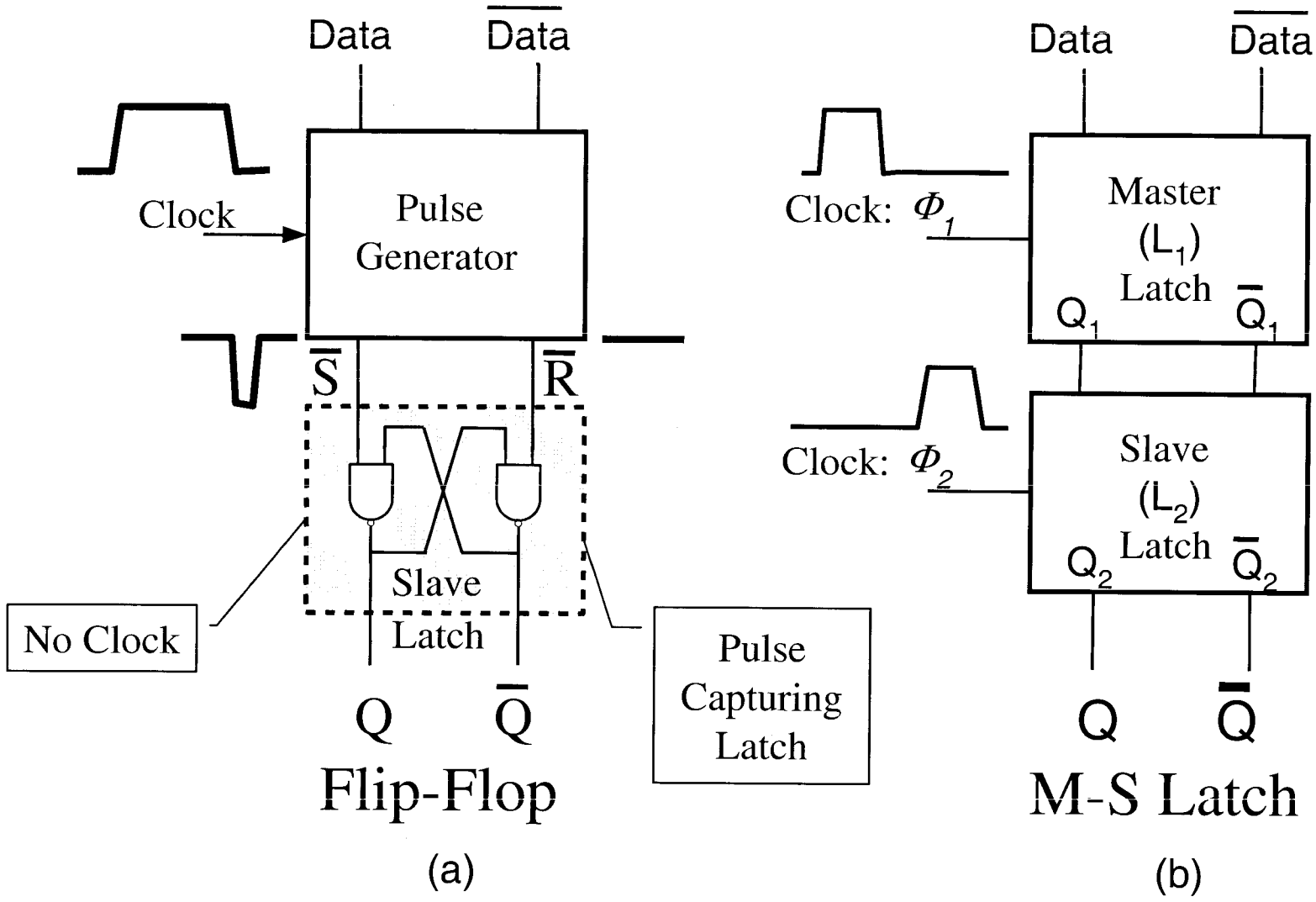
(a) non-overlapping clocks; (b) single external clock; (c) timing diagram; (d) PowerPC 603 MS Latch (Gerosa, JSSC 12/94), Copyright © 1994 IEEE

Flip-flop



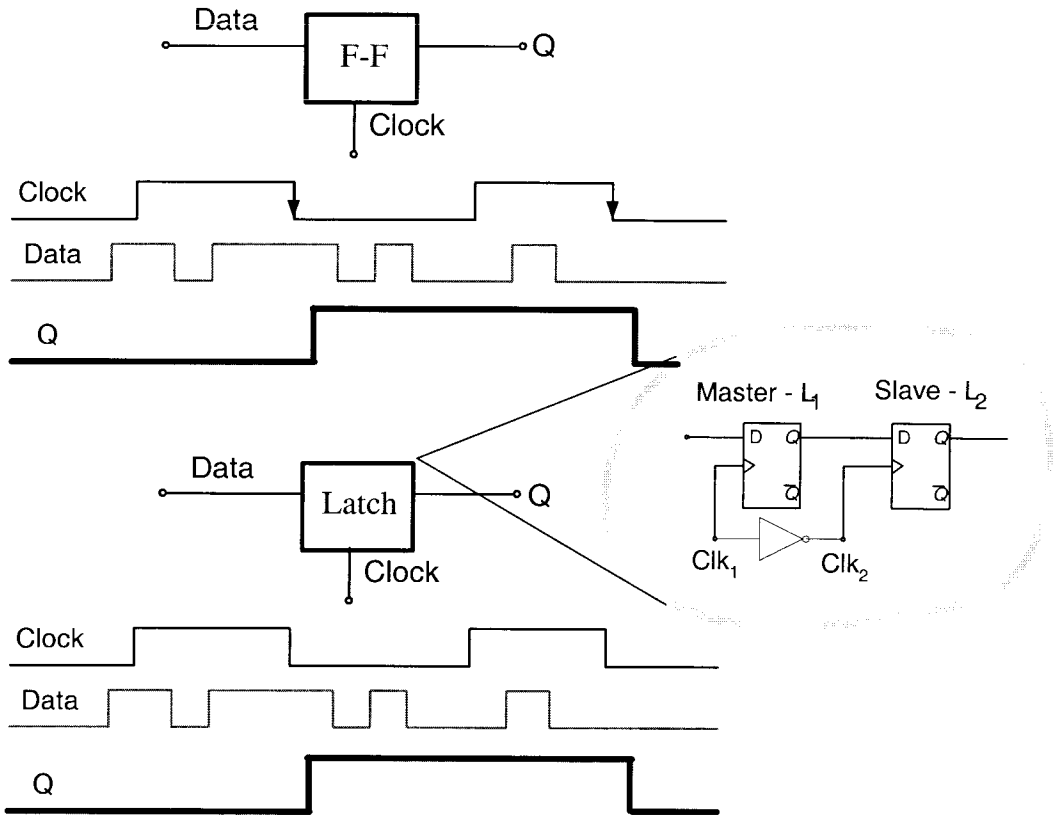
(a) Early version of a flip-flop; (b) PDP-8 direct set-reset sequential element

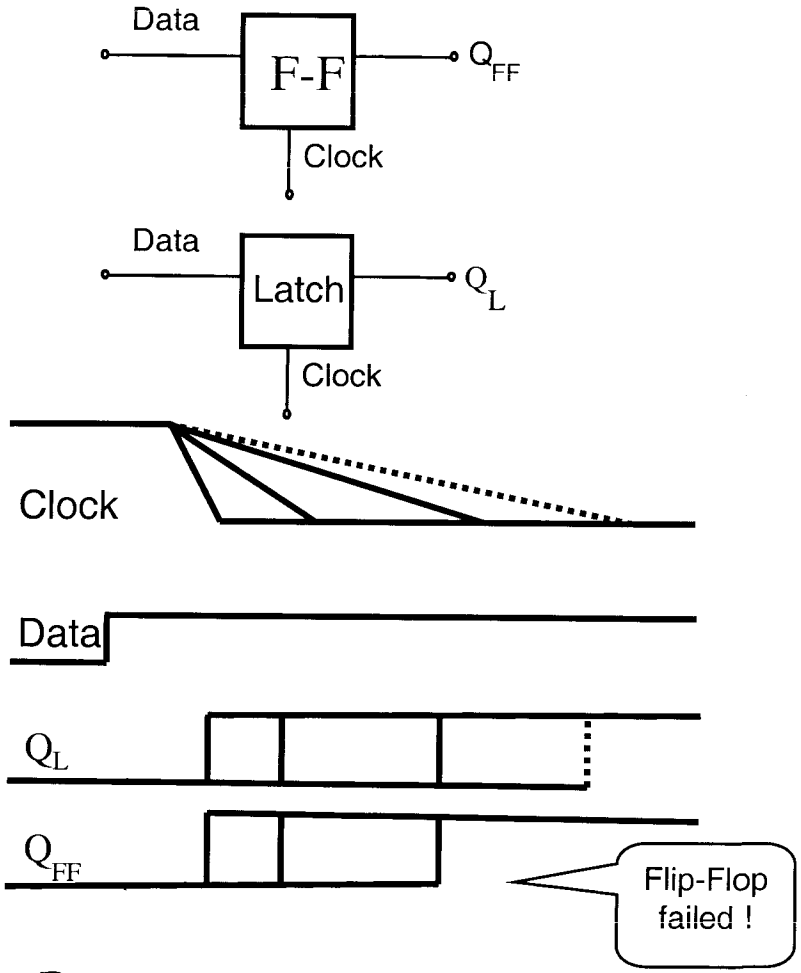
Difference between Flip-flop and M-S Latch



(a) General flip-flop structure; (b) general M-S latch structure

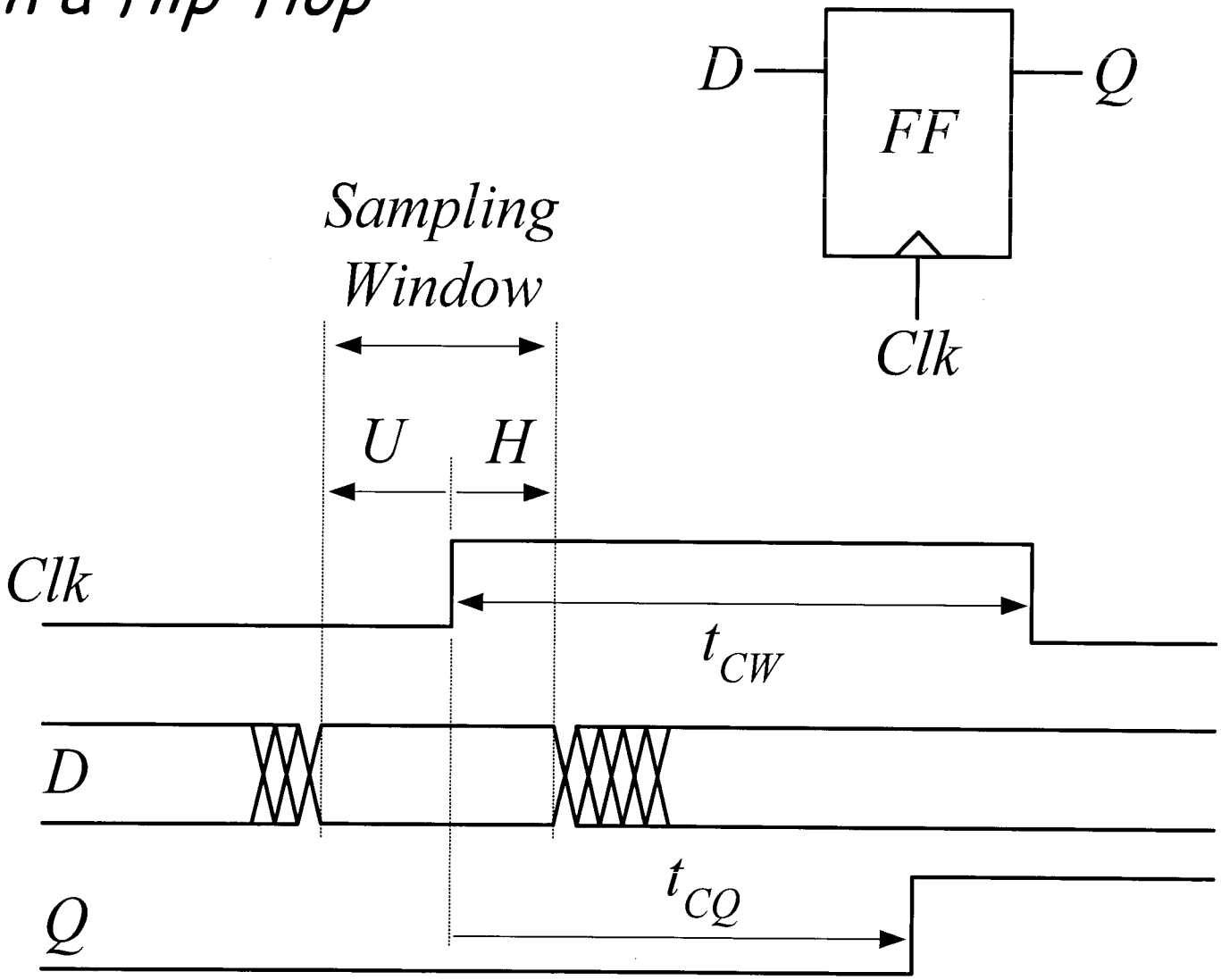
Black-box view of the Flip-flop and M-S latch





Experiment causing the flip-flop to fail while the M-S latch is still operational

Setup time, hold time, sampling window and clock width in a flip-flop

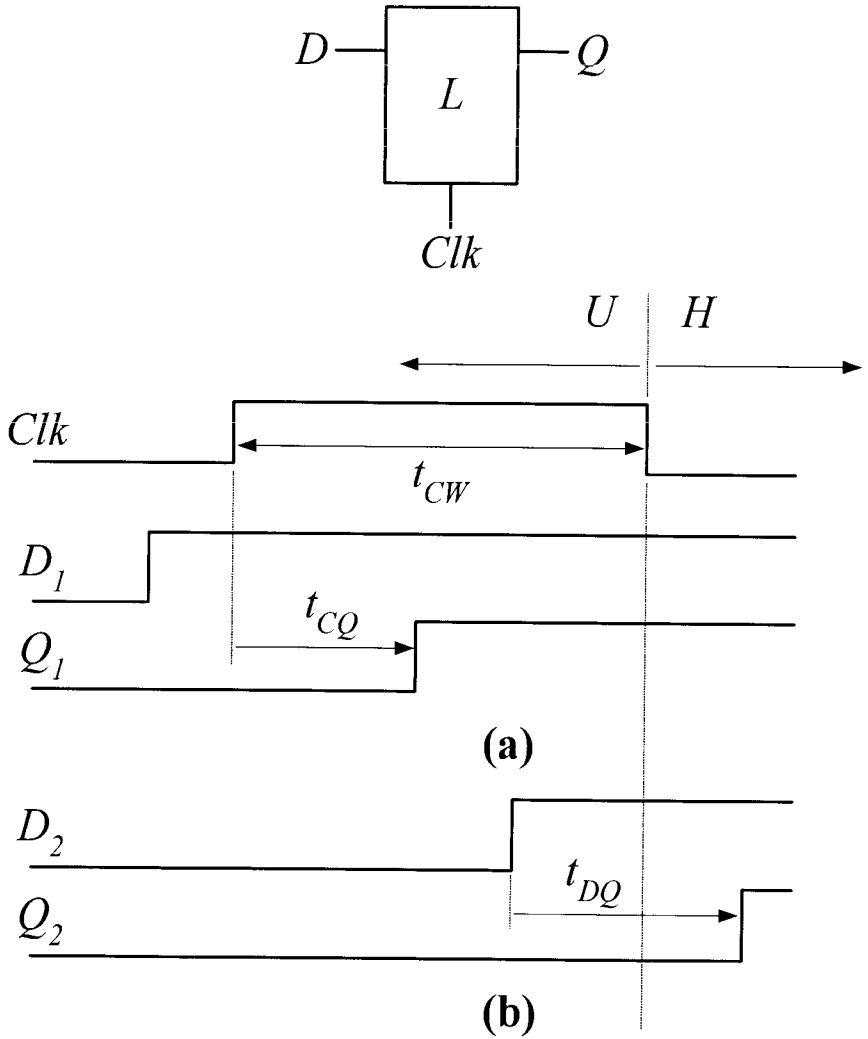


Latch: setup and hold time

Unlike Flip-Flop, Latch has two situations:

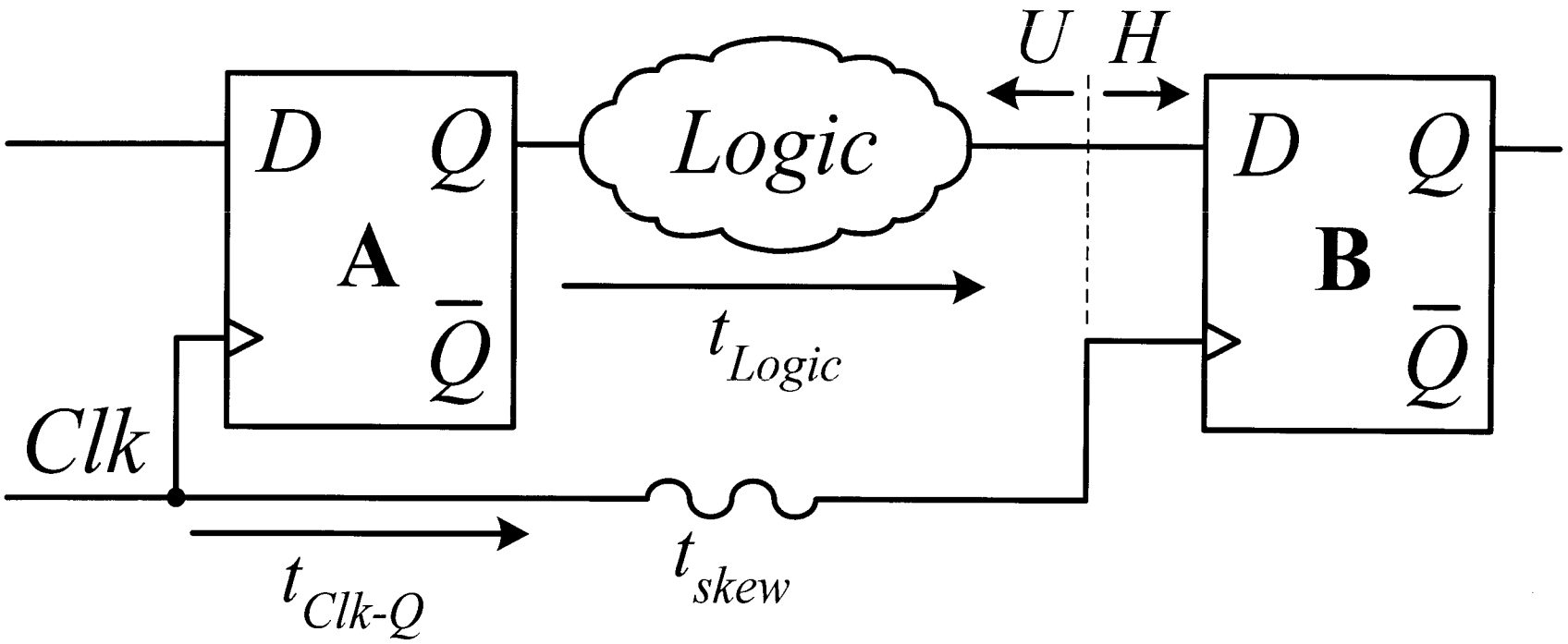
(a) Data is ready – waiting for the clock

(b) Latch is open – data arrives during the active clock signal



(a) early data D1 arrival; (b) late data D2 arrival

Illustration of a data path



Timing in a digital system using a single clock and flip-flops