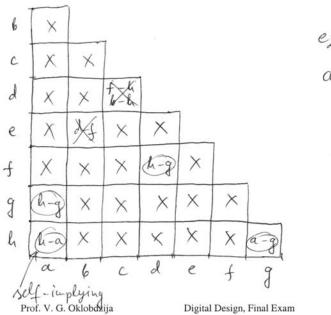
#### PROBLEM No.1 (15 points)

Reduce the following state table to a minimum number of states:

Present State	Next State		Output Z		
Sn	Sn+1				
	X=0	X=1	X=0	X=1	
a	h	С	1	0	
b	С	d	0	1	
С	h	b	0	0	
d	f	h	0	0	
e	С	f	0	1	
f	f	g	0	0	
g	g	С	1	0	
h	a	С	1	0	

- a) [10] Write the resulting state table. Determine the equivalent states show them !
- b) [3] Draw the resulting state diagram with all states, transitions and outputs!
- c) [2] Mark the transitions that are producing Z=1 as an output on the state diagram (circle them !)



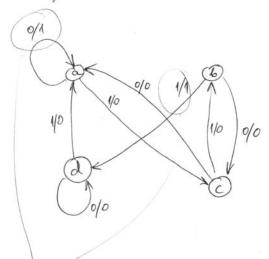
equivalent states: a = g = h d = f e = b

### (extra space for Problem 1)

new table:

Su	Sent	1	2	1
	X=0	x=1	X=0	x=1
a	a	С	1	0
L	C	d	0	1
C	a	6	O	0
d	d	a	0	0

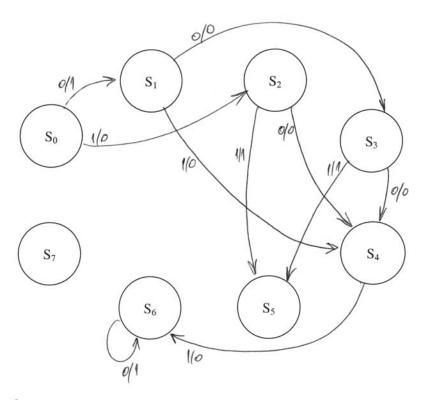
# state diagram:



Here transitions produce 2=1

#### Problem 2.

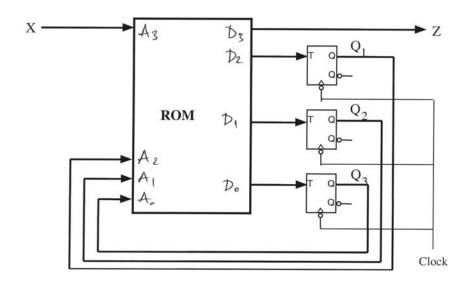
correction: There is also a transition from S5 to S0 for X/Z = 0/0 and 1/0. Also, there is a transition from S4 to S5 for X/Z = 0/1.



- Mealy FSM
- problems:

• SG - can't get out from SG

• S7 - after powerup > undefined transition

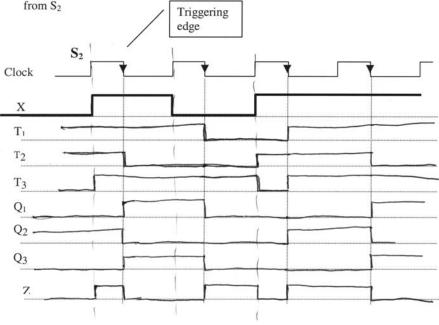


Address A3 A2 A1 A0	Content of ROM D3 D2 D2 D0	next	1
0000	1001	001	
0001	0010	011	
0010	0110	(00	
0011	0111	100	$\top$
0100	1001	101	
0101	0101	000	
0110	1000	110	7
0111	x x x x	XXX	
1000	0010	010	T
1001	0101	100	T
1010	4 ( 1	101	
1011	1110	101	T
1100	0010	110	T
1101	0101	000	+
1110	XXXX	Xxx	+
1111	X X X X	Xxx	-

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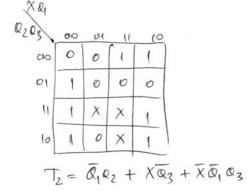
Digital Design, Final Exam

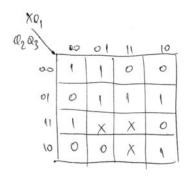
c) [15] Draw a timing diagram for the change of the first four states starting from S<sub>2</sub>



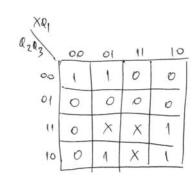
- d) Suppose the ROM in part a) is to be replaced by a PLA:
  - [6] Write **minimal form** equations for the inputs to the T flip-flops, called respectively  $T_1$ ,  $T_2$  and  $T_3$ ?
  - [2] Write an equation for the output Z that can be realized as part of the PLA

XQ	the PLA.			
Q2Q3	00	01	Įŧ	10
00	0	0	0	0
01	0	1	(	1
u	1	X	×	1
10	ţ	0	X	1



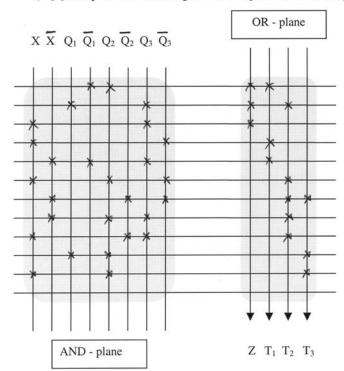


$$T_3 = Q_1 Q_3 + \overline{\chi} \overline{Q_2} \overline{Q_3} + \chi Q_2 \overline{Q_3} + \chi \overline{Q_2} \overline{Q$$



$$\mathcal{Z} = Q_1 Q_2 + X Q_2 + \overline{X} \overline{Q}_2 \overline{Q}_3$$

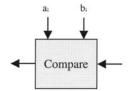
e) [3] Complete the "stick-diagram" PLA representation of the part d).



correction: In the last row of the table (for  $G_i = A_i = B_i = 1$ ),  $G_{i+1}$  should be 1 instead of 0.

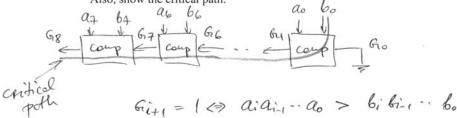
#### PROBLEM No. 3 (15 points)

Design an iterative network for comparing two unsigned binary numbers. These numbers are designated as:  $a = a_n a_0$ ,  $b = b_n b_0$ . The comparator checks if a > b! A typical cell for the comparator is shown:

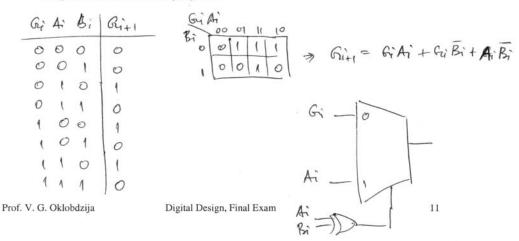


Note that there is a signal propagating between the cells. What is the function of that signal? How would you use it?

(a.) [5] Draw a schematic of a comparator comparing two 8-bit words using these cells. Explain how it works and connect any signals that need to be connected. Also, show the critical path.



(b.) [10] Derive the logic inside this cell and write equations for this logic. Show the most efficient logic implementation for this comparator cell (a cell can be realized using one MUX and one logic gate).



## Problem 4.

(extra space for Problem 4)

