UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

**EEC180A** **DIGITAL SYSTEMS I**

# Lab 3: COMBINATIONAL NETWORK DESIGN USING ALGEBRAIC SIMPLIFICATION

The purpose of this lab is to reinforce the topics which are being covered in the lectures and textbook regarding the application of Boolean algebra to combinational network design. You will verify your combinational network designs using the Altera design system through schematic capture and functional simulation.

## Preparation

- Design the two combinational networks specified in the write-up. Turn in your design, including your algebraic simplification of the networks, to your TA at the *beginning* of your lab period.

## Part 1

1. Design the combinational network described in Problem 5.19 of the text (Roth, Fundamentals of Logic Design, Fourth Edition, p. 102). The problem statement is replicated below.

   > A combinational switching network has four inputs (A, B, C, and D) and one output Z. The output is 1 iff the Gray coded digit represented by ABCD is less than 5. Design the network using two AND gates and one OR gate. Assume that each gate has a maximum of two inputs so that it will be necessary to partially factor your logic equation before you realize it.

   The following table shows the complete 4-bit Gray code and the corresponding Z outputs in order to eliminate confusion regarding the problem specification. Be sure to use algebraic simplification to simplify your network equations. Show your work.

| Decimal (Hex) equivalent | Gray code (A B C D) | Output (Z) |
|---|---|---|
| 0 | 0000 | 1 |
| 1 | 0001 | 1 |
| 2 | 0011 | 1 |
| 3 | 0010 | 1 |
| 4 | 0110 | 1 |
| 5 | 0111 | 0 |
| 6 | 0101 | 0 |
| 7 | 0100 | 0 |
| 8 | 1100 | 0 |
| 9 | 1101 | 0 |
| 10 (0xA) | 1111 | 0 |
| 11 (0xB) | 1110 | 0 |
| 12 (0xC) | 1010 | 0 |
| 13 (0xD) | 1011 | 0 |
| 14 (0xE) | 1001 | 0 |
| 15 (0xF) | 1000 | 0 |

2. Use the Altera schematic capture tool to enter your combinational network design. You may use inverters (NOT component) to generate the complements of input signals, as needed. Otherwise, you

may only use the number of logic gates specified in the problem statement. Perform a functional simulation to verify that your design functions as specified. Print your schematic and simulation output.

Hint: You can group your inputs and specify a Gray code input sequence using the following commands:

- Highlight the input signals in the waveform editor.
- Select Enter Group… (Node menu) and specify a name for the group. Note that the order that the signals are listed (top to bottom) reflects the MSB to LSB ordering in the group. Thus, you should order your signals so that they are listed A to D, with A on top and D on bottom. Re-ordering signals is simple – just select the node icon and drag the signal to its desired location.
- With the group highlighted, click the right mouse button to bring up a pop-up menu. Then select Overwrite > Count value… and click on the Gray code button.
- There is also a "Display Gray Code Count As Binary Count" option in the Enter Group… dialog box. If you select this button, your simulation inputs will be displayed as the decimal equivalent of the Gray code as shown in the table above.

**Part 2**

1. Design the combinational network described in Problem 5.20 of the text (Roth, Fundamentals of Logic Design, Fourth Edition, p. 102). The problem statement is replicated below.

   > A combinational switching network has four inputs (A, B, C, and D) and one output Z. The output is to be 0 iff two or more inputs are 1. Design the network using four AND gates and three OR gates. Assume that each gate has a maximum of two inputs so that it will be necessary to partially factor your logic equation before you realize it.

   Show your work in simplifying the network equation.

2. Use the Altera schematic capture tool to enter your combinational network design. You may use inverters (NOT component) to generate the complements of input signals, as needed. Otherwise, you may only use the number of logic gates specified in the problem statement. Perform a functional simulation to verify that your design functions as specified. Print your schematic and simulation output.

**Lab Report**

Each individual will be required to submit a lab report. Be sure to include the following items in your lab report:

- Lab cover sheet with TA verification for circuit simulation
- Graded pre-lab
- Altera schematics and simulation waveforms for the two combinational networks.