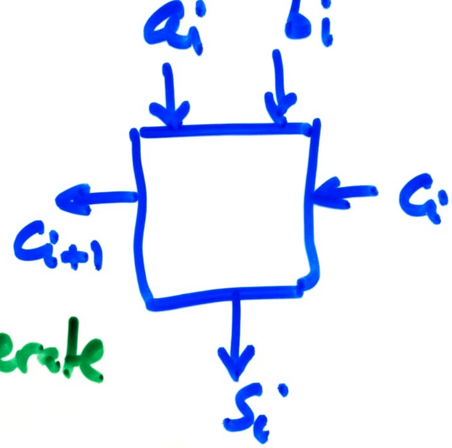
inputs			outputs	
a_i	b_i	c_i	s_i	c_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

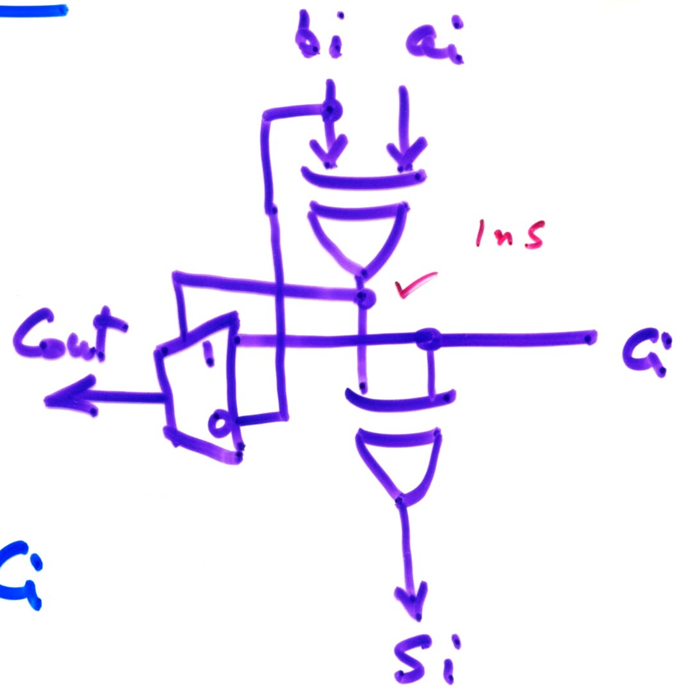
generate

propagated



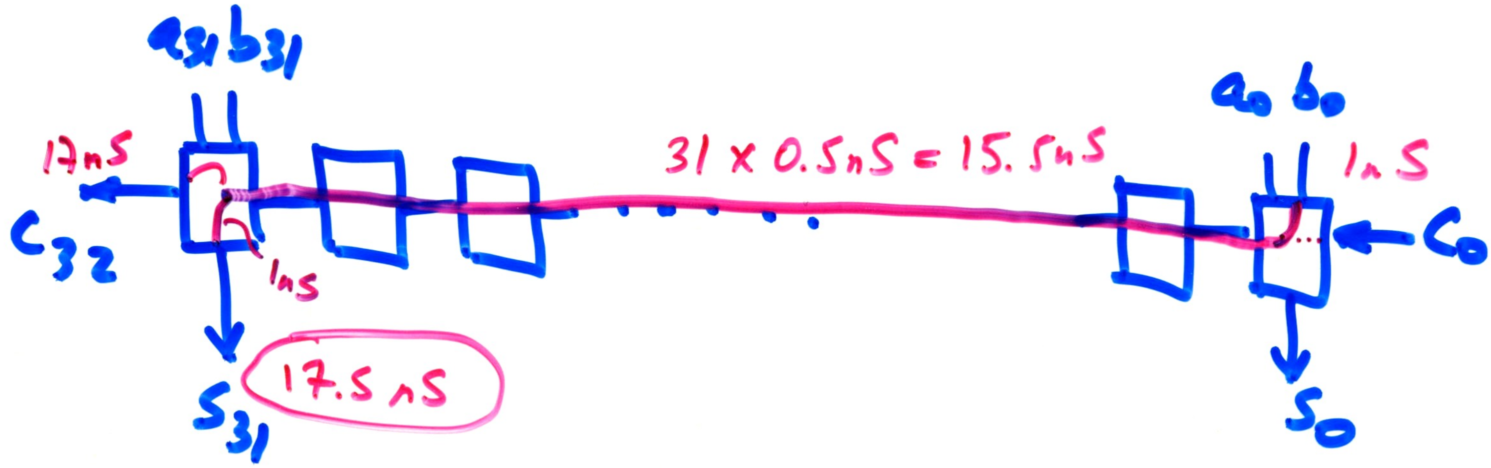
$p_i = a_i \oplus b_i$

$g_i = a_i b_i$



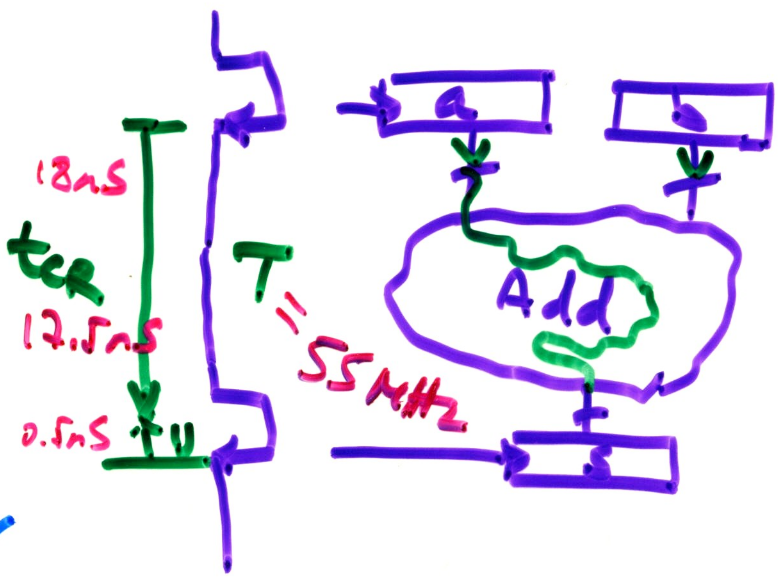
$$C_{out\,(i+1)} = g_i + p_i \cdot c_i$$

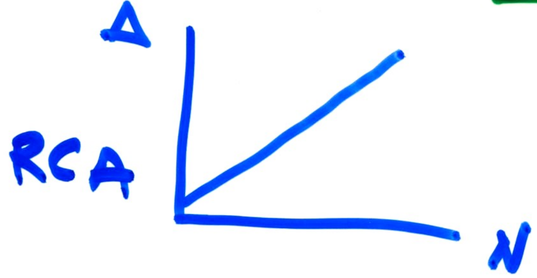
$$c_{i+1} = a_i b_i + a_i c_i + b_i c_i$$



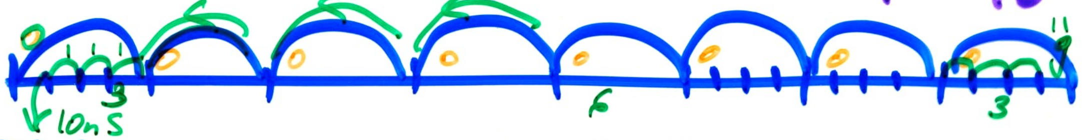
XOR = 1nS

MUX = 0.5nS





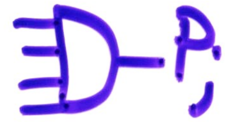
CSKA



CSA

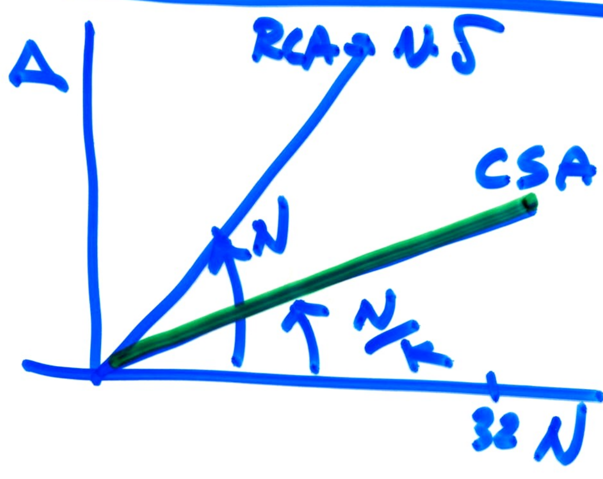
$\Delta = 12\,nS$

$$P_j = P_i P_{i+1} P_{i+2} P_{i+3} = 1$$

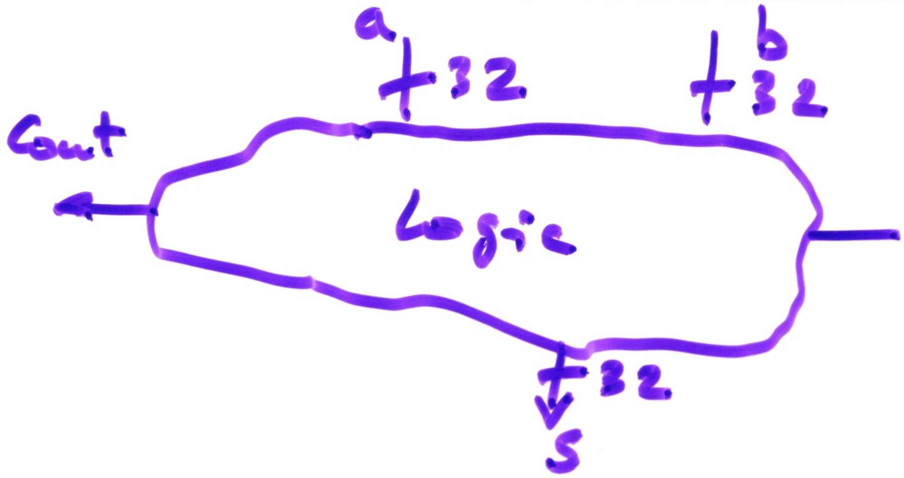


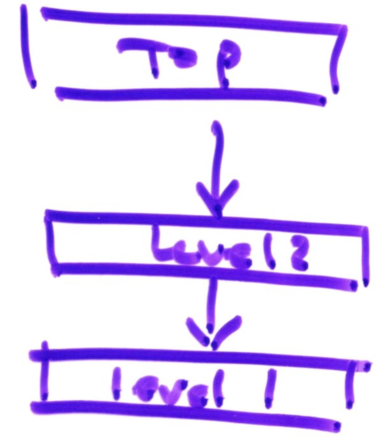
RCA $\Delta = N \cdot \delta$

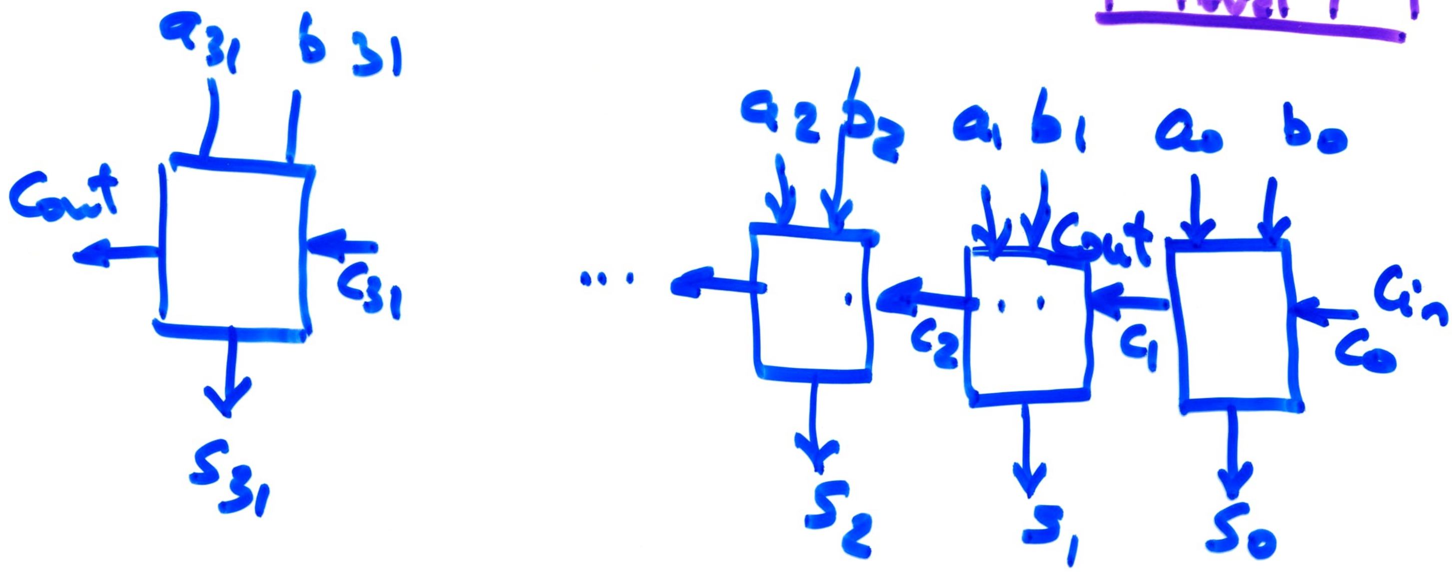
CSK $\boxed{\Delta = 2(k-1) + \left(\frac{N}{k} - 2\right)}$ $\frac{N}{k} \begin{matrix} = 32 \\ = 4 \end{matrix}$ $= 8$



Circuits for Arithmetic <C-20>

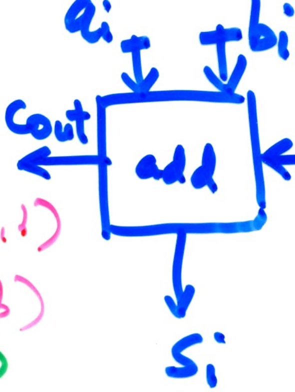


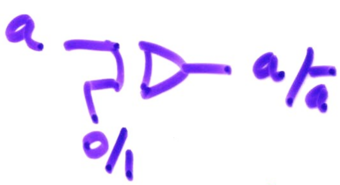


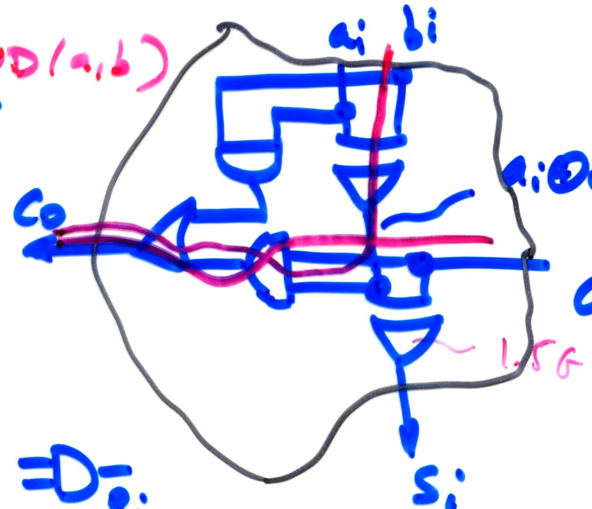


Adders (ALU)

C_i	a_i	b_i	S_i	C_o	
0	0	0	0	0	AND(a,b)
0	0	1	1	0	XOR(a,b)
0	1	0	1	0	
0	1	1	0	1	AND(a,b)
1	0	0	1	0	AND(a,b)
1	0	1	0	1	$\overline{\text{XOR}(a,b)}$
1	1	0	0	1	
1	1	1	1	1	AND(a,b)



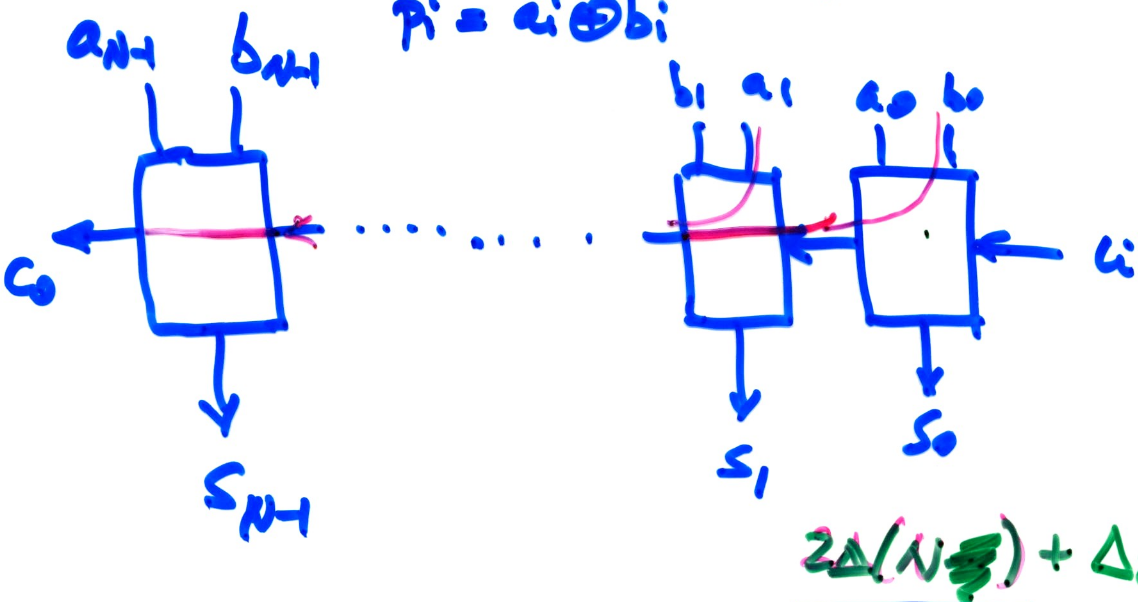




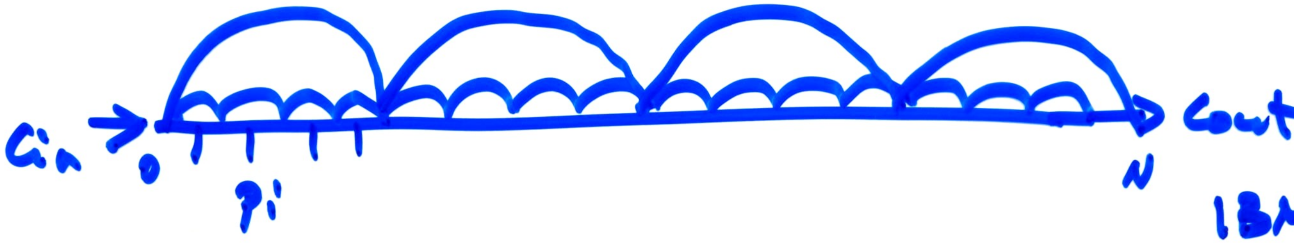
$$C_o = g_i + p_i \cdot C_i$$

$$g_i = a_i b_i$$

$$p_i = a_i \oplus b_i$$



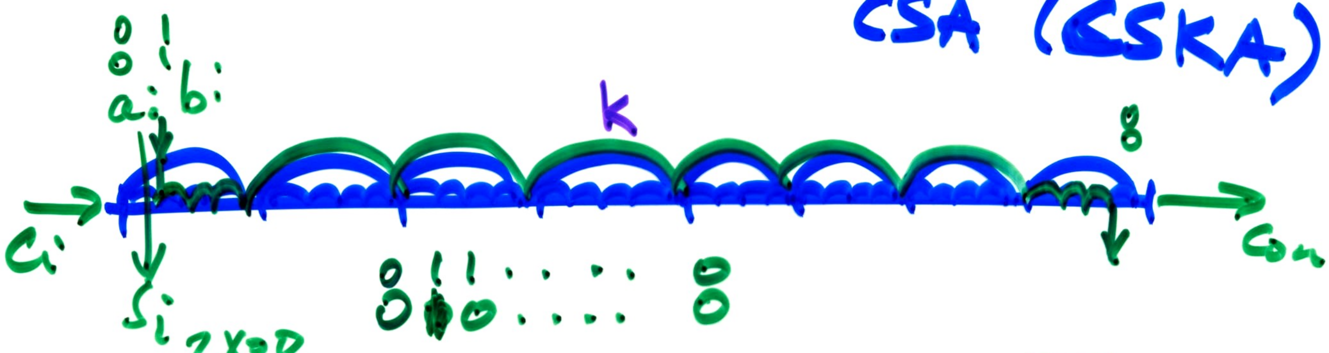
$2\Delta(N) + \Delta_{XOR} = 65\Delta$



IBM $\longrightarrow$ BE

$P_i = p_i p_{i+1} p_{i+2} p_{i+3}$

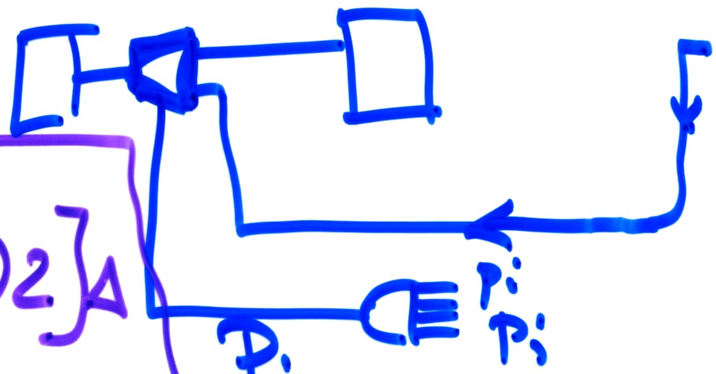
CSA (CSKA)

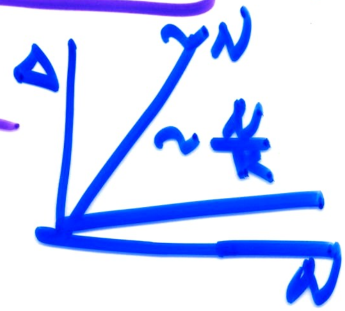


$D = 8\Delta_S$

$$\boxed{D = \left[\left(\frac{N}{k} - 2\right) + (k-1)2\right]\Delta}$$

CSKA



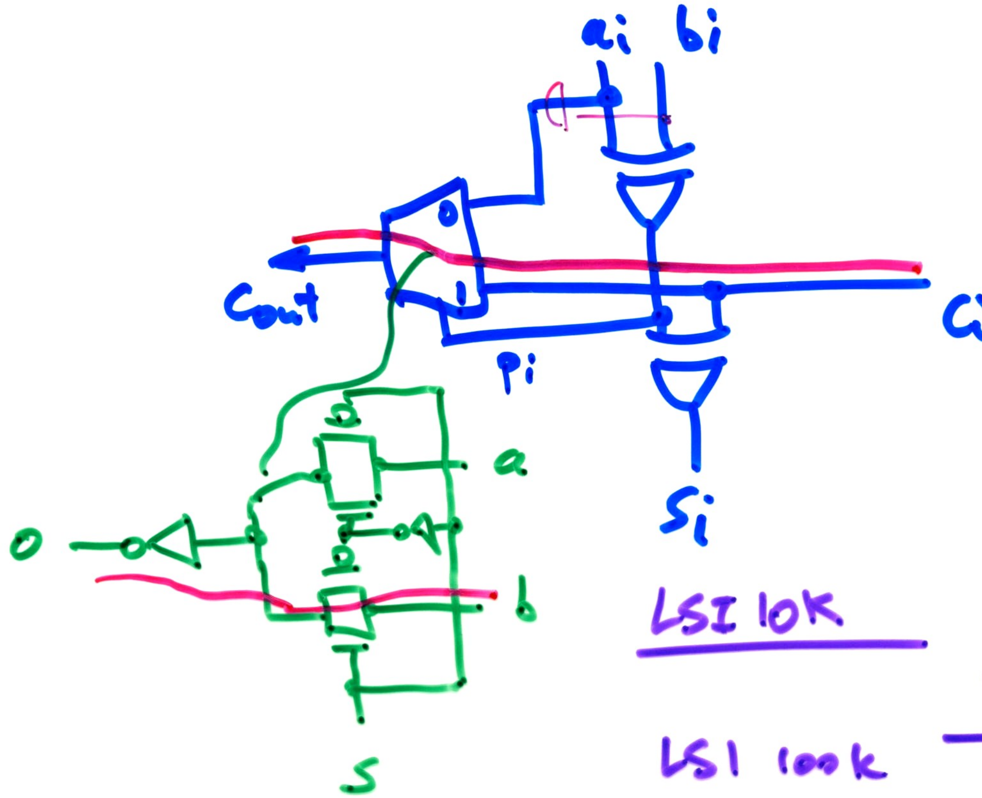


VBA

Earl Barnes (GT)

ARITH '85 Urbana, Ill.

3 pt



LSI 10K 1-2nS

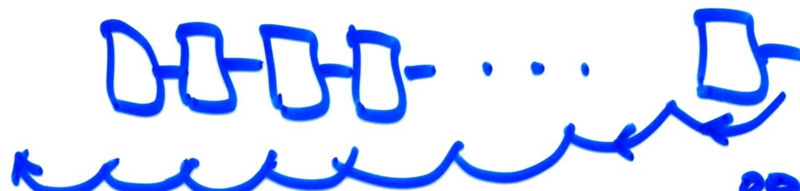
700ps

LSI 100k 400-700ps

150ps

$$\boxed{\text{Delay} = (N-1)\,\Delta_{MUX} + \Delta_{XOR}}$$

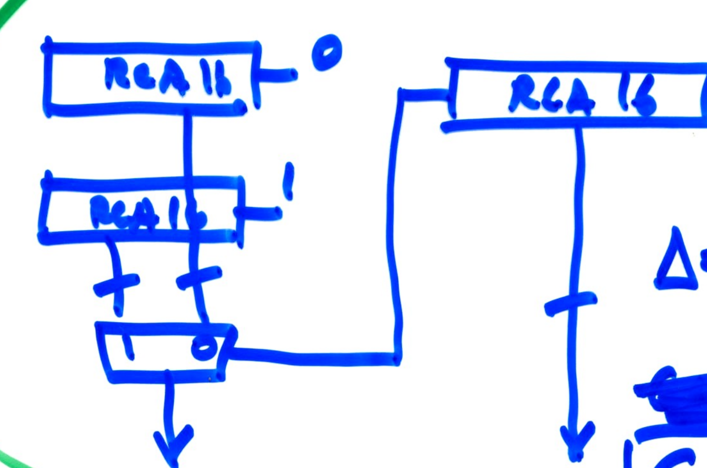
RCA:



0000001
1111111

$D \propto \Delta \cdot N$

1 pt



$\Delta = D_{16} + \Delta_{mux}$

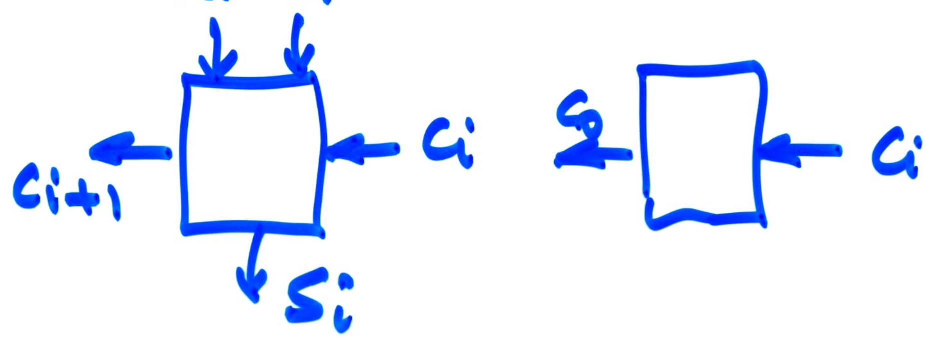
CSA

CSLA

CLA

Arnold Weinberger 1959

IBM NBS

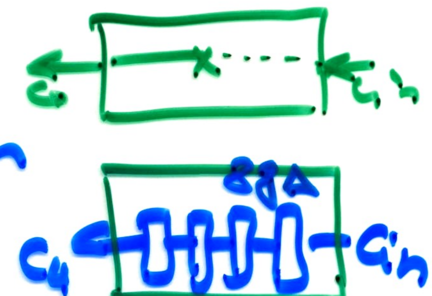


$$c_{i+1} = g_i + p_i c_i$$

$$c_1 = g_0 + p_0 c_{in}$$

$$c_1 = g_1 + p_1 (g_0 + p_0 c_{in})$$

$$= g_1 + p_1 g_0 + p_1 p_0 c_{in}$$

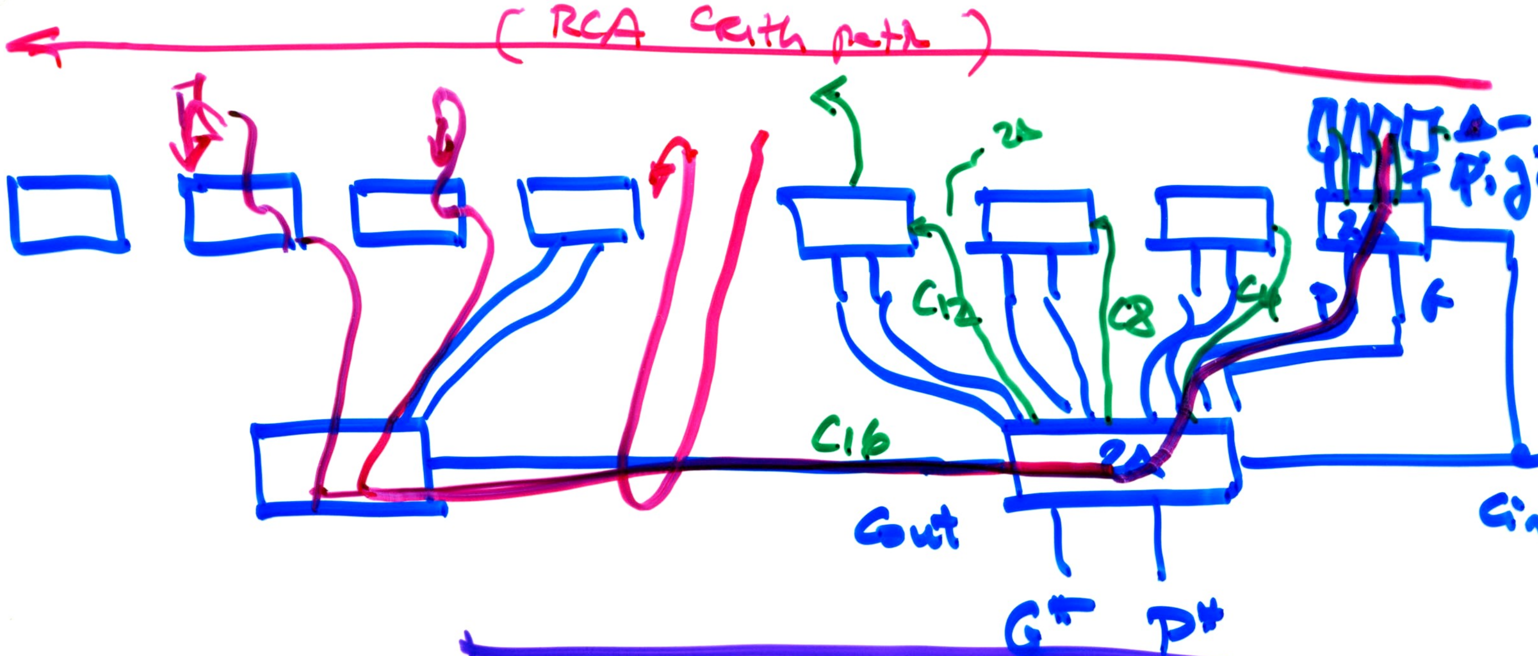


$$\boxed{c_4 = \overbrace{g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0}^{G} + \underbrace{p_3 p_2 p_1 p_0}_{P} \cdot c_{in}}$$

$$c_{i+1} = g_i + p_i g_{i-1} + p_i p_{i-1} g_{i-2} \cdots$$

$$\boxed{c_4 = G + P \cdot c_{in}}$$

$$D = 2\Delta + 2\Delta = 4\Delta$$



$$\boxed{D \approx \alpha\, 2 \log_K(N)}$$ $(k=4)$

Δ ..... $p_i\ g_i$

2Δ ..... $P,\ G,\ c_1, c_2, c_3$ ... $P^* = P_0 P_1 P_2 P_3$

G^*

2Δ ..... P^*, G^*, c_{16}

2Δ ..... c_4, c_8, c_{12}

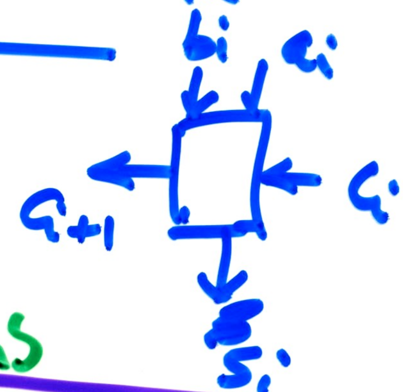
2Δ ...... c_i

Δ ... S_i

10Δ CLA (65Δ RCA, 14Δ CSA)

CLA (1959, Weinberger, A.) Smith

Carry Lookahead

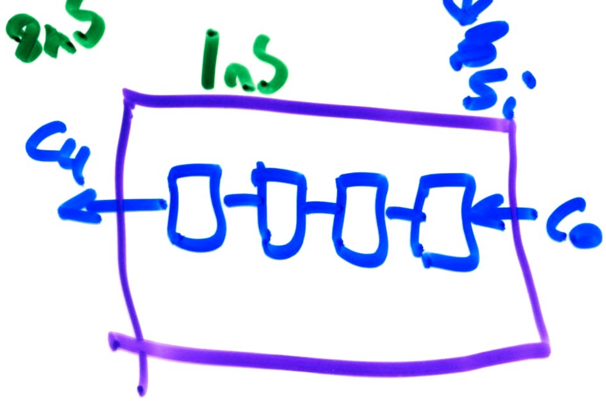


$$C_1 = g_0 + p_0 \cdot C_0$$

$$C_2 = g_1 + p_1 \cdot C_1$$

$$C_3 = g_2 + p_2 \cdot C_2$$

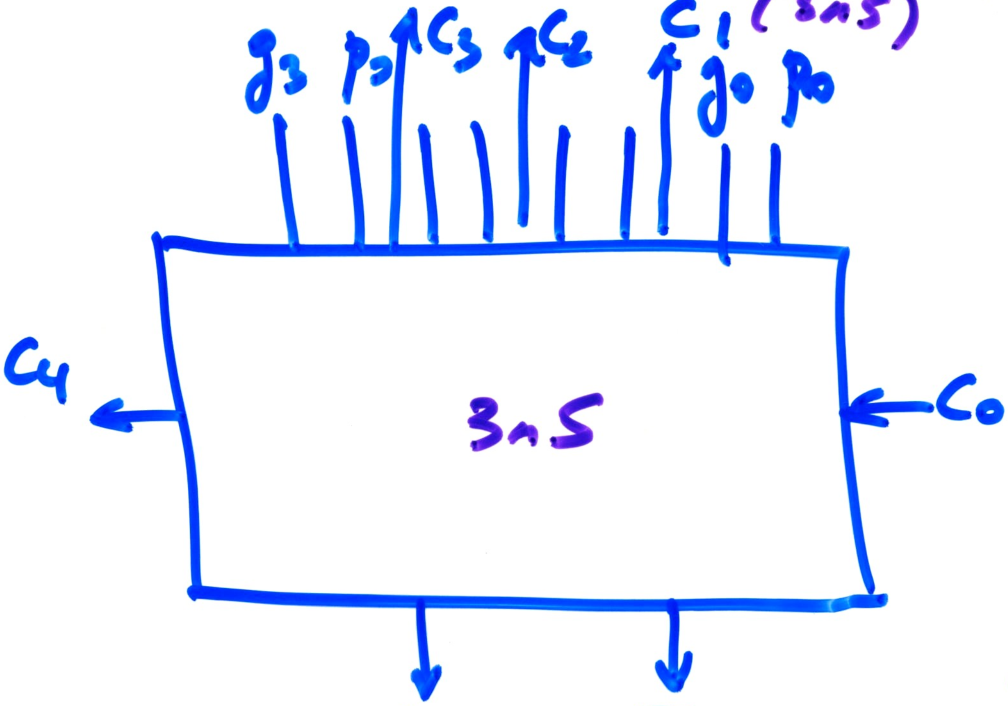
$$C_4 = g_3 + p_3 \cdot C_3$$



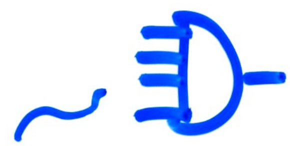
$$C_4 = \underbrace{g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0}_{G} + \underbrace{p_3 p_2 p_1 p_0}_{P} \cdot C_0$$

$$C_4 = G + P \cdot C_0$$

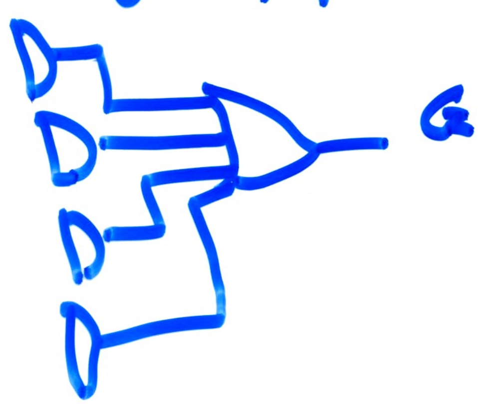
(1)	p_i, g_i	1L	1nS
(2)	P	1L	2nS
(3)	G	2L	3nS
(4)	C_4	2L	5nS



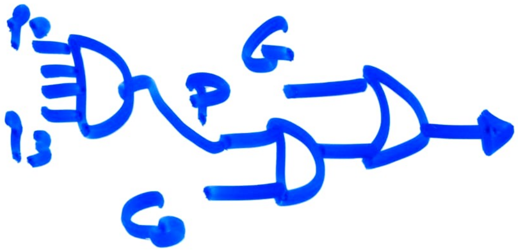
G (2ns) $P = p_0 p_1 p_2 p_3$



$G = g_3 + g_2 p_3 + g_1 p_2 p_3 + g_0 p_1 p_2 p_3$



$C_4 = G + P \cdot C_0$

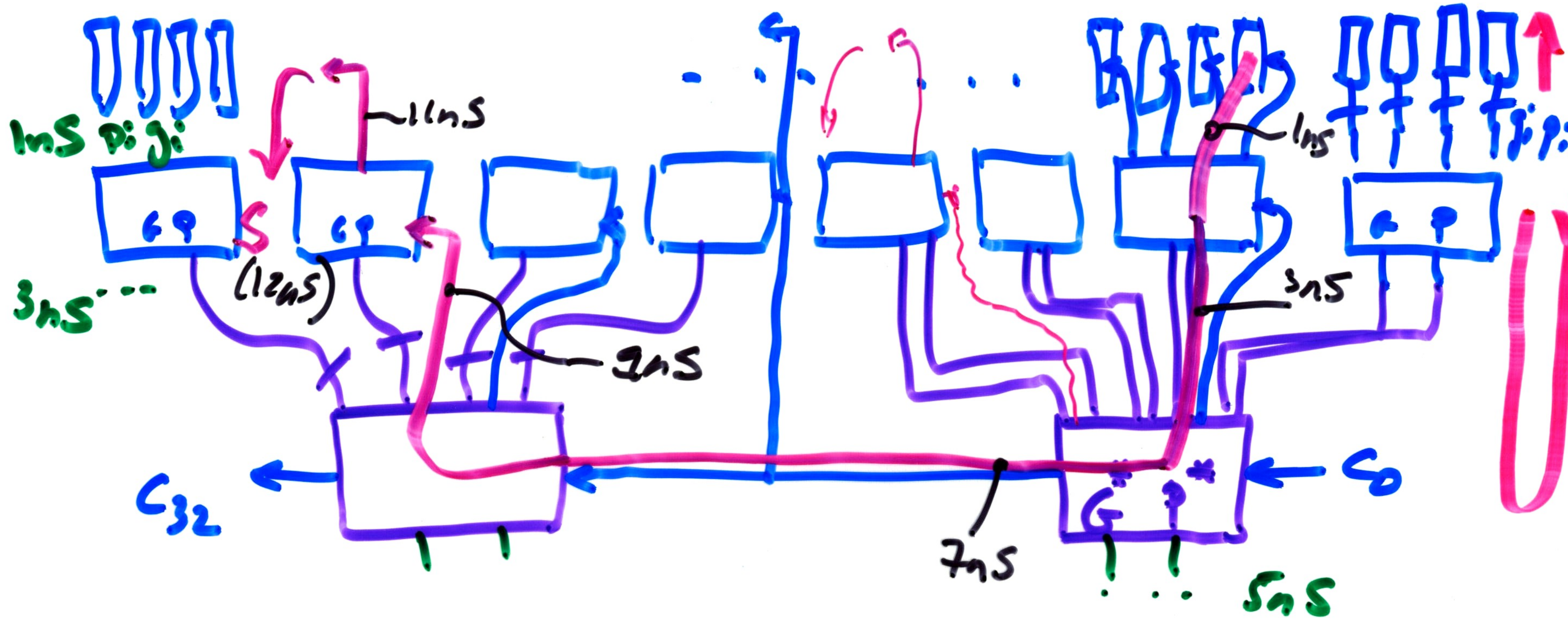


$c_1 = g_0 + p_0 c_0$

$c_2 = \ldots\ldots$

$c_3 = \ldots$

32-bit CLA (Weinberger '59)

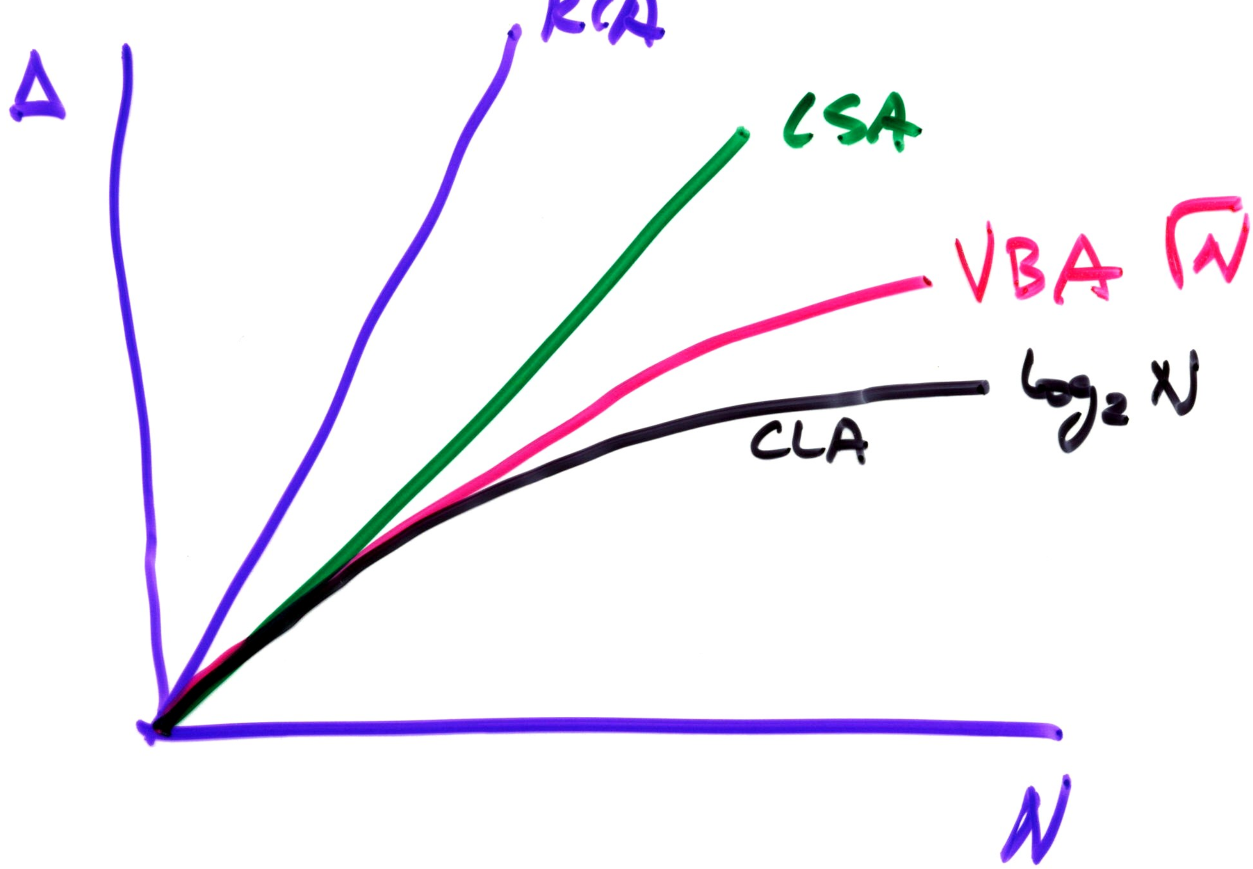


RCA 32 X 2 X 1nS = 64nS

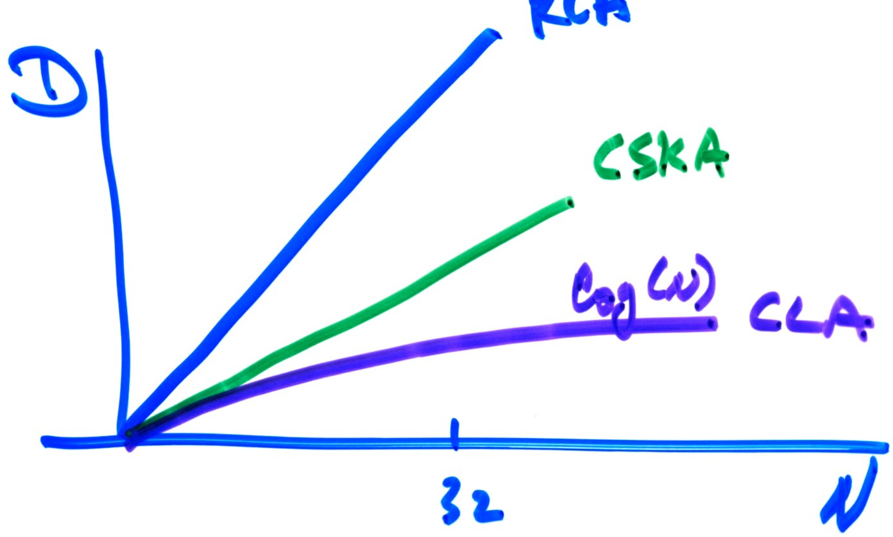
$$c_j = G^* + P^* c_{j+1} \quad 2L \quad (2nS$$

$\boxed{\text{CLA} = 12\text{nS}}$ vs 64nS (RCA)
24nS (CSA)

Depth ~ $\log_2 N$ ~ Δ ~ $k \log_2 N$



RCA
Δ
CSA
VBA √N
log₂ N
CLA
N


RCA
D
CSKA
log(N)
CLA
32
N

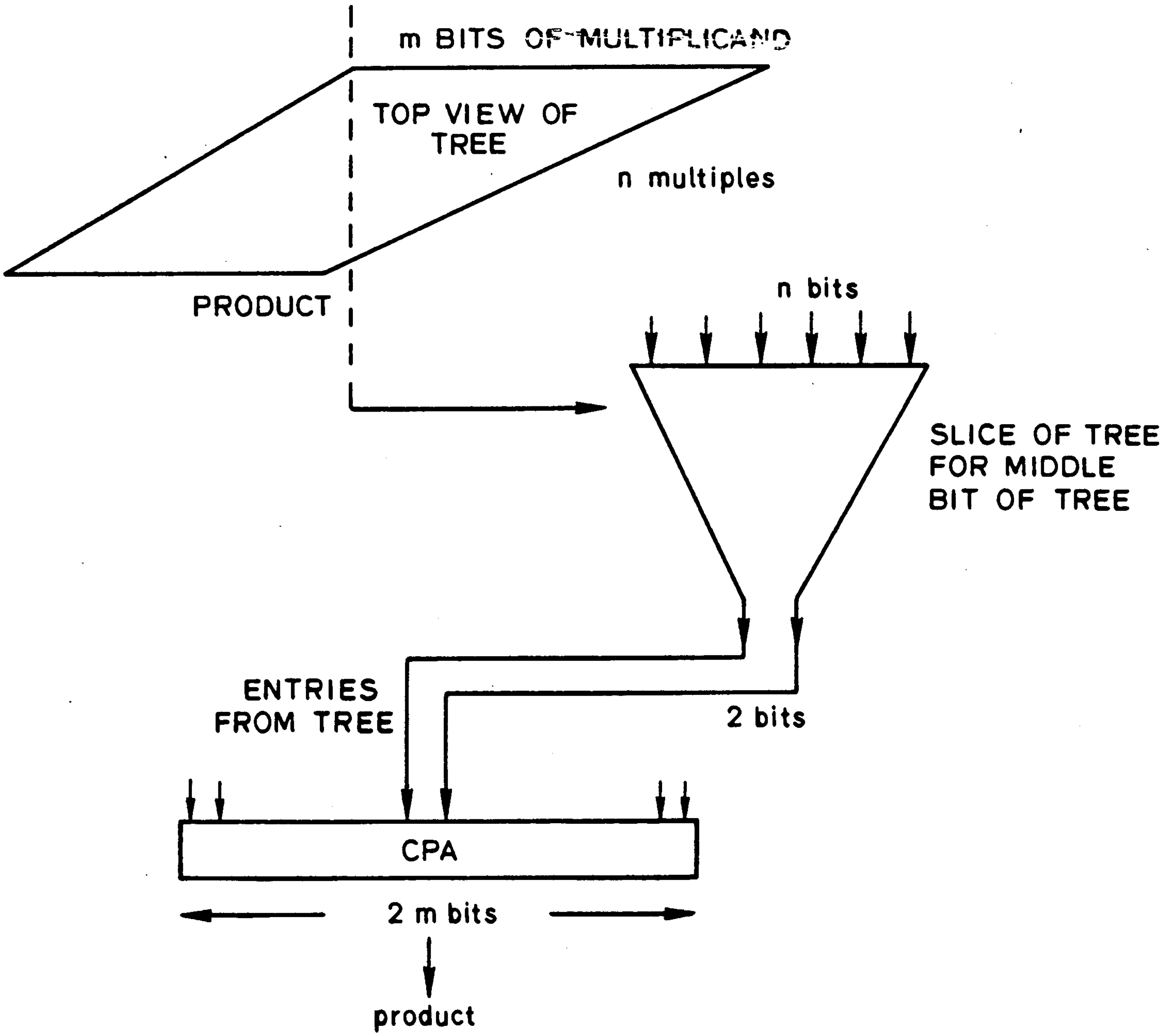
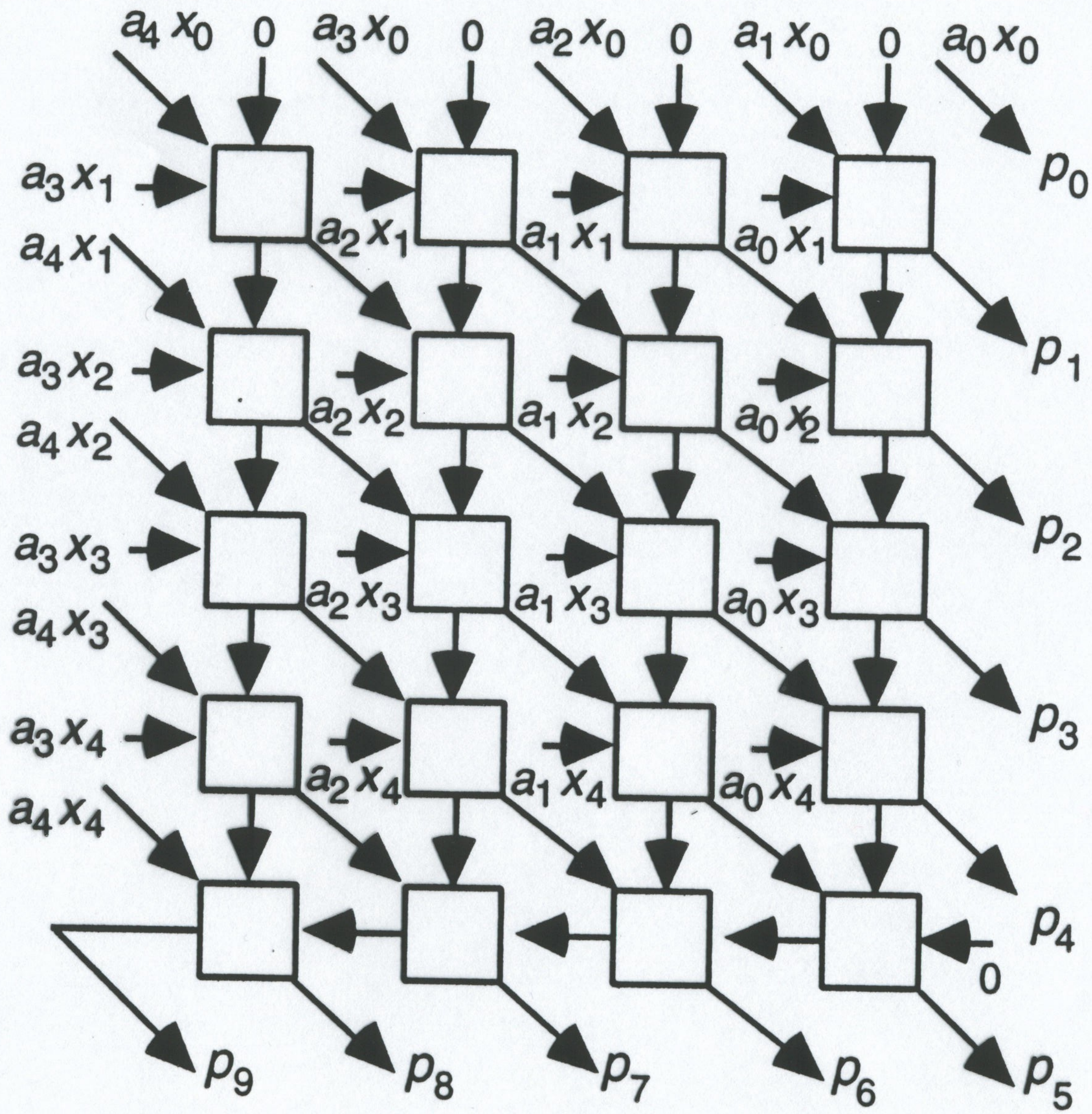


Figure 4–6. Wallace tree



a_4x_0 0 a_3x_0 0 a_2x_0 0 a_1x_0 0 a_0x_0
a_3x_1 a_2x_1 a_1x_1 a_0x_1
a_4x_1
a_3x_2 a_2x_2 a_1x_2 a_0x_2
a_4x_2
a_3x_3 a_2x_3 a_1x_3 a_0x_3
a_4x_3
a_3x_4 a_2x_4 a_1x_4 a_0x_4
a_4x_4
0
p_0 p_1 p_2 p_3 p_4 p_5 p_6 p_7 p_8 p_9

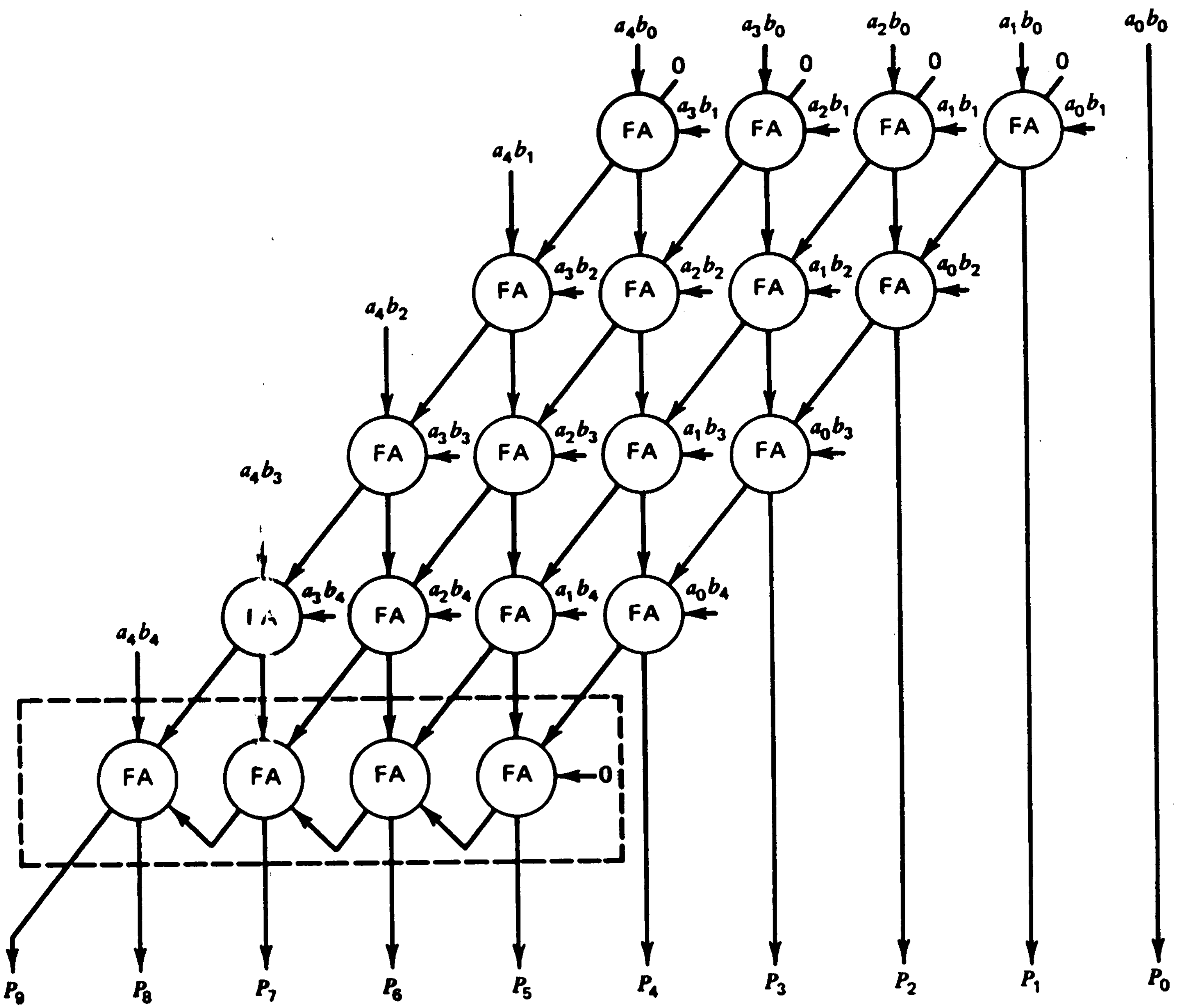


Figure 6.3 The schematic circuit diagram of a 5-by-5 unsigned array multiplier (Braun [5]).

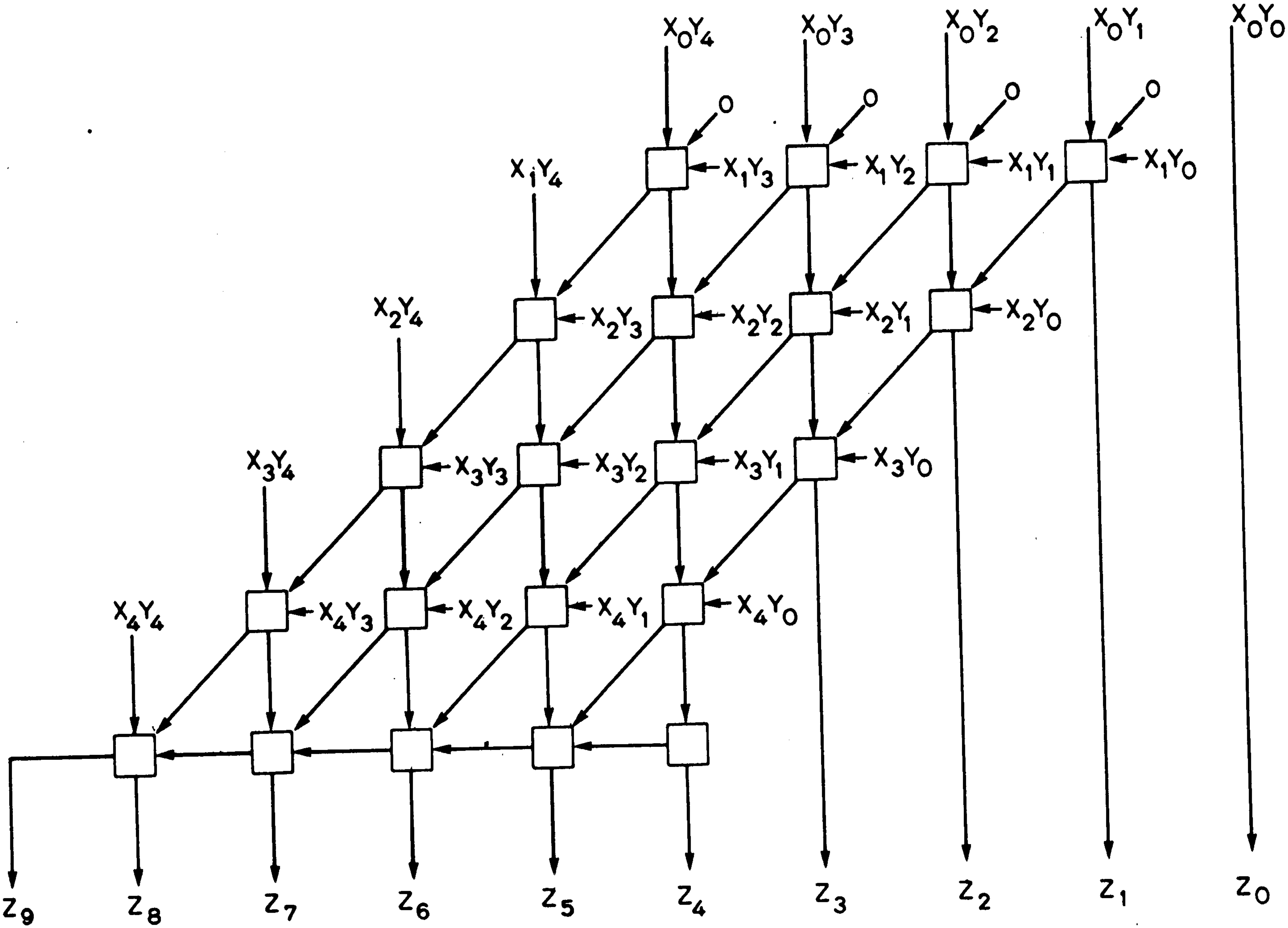


Figure 4–15a. 5 × 5 unsigned multiplication.

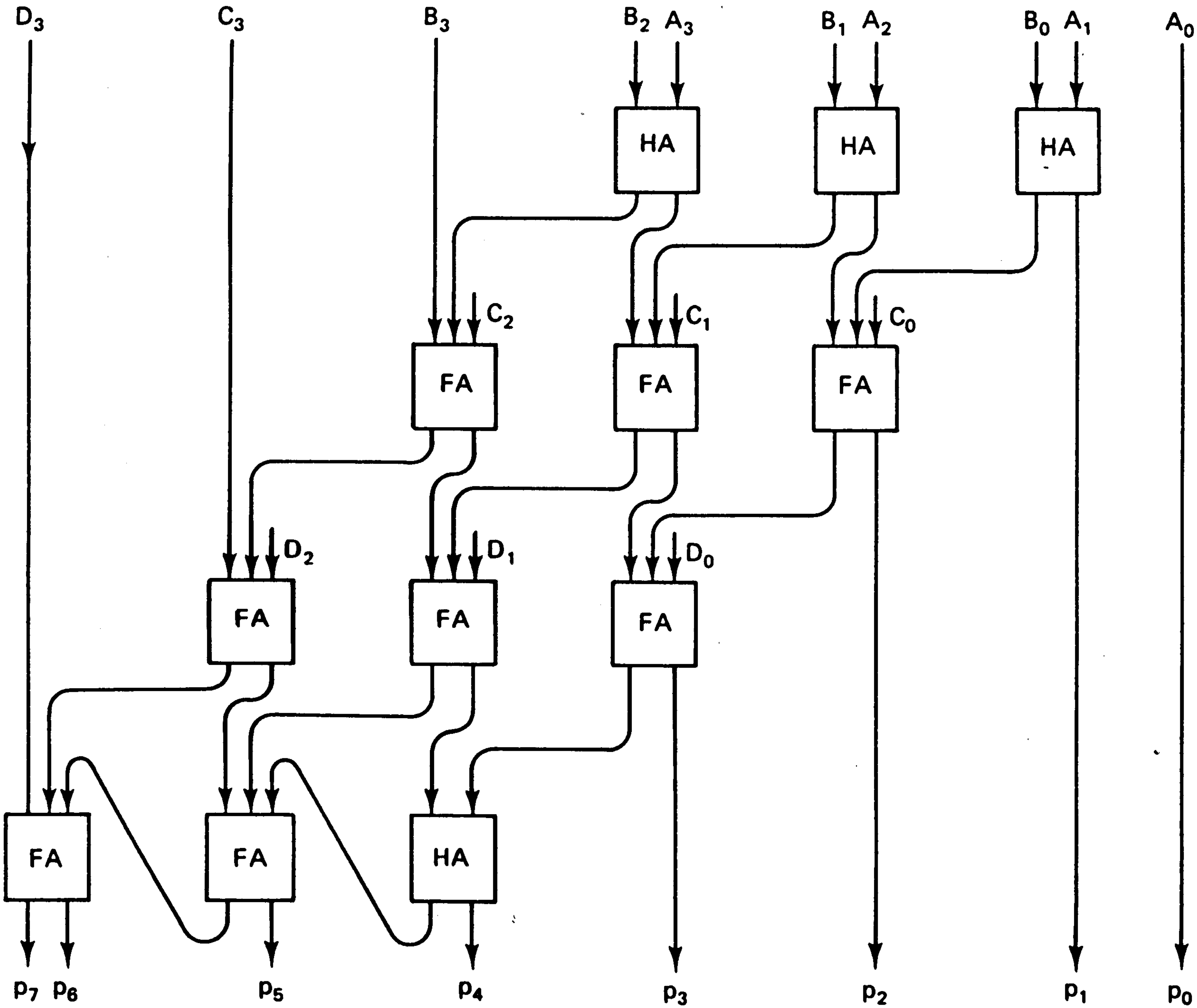


Figure 4.4 Array of half-adders and full-adders for 4-bit $\times$ 4-bit multiplication.