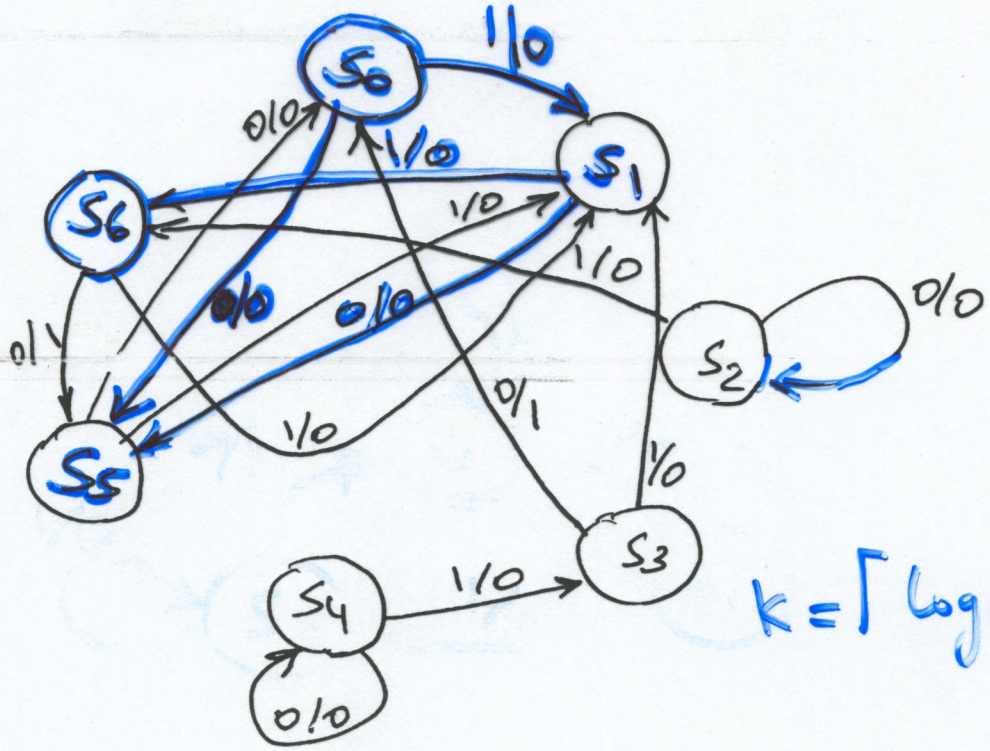
State Reduction :

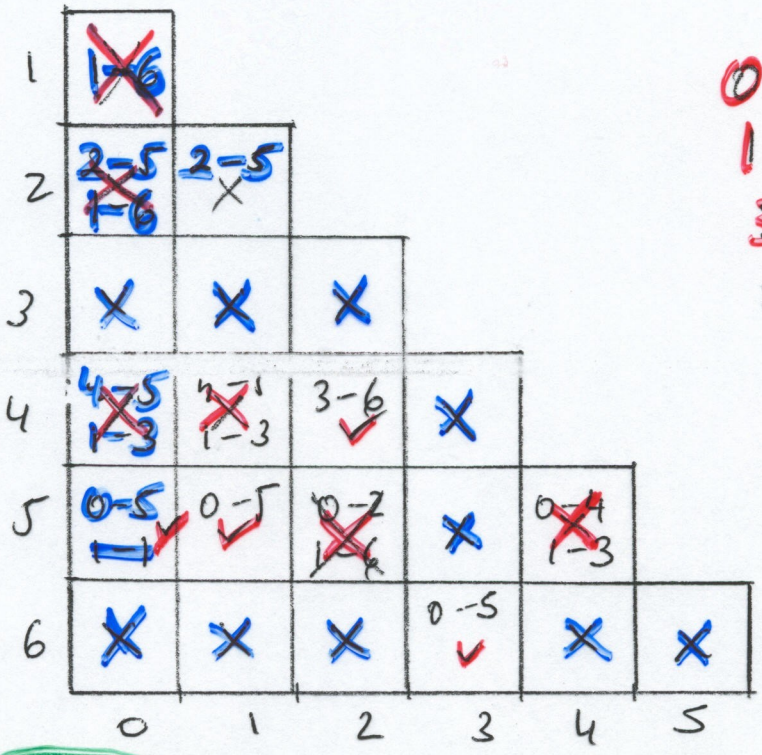
Could this be implemented with fewer states ?

S_n	S_{n+1} x=0	S_{n+1} x=1	Output Y x=0	Output Y x=1
S_0	S_5	S_1	0	0
S_1	S_5	S_6	0	0
S_2	S_2	S_6	0	0
S_3	S_0	S_1	1	0
S_4	S_4	S_3	0	0
S_5	S_0	S_1	0	0
S_6	S_5	S_1	1	0

S_2^*



$k = \lceil \log(N) \rceil$



0≡5
1≡5
3≡6
2≡4

0≡1≡5 = S_0*
2≡4 ≡ S_1*
3≡6 = S_2*

S_n	S_{n+1} X=0	S_{n+1} X=1	Y X=0	Y X=1
S_0	S_0	S_0	0	0
S_1	S_1	S_2	0	0
S_2	S_0	S_0	1	0

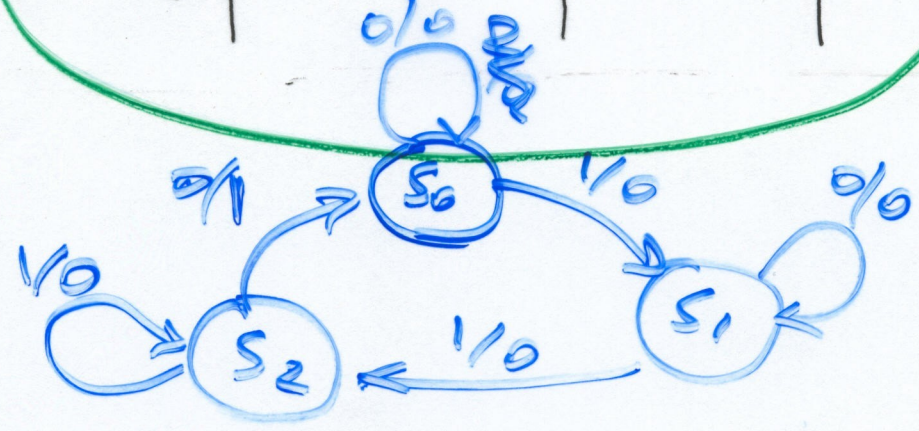


TABLE 13-4
A State Table with Multiple Inputs and Outputs

Present State	Next State X_1X_2 = 00	01	10	11	Present Output (Z_1Z_2) X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

FIGURE 13-15
State Graph for Table 13-4

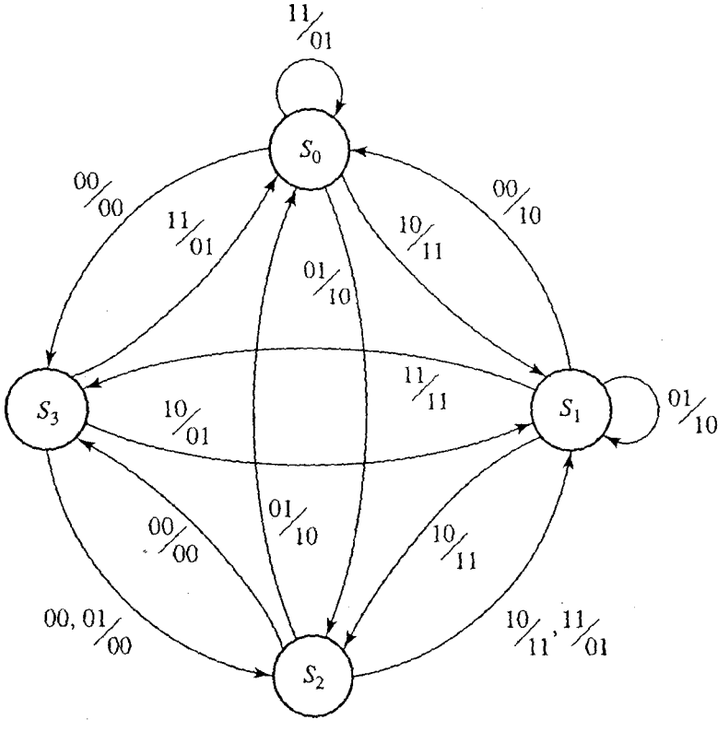


TABLE 13-4
A State Table with Multiple Inputs and Outputs

Present State	Next State $X_1X_2 = 00$	01	10	11	Present Output (Z_1Z_2) $X_1X_2 = 00$	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

FIGURE 13-15
State Graph for Table 13-4

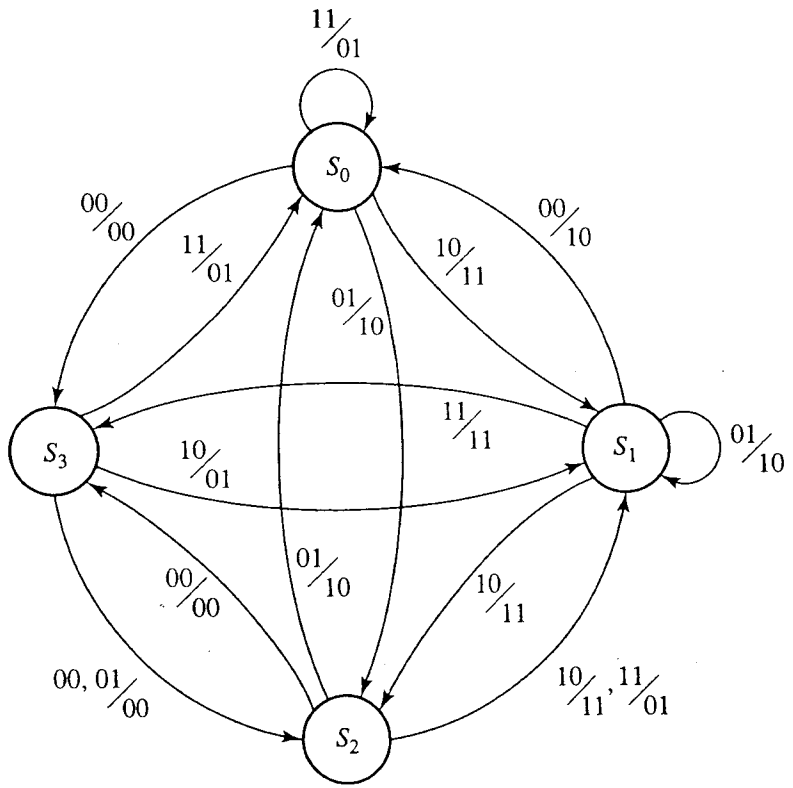
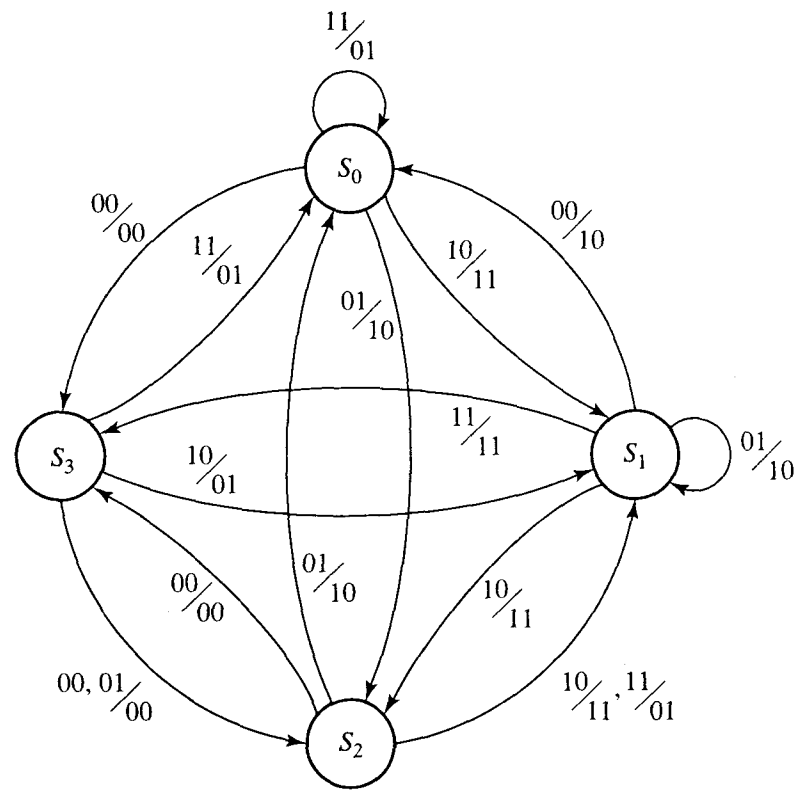


TABLE 13-4
A State Table with Multiple Inputs and Outputs

Present State	Next State $X_1X_2 = 00$	01	10	11	Present Output (Z_1Z_2) $X_1X_2 = 00$	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

FIGURE 13-15
State Graph for Table 13-4



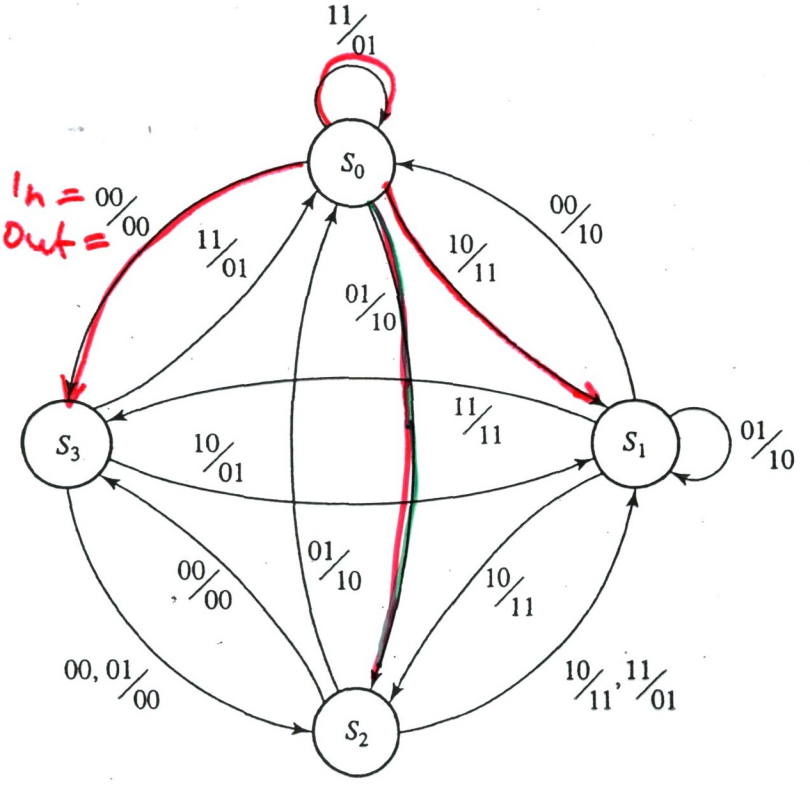
resent a carry (c_i) of 0 and 1, respectively. From the table, c_i is the present state of the sequential circuit, and c_{i+1} is the next state. If we start in S_0 (no carry), and $x_i\, y_i = 11$, the output is $s_i = 0$ and the next state is S_1. This is indicated by the arrow going from state S_0 to S_1.

Table 13-4 shows a state table for a Mealy sequential circuit with two inputs and two outputs. Figure 13-15 shows the corresponding state graph. The notation 00, 01/00 on the arc from S_3 to S_2 means if $X_1 = X_2 = 0$ or $X_1 = 0$ and $X_2 = 1$, then $Z_1 = 0$ and $Z_2 = 0$.

TABLE 13-4
A State Table with Multiple Inputs and Outputs

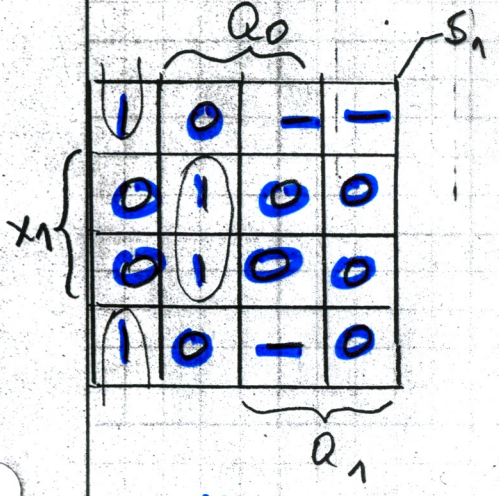
Present State	Next State X_1X_2 = 00	01	10	11	Present Output (Z_1Z_2) X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

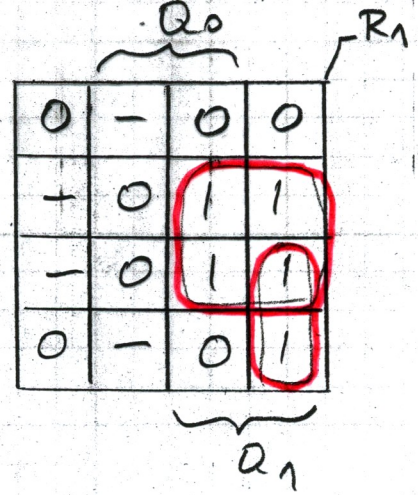
FIGURE 13-15
State Graph for Table 13-4

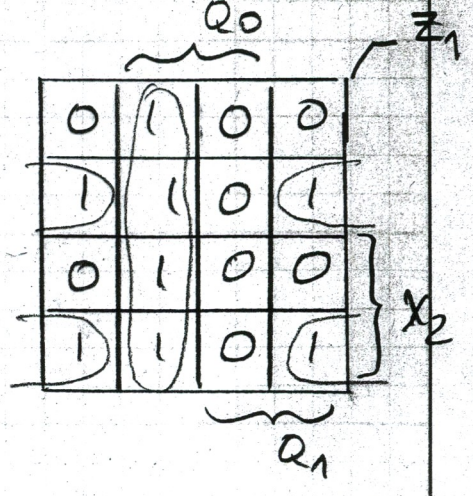


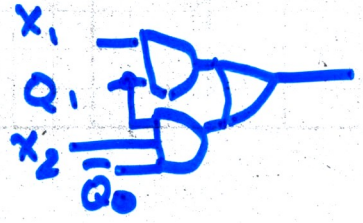
V. Oklobdija | pg. 372 Table 13-4

Input S_n		Current State		Next State S_{n+1}		Output		RS-FF			
X_1	X_2		Q_1^n Q_0^n		Q_1^{n+1} Q_0^{n+1}	Z_1	Z_2	S_1	R_1	S_0	R_0
0	0	S_0	0 0	S_3	1 1	0	0	1	0	1	0
0	0	S_1	0 1	S_0	0 0	1	0	0	–	0	1
0	0	S_2	1 0	S_3	1 1	0	0	–	0	1	0
0	0	S_3	1 1	S_2	1 0	0	0	–	0	0	1
0	1	S_0	0 0	S_2	1 0	1	0	1	0	0	–
0	1	S_1	0 1	S_1	0	1	0	0	–		
0	1	S_2	1 0	S_0	0	1	0	0	1		
0	1	S_3	1 1	S_2	1	0	0	–	0		
1	0	S_0	0 0	S_1	0	1	1	0	–		
1	0	S_1	0 1	S_2	1	1	1	1	0		
1	0	S_2	1 0	S_1	0	1	1	0	1		
1	0	S_3	1 1	S_1	0	0	1	0	1		
1	1	S_0	0 0	S_0	0	0	1	0	–		
1	1	S_1	0 1	S_3	1	1	1	1	0		
1	1	S_2	1 0	S_1	0	0	1	0	1		
1	1	S_3	1 1	S_0	0	0	1	0	1		









$$R_1 = X_1 Q_1 + X_2 Q_1 \bar{Q}_0$$

$$Z_1 = \bar{Q}_1 Q_0 + X_1 \bar{X}_2 \bar{Q}_0 + \bar{X}_1 X_2 \bar{Q}$$