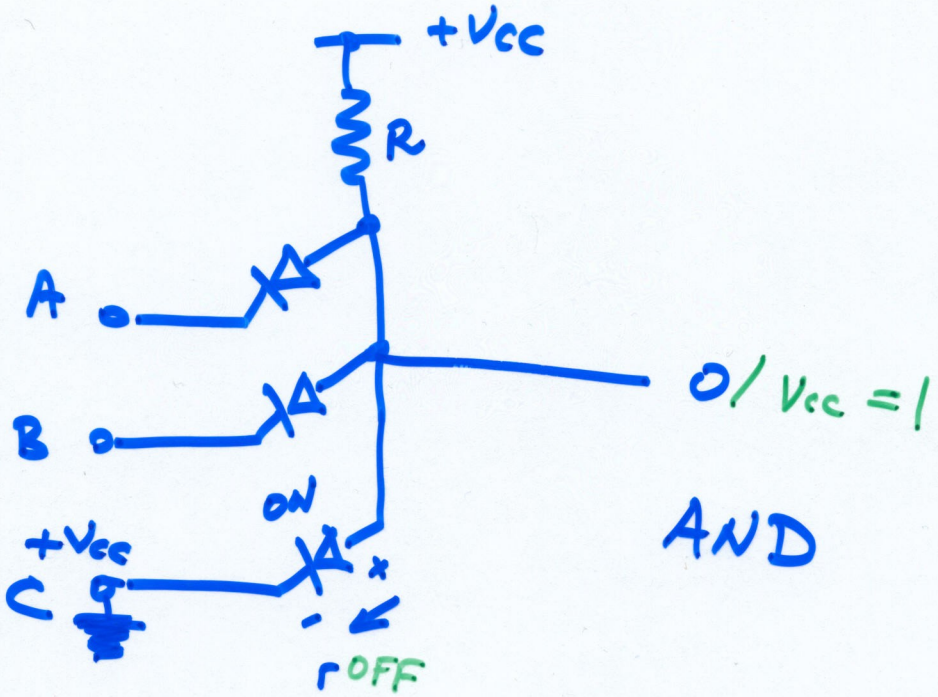
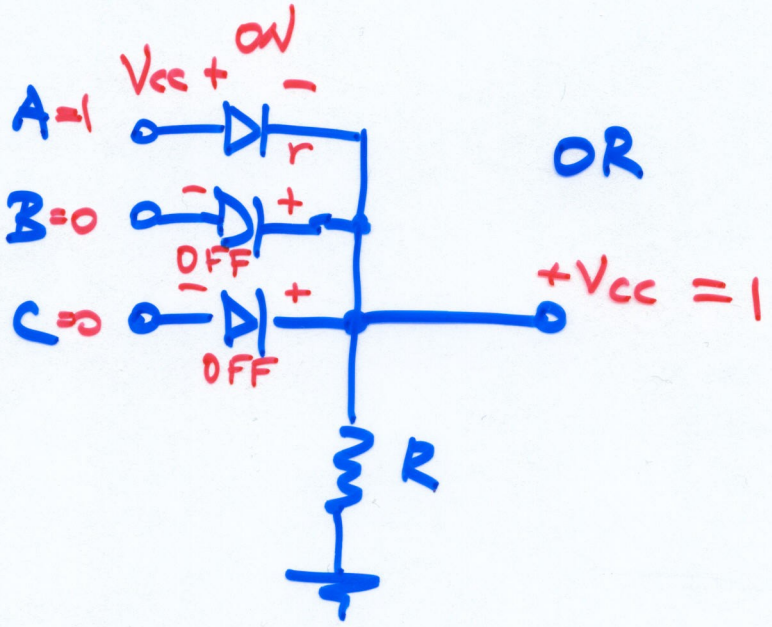
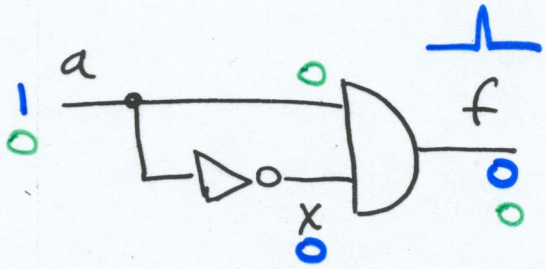


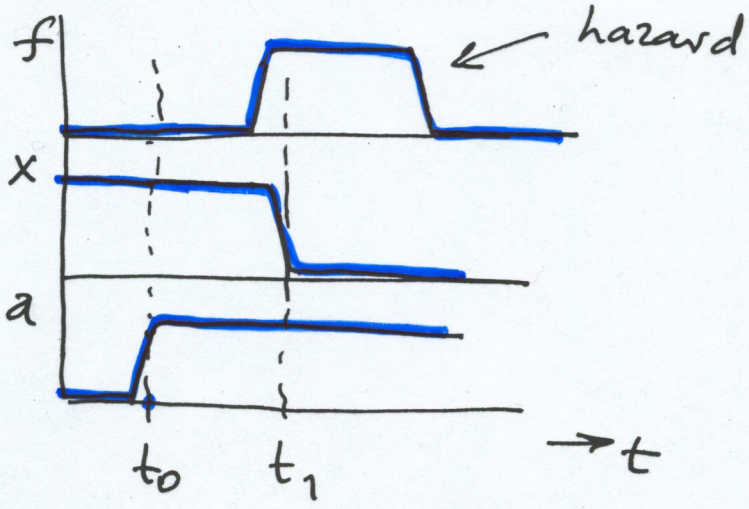


SoP: AND - OR → any function

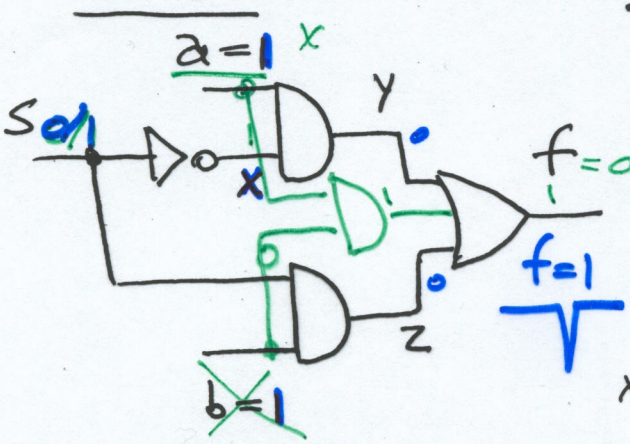
PoS: (OR - AND)

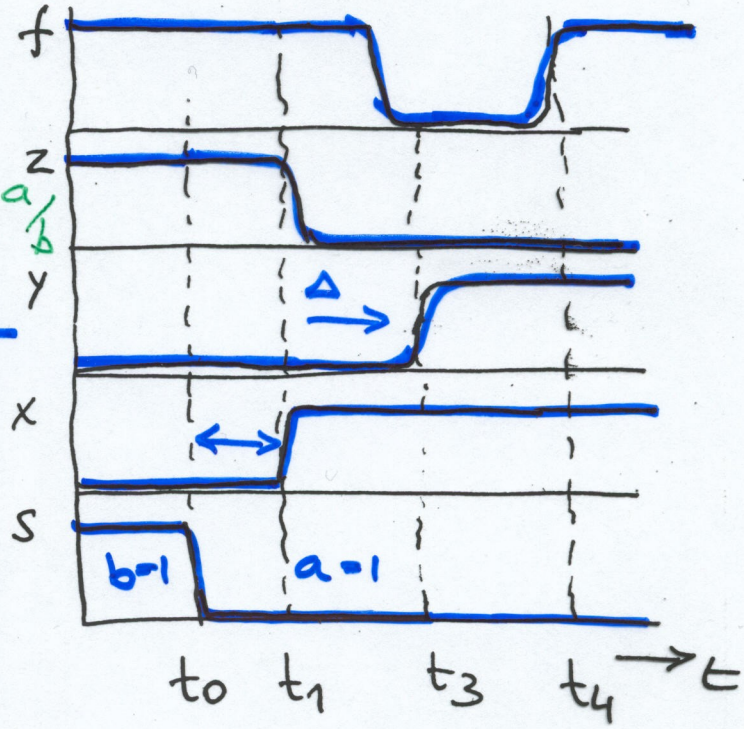
Hazard in Combin. Ckts

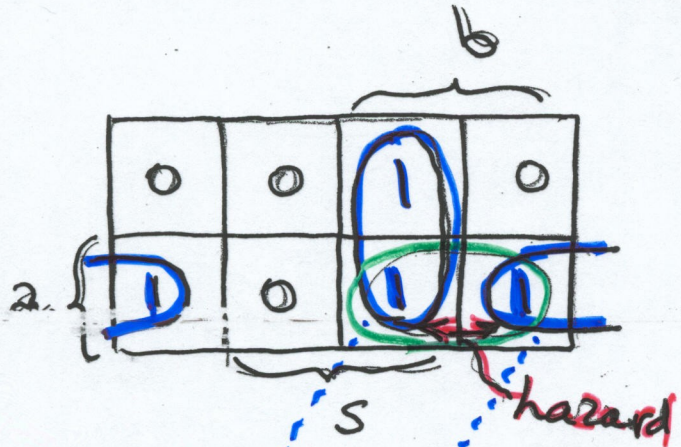




MUX :





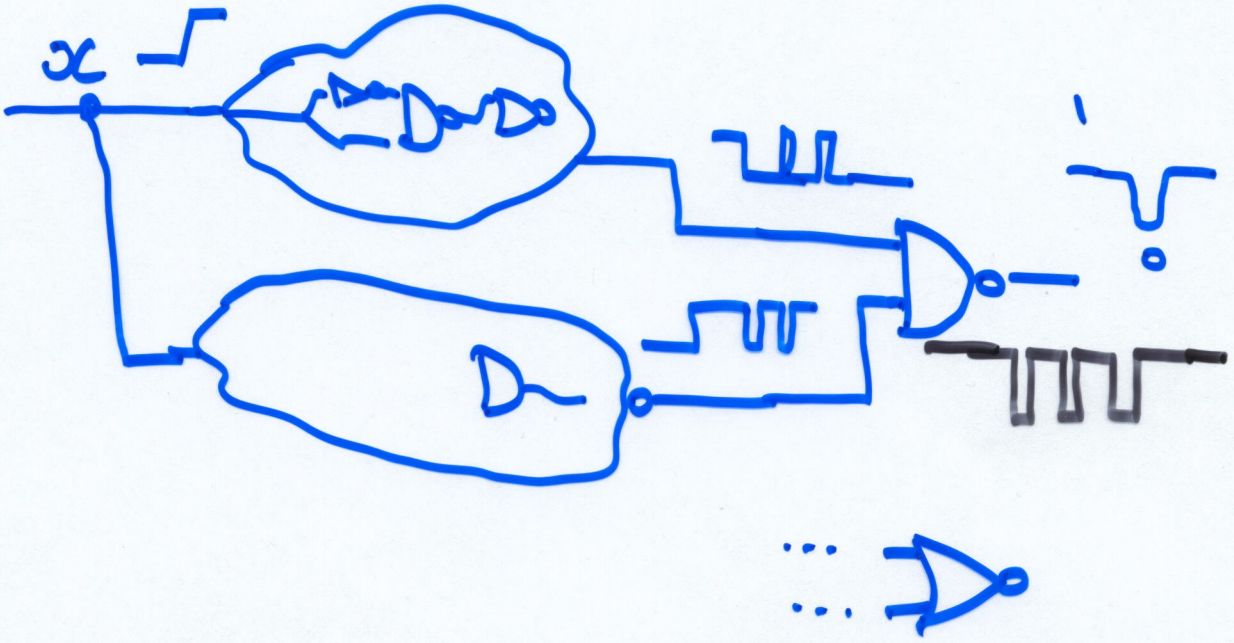


$$f = s \cdot b + \bar{s} \cdot a$$

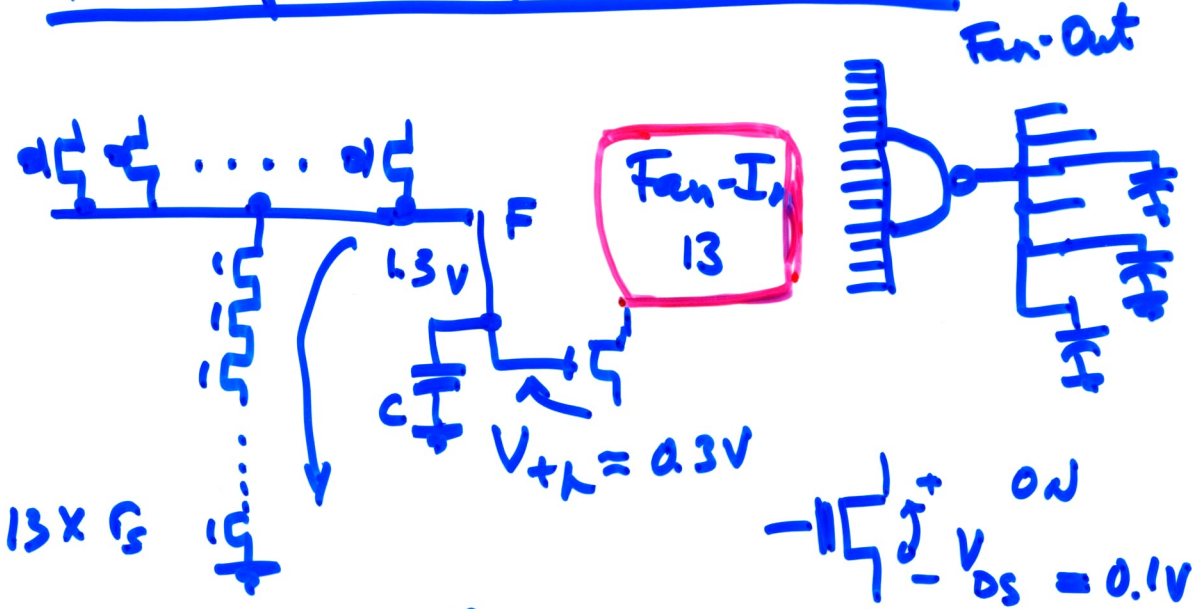
$s=0$; $f=a$

$s=1$; $f=b$

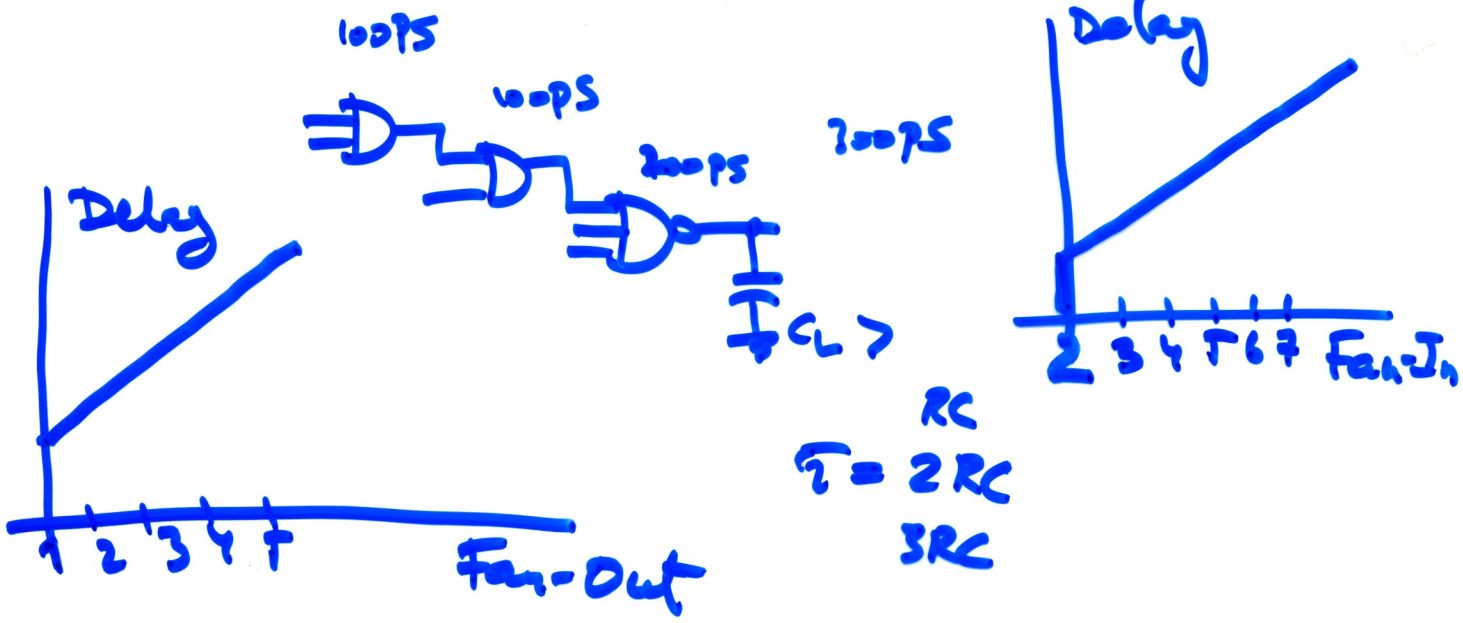
Re-Convergent Fan-Out w/ non-equal parities of inversion:



Multiple Output Networks



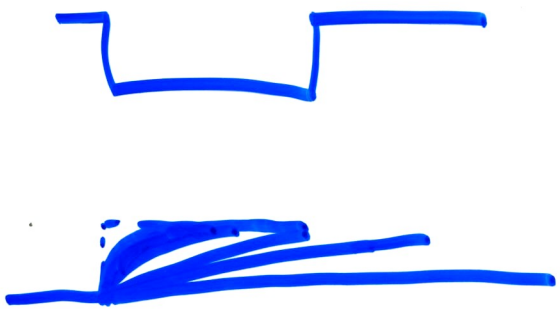
$13 \times R_S \cdot C$

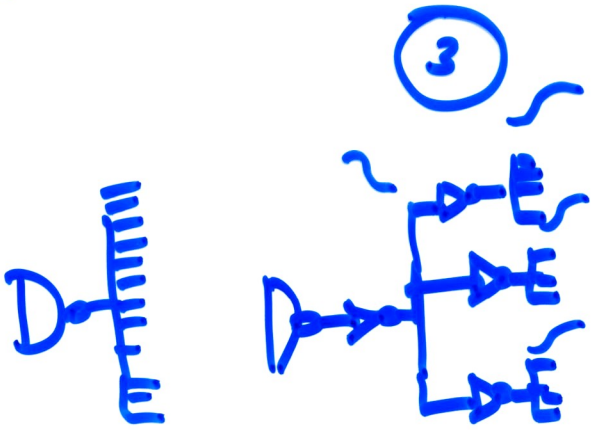


RC

$\tau = 2RC$

3RC



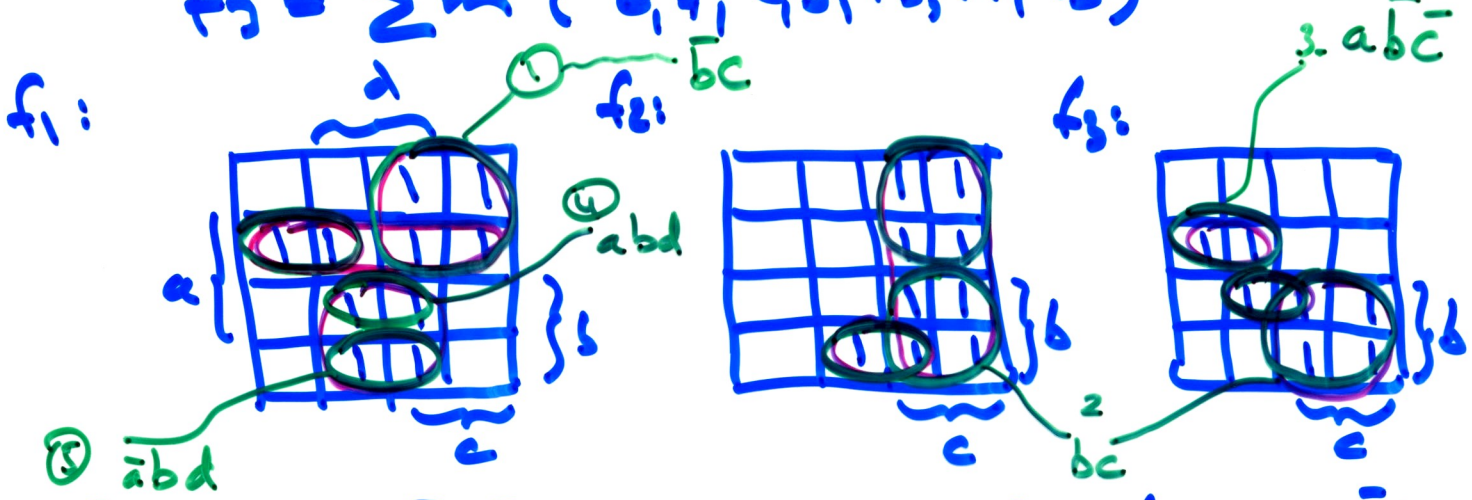


Multiple Output Networks

$$f_1 = \sum m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$$

$$f_2 = \sum m(2, 3, 5, 6, 7, 10, 11, 14, 15)$$

$$f_3 = \sum m(6, 7, 8, 9, 13, 14, 15)$$



$f_1 = bd + a\bar{b} + \bar{b}c$ $\quad f_2 = c + \bar{a}bd$ $\quad f_3 = bc + a\bar{b}\bar{c} + abd$

10 Gates 25 inputs

$$f_1 = \underset{①}{\bar{b}c} + \underset{②}{\bar{a}bd} + \underset{③}{abd} + \underset{④}{a\bar{b}\bar{c}}$$

$$f_2 = \underset{①+②+③}{\bar{b}c + bc + \bar{a}bd} = c + \bar{a}bd$$

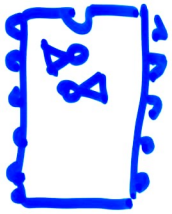
$$f_3 = \underset{①+②+④}{bc + a\bar{b}\bar{c} + abd}$$

8 gates
22-inputs

SSI

small scale of integr.

60's
70's



7400

7404

2-8

100 gates

MSI

70's

Medium Scale of Integr

1000 gates

LSI

70's

4004
8008

Large Scale of Integ

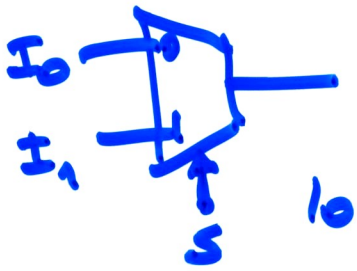
2K-10K gates

4150 transistors

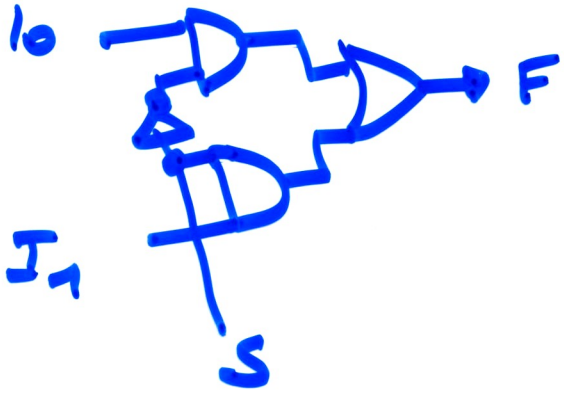
4300

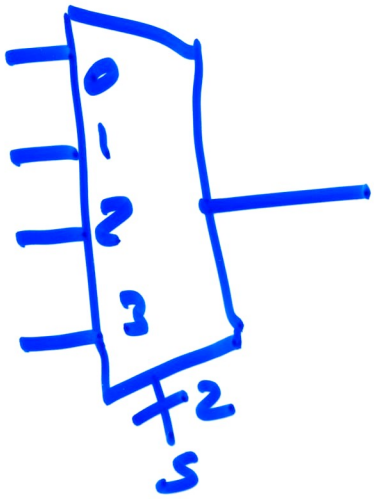
SSI Functions

MUX:

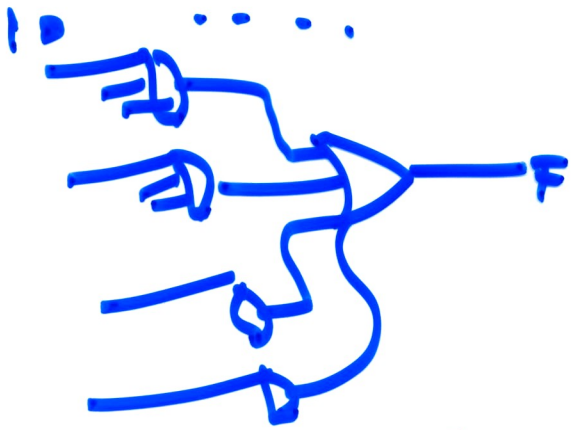


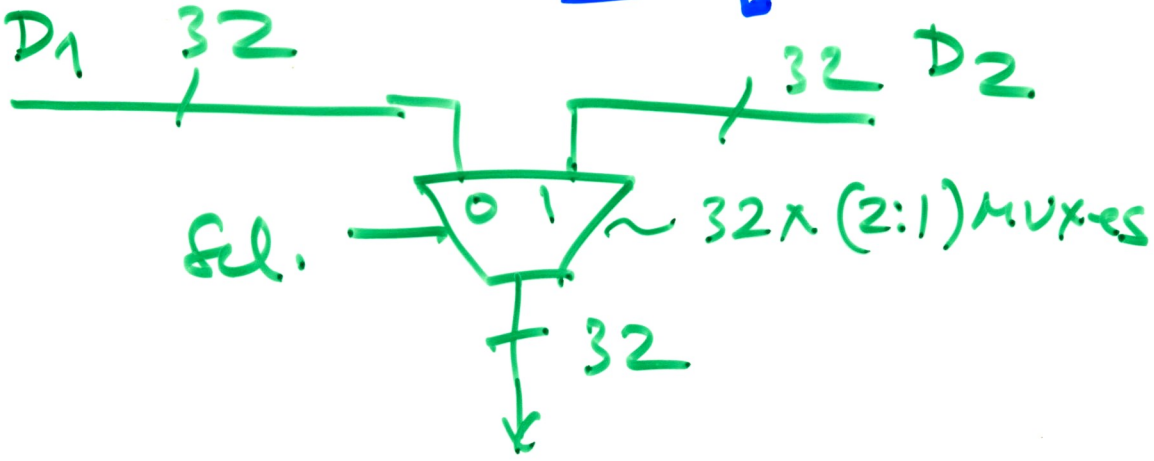
$F = S \cdot I_1 + \bar{S} I_0$





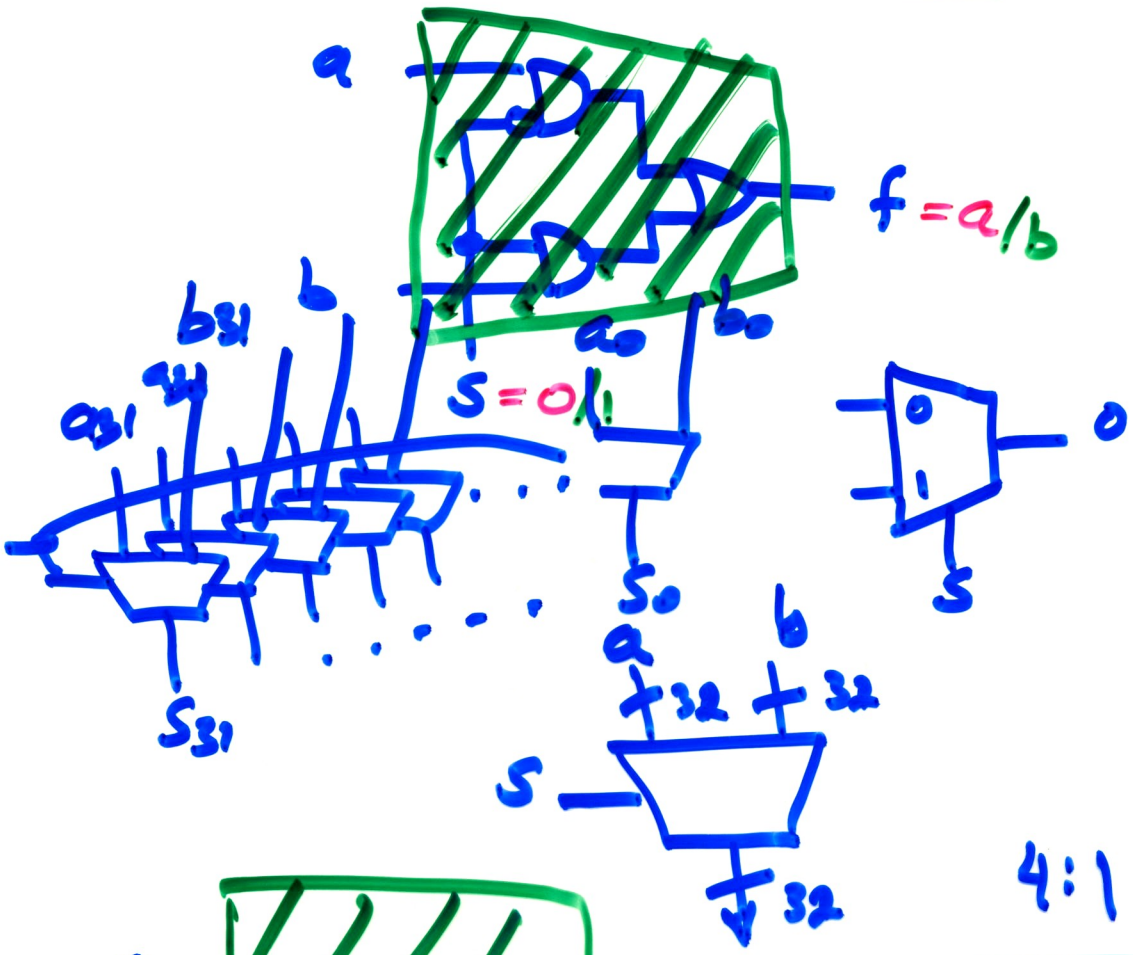
$F = \bar{S}_0 \bar{S}_1 \cdot I_0 + \bar{S}_1 S_0 \cdot I_1 +$

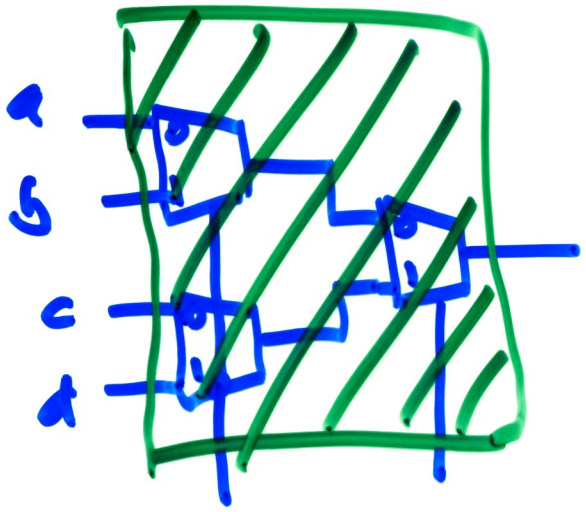


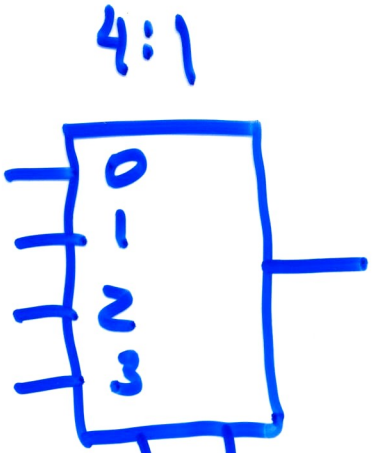


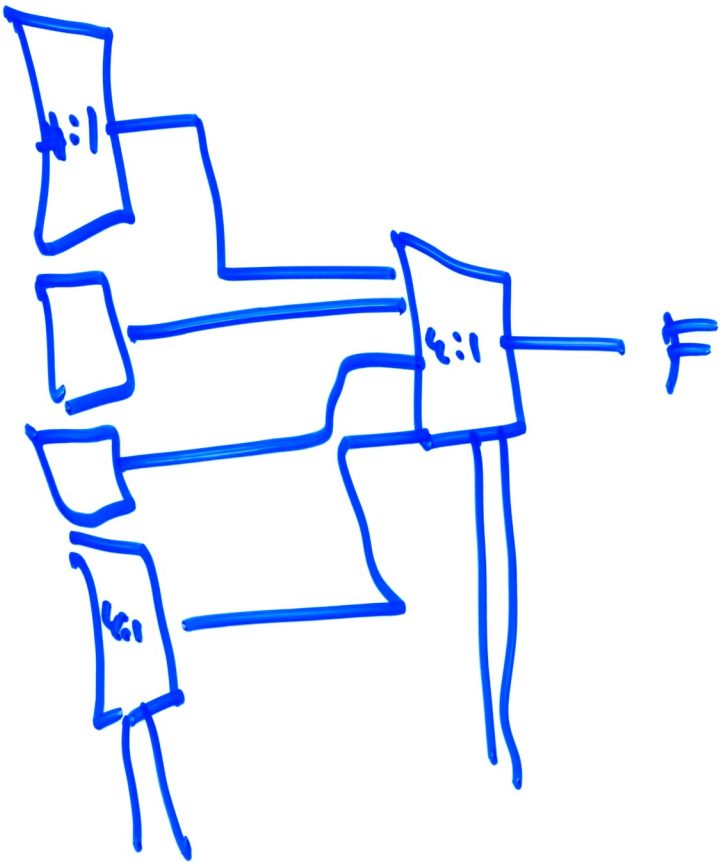
SSI Functions

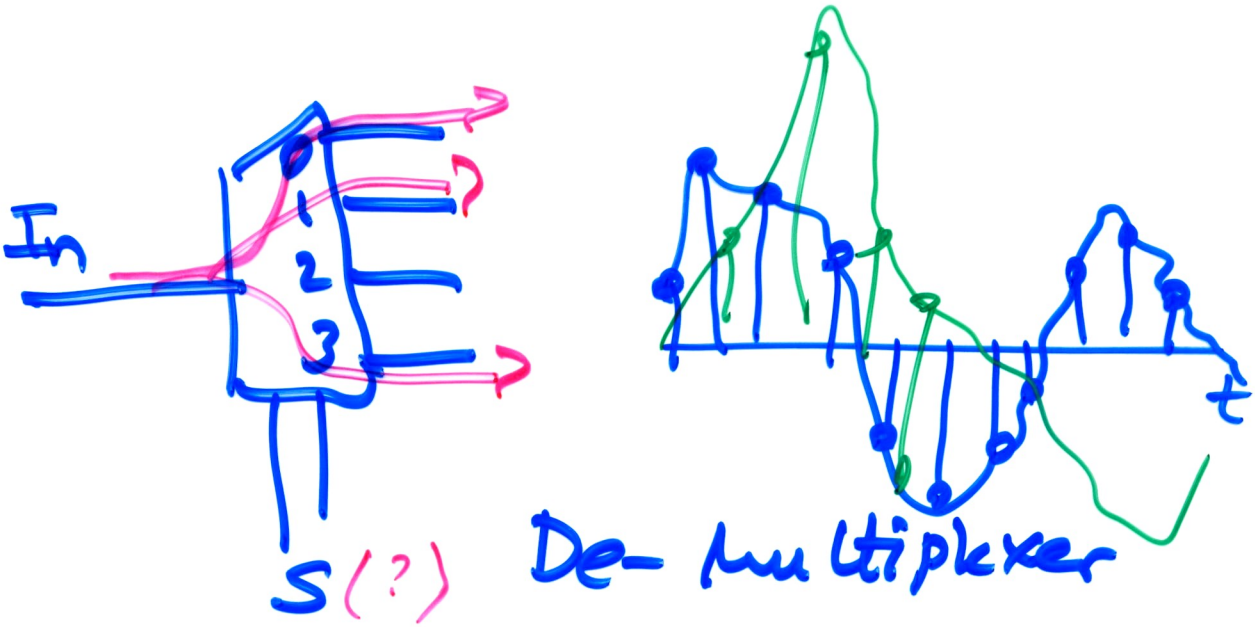
74xx SSI → LSI → μP '4 4x 40-4 → VLSI ~ 1BT



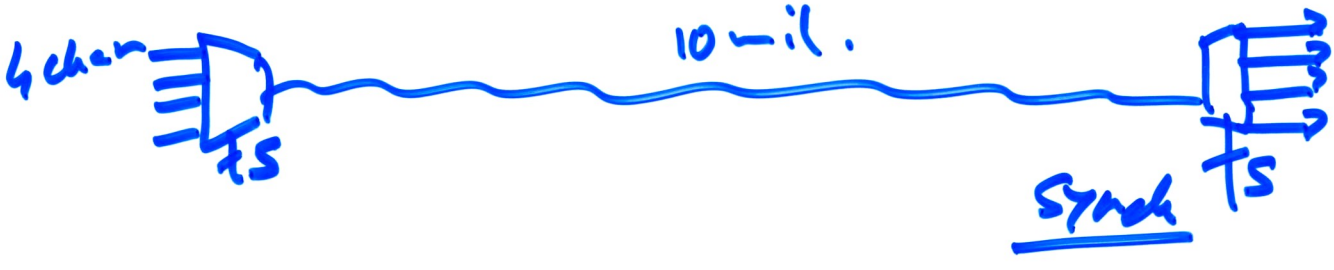








De-multiplexer

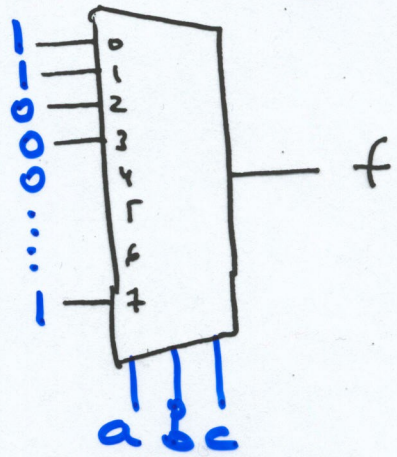


Implementing a function with a MUX:

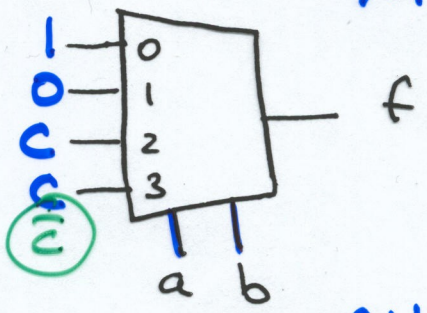
a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Truth Table

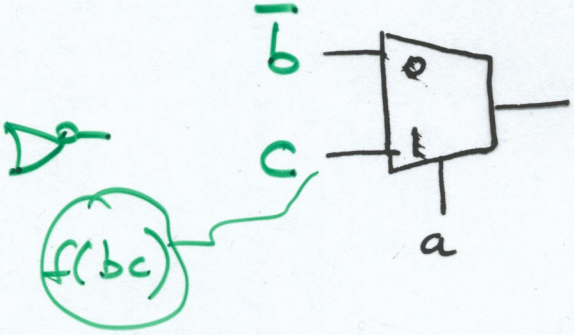
8:1

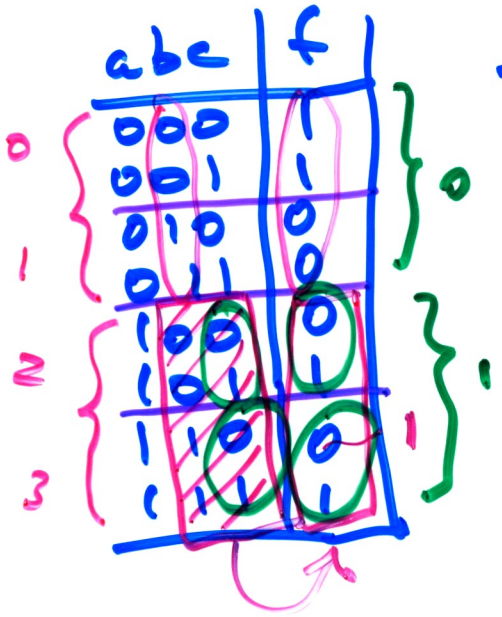


4:1



2:1





$f = \bar{a}\bar{b} + ac$