UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180A **DIGITAL SYSTEMS I** **Winter 2006**

LAB 3: COMBINATIONAL NETWORK DESIGN

The purpose of this lab is to learn how to design a simple combinational logic network.

Hardware Required:

3 pcs.	74LS00	Quad 2-input NAND gate
2 pcs.	74LS04	Hex INVERTER
3 pcs.	74LS10	Triple 3-input NAND gate
1 pc.	7730	7-Segment Display

1. Preparation (Pre-lab)

Do the *complete* paper design of the NAND-NAND implementation of the combinational network specified in the lab write-up. Your paper design must include the following items:

- K-maps for each of the 7-segment driver signals, a-g
- A minimized sum of products (SOP) equation for each of the 7-segment driver signals, a-g
- Circuit representation using gates (i.e. schematic diagram) for the complete network using 3-input NAND gates, 2-input NAND gates and inverters. Note that you are limited to the number of parts specified in the "Hardware Required" list above. Due to the limitation in parts, your implementation will be multi-level instead of two-level.

2. Description

a) Design a combinational network which takes a 4-bit Gray code input and displays a corresponding decimal number on a 7-segment display, as shown in Figure 1. The table on the last page shows the Gray code input patterns and the desired output display values. You should fill in the remainder of the table for each of the 7-segment driver signals, a-g, such that the appropriate decimal number is displayed on the 7-segment display. (The segment labels are shown in Figure 2.) Note that the 7-segment display is ***active low***, meaning that a low voltage is used to light a segment and a high voltage is used to keep a segment un-lit**.** For example, to display 0 on the 7-segment display, segments a-f should be lit and segment g should be off. Therefore, to display 0 signals a-f should be low (0) and g should be high (1) as shown in the table. If an input is given which is not a valid Gray code (i.e. not shown in the table), the output is unspecified or "don't care". Several entries in the table have been given as examples. The digits 6 and 9 can be represented in two different ways on a 7-segment display, so one of the segments in each of these outputs is specified as a don't care. You can use whichever representation is easier to implement.

b) Design **two** networks which satisfy the specification given in part a:

1. Using 3-input NAND gates, 2-input NAND gates and inverters. This design will be based on the minimum SOP equations.
2. Using 3-input NOR gates, 2-input NOR gates and inverters. This design will be based on the minimum POS equations. There are no restrictions on the number of parts which can be used for this design.

c) Enter **both** of your designs in Altera and verify each by simulation. Have your TA verify your simulations.

d) Build and test the circuit using the NAND gates and inverters. You are only allowed to use the number of parts listed in the Hardware Required list. Remember to have your TA verify your working circuit.

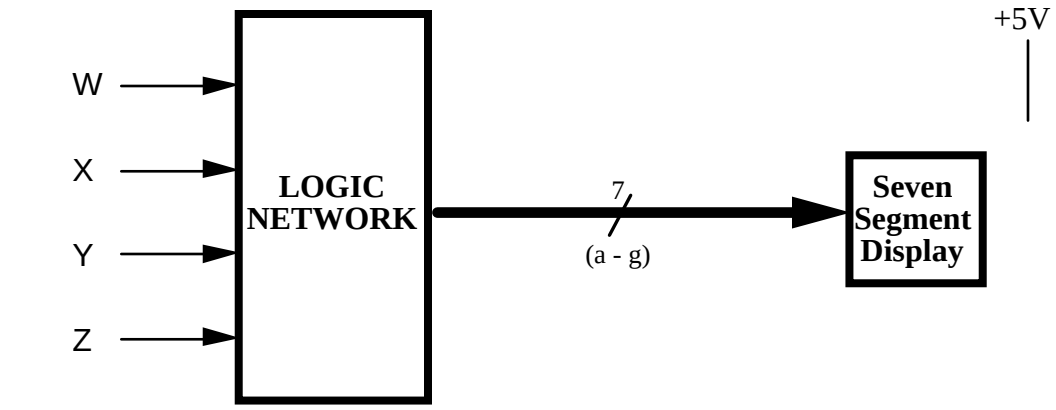
IMPORTANT!!

Make sure that you connect a 330 to 500 ohm resistor to ***each*** segment input of the 7-segment display. Explain why this is necessary in your lab report. (Refer to section 3.5 in your text.) The pin-out of the 7-segment display is shown in Figure 2.

3. Lab Report

Each individual will be required to submit a lab report. Be sure to include the following items in your lab report:

- Lab cover sheet with TA verification for circuit simulation and performance
- Graded pre-lab
- Altera schematics for the two combinational networks
- Complete paper design for the NOR-NOR network including K-maps and minimized product of sums (POS) equations for each of the 7-segment driver signals, a-g



Gray code input

Figure 1. System Block Diagram

W X Y Z	Number to display	a	b	c	d	e	f	g
0000	0	0	0	0	0	0	0	1
0001	1							
0011	2							
0010	3							
0110	4							
1110	5							
1010	6	X	1	0	0	0	0	0
1011	7							
1001	8							
1000	9	0	0	0	X	1	0	0

TABLE OF INPUTS AND OUTPUTS (partial)

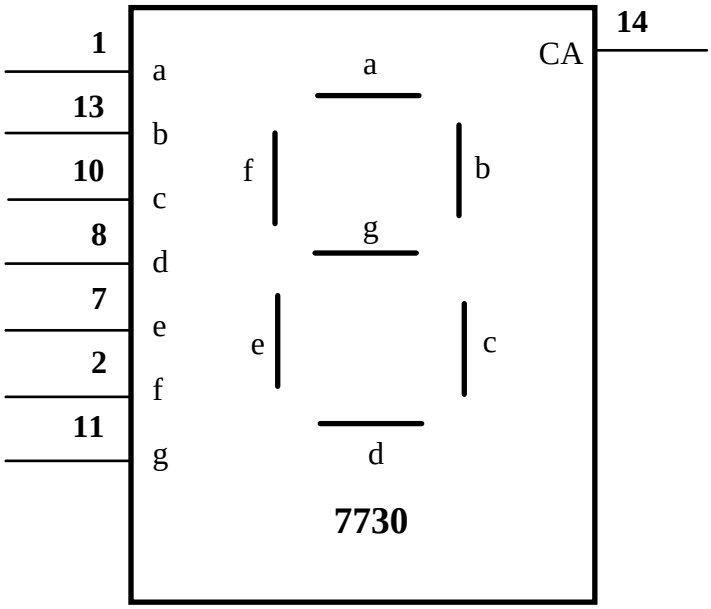


Figure 2. 7730 7-Segment Display Pin-out

Grading

Prelab	20 points
Lab Checkoff	60 points
Lab Report	20 points