University of California, Davis
Department of Electrical and Computer Engineering

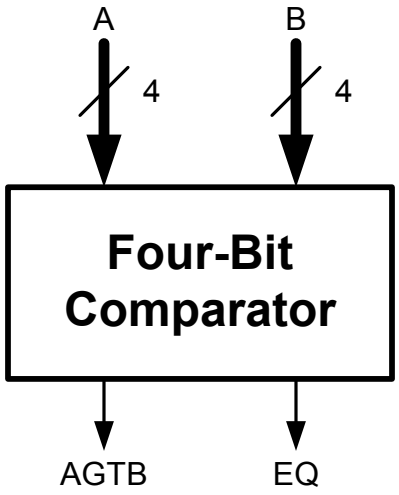
EEC118 Laboratory Project
FOUR-BIT COMPARATOR

Report due on Friday noon, June 6, in EEC118 homework box

Objective:
Design a 4-bit comparator. The logic must be able to handle two single-ended 4-bit inputs and provide two outputs: AGTB (A > B) and EQ (A = B). Hence,

- If A > B, then AGTB = 1 and EQ = 0;
- If A = B, then AGTB = 0 and EQ = 1;
- If A < B, then AGTB = 0 and EQ = 0;

Obviously, AGTB = 1 and EQ = 1 is an invalid output.



Specifications:

- Supply voltage is 2.5V
- Load capacitance on outputs AGTB and EQ are 500fF
- Any logic families except Static CMOS Logic
- NM_H: 1.00V for dynamic circuits, or 0.8V for others
- NM_L: 0.45V for dynamic circuits, or 0.8V for others
- Most importantly, minimize *power-delay product.*

Functional Verification: *demo due week 7*

- Develop logic equations for the comparator.

- Select logic families to implement them.
- Use Max Plus II or equivalent tools to verify the functionality of your Boolean expressions. Make sure it works before you proceed to the next steps.

Circuit Sizing with Logical Effort Method: *demo due week 8*
Apply logical effort method to size your circuit. You need to:
- Identify any critical paths
- Develop sizing and energy strategies
- Find the test vectors for worst-case delays and worst-case energy.

HSPICE Simulation: *demo due week 9*
Use HSPICE to verify your design for possible glitches and transient behaviors.
- Run HSPICE on each basic gate used to obtain the VTC.
- Run HSPICE for the worst-case delay of each output and the worst-case energy
- Assume the following for PMOS and NMOS: AS = AD = 0.25μm*W, PS = PD = 0.5μm+W
- All input signals and clocks have rise and fall times of 300 ps. The rise and fall times of the output signals (10% to 90%) should not exceed 500ps.
- A *rough* SPICE template will be provided for simulation.

Transient analysis on SPICE is computationally intensive. Be sure that you have fully simulated each block before simulating the whole.

Layout: *demo due June 5*
- Sketch the layout at the cell-level and show the cell I/O connections.
- Layout the entire 4-bit comparator in MAGIC. Include power and ground buses. Inputs, outputs, power, and ground I/O's must go to the edges of the cell layout. No layout rules are violated.
- Find your IC area (i.e. smallest rectangular box that encloses the layout)
- Extra credit: extract the comparator netlist from the layout and rerun HSPICE simulation. Compare the results to the previous simulation.

Report:
A formally typed project report is due **June 6th** for all lab sections. Discuss each major phase in detail. Attach related sketches, diagrams, schematics, simulation results and layout. Tabularize your results.