University of California, Davis
College of Engineering
Department of Electrical and Computer Engineering

EEC118 EXPERIMENT No. 5
CMOS DOMINO CIRCUITS

I. OBJECTIVE

The objective of this experiment is to explore the performance advantage of domino circuits over static CMOS and to analyze the charge-sharing problem in domino circuits and its solutions

II. PRELAB

a. Study section 5.4 in the textbook for the operation of domino circuits.
b. Components used in this lab are PMOS-NMOS CD4007 IC and 50-pF capacitance. Pick up these components and build the circuits.
c. From the W/L ratio of PMOS and NMOS found in Experiment No. 2, what is the relative width of PMOS to NMOS in CD4007 (assuming equal length)?

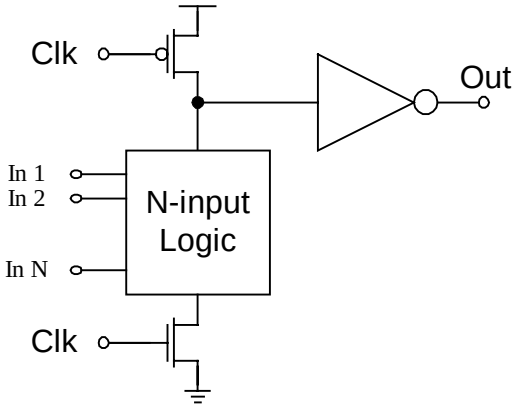

Figure 1

III. FURTHER BACKGROUND

CMOS domino circuits are widely used in high-performance digital system, such as microprocessor and high-speed register files. Typical domino circuit

is shown in Figure 1. It consists of a dynamic circuit followed by a static gate.

There are two phases of operation: pre-charge and evaluation. During the pre-charge phase, clock signal is Low. Therefore, the dynamic output is preset to High and the static output is reset to Low. In evaluation, clock signal is set to High and input to NMOS logic is inserted. If the result of the NMOS logic is false, no transition is seen and the output result is the same as the precharge value. On the other hand, if the result of the logic NMOS is true, the dynamic output will be discharged and causes the static output to be pulled up high to match the logic result.

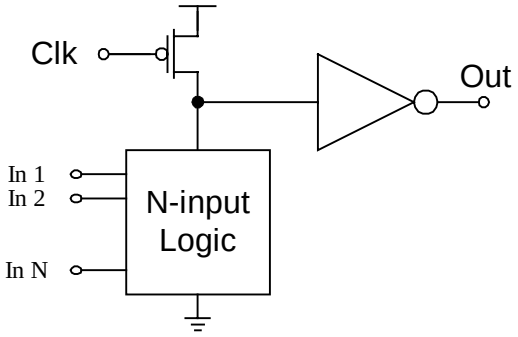

Figure 2

Figure 2 shows a modification of the domino circuit. The clock-controlled NMOS is removed or unfooted to reduce NMOS stack height and therefore increase the pull-down strength of NMOS logic. That results in even higher performance.

IV. DELAY ADVANTAGE OF CMOS DOMINO

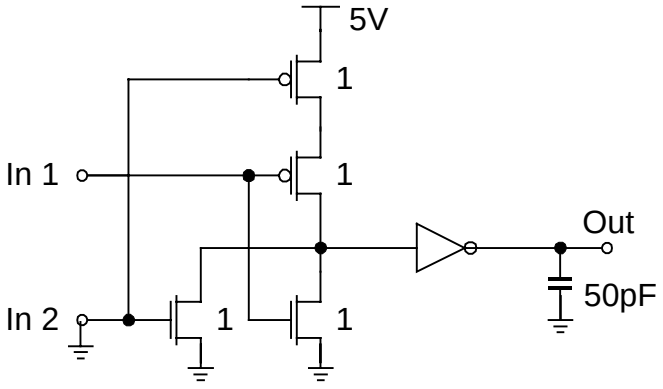

Figure 3

(1) Wire up the CMOS NOR-INVERTER chain as shown in Figure 3. The load capacitance to 50pF. Connect one input to ground. Apply a 5-V, 1-MHz square wave to the other input. Measure the delay from input to the output, for both rising and falling transitions.

(2) Build the CMOS domino OR gate as shown in Figure 4. What is the total size of the input compared to the NOR gate input in (1)? Ground one-OR input and connect the other to supply. Apply a 5-V, 1-MHz square wave to clock. Measure the delay from OR-input to output and compare to the result in (1).

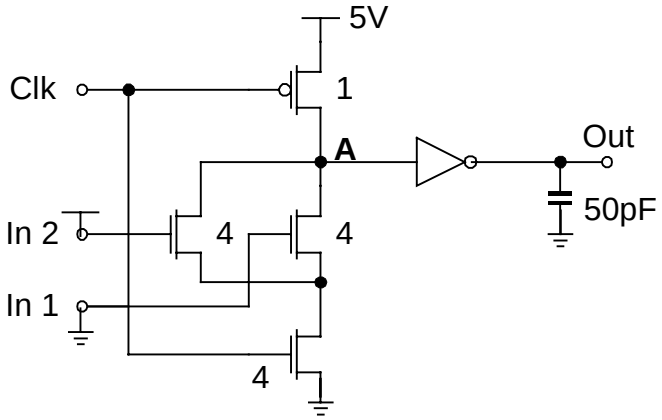

Figure 4

V. CHARGE SHARING PROBLEM IN DOMINO CIRCUITS

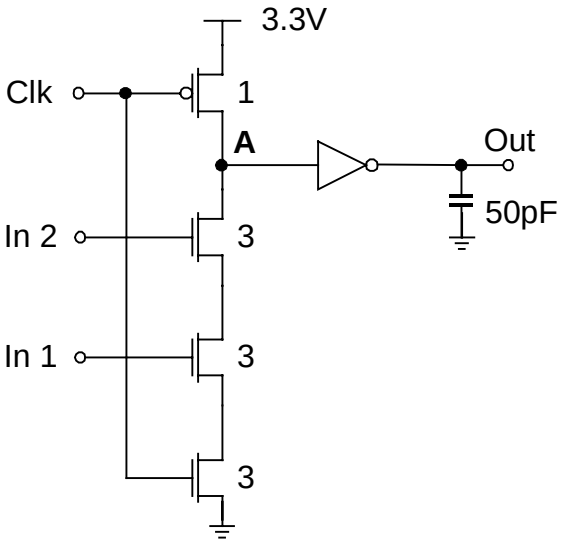

Figure 5

(3) Build the circuit in Figure 5. Follow the following steps carefully to see the charge sharing.

a. Connect Clock, In 1 and In 2 to supply to discharge the dynamic node A.
b. Connect In 2 to ground to isolate node A from ground.
c. Connect Clock to ground to precharge node A. Measure its DC voltage. Then, reconnect Clock to supply.
d. Connect In 1 to ground; then connect In 2 to supply.
e. Measure the DC voltage of node A. Explain what happens.

(4) Connect both In 1 and In 2 to supply. Apply a 5-V, 1-MHz square wave to Clock. Measure the delay from clock to output.

VI. SOLUTIONS TO CHARGE-SHARING PROBLEM

(6) One solution to charge sharing is to use keeper. Build the circuit as shown in Figure 6. Explain how it works.

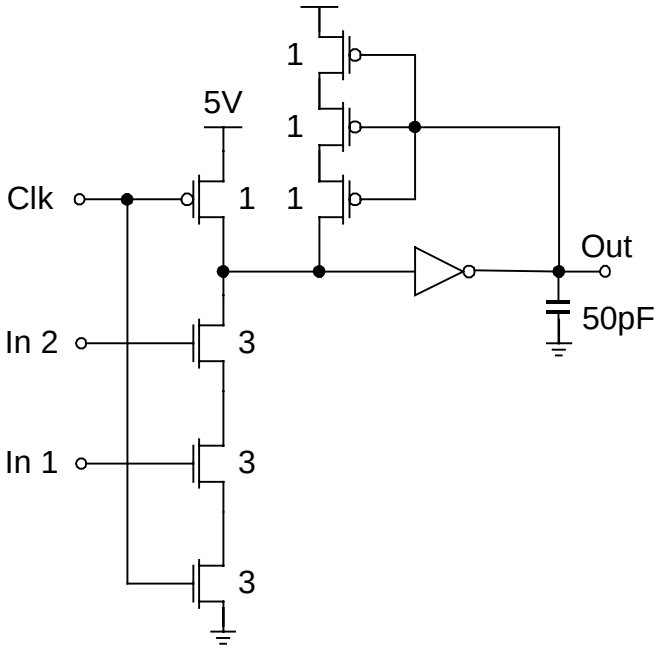

Figure 6

(7) Set both In 1 and In 2 to supply. Apply a 5-V, 1-MHz square wave to Clock. Measure the delay from clock to output. Compare it to the result in section V-4.