University of California, Davis
College of Engineering
Department of Electrical and Computer Engineering

EEC 118 EXPERIMENT No. 3
CMOS INVERTER AND GATES *

I. OBJECTIVE

The objective of this experiment is to determine the Voltage Transfer Characteristic (VTC) of a CMOS inverter and to observe its characteristics in circuit connections.

II. PRELAB

(a) Use your transistor data from EXPERIMENT NO. 2 to calculate several points on the VTC, including V_{OH}, V_{IH}, V_{OL}, and V_{IL}, for the CMOS inverter shown in Figure 1.

HINT: For simplicity in hand calculations, take output voltage as the independent parameter; calculate I_D and input voltage from it

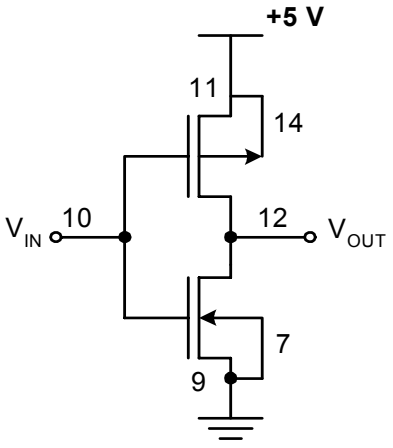

Figure 1

(b) Derive the formula that relates the average delay time to the period of the waveform observed at the output of any of the gates in the oscillator.

* Excerpt from Paul Hurst et al's EEC118 Lab Manual, Spring 2001 – printed with Prof Hurst's permission

III. VOLTAGE TRANSFER CHARACTERISTIC

(1) Wire up the CMOS inverter shown in Figure 1 and observe its VTC. Compare with your calculated results from the Prelab.

(2) Wire up a 2-input CMOS NOR gate using the transistors in the 4007 package.
   a. Show the schematic in your lab manual. Verify the NOR gate truth table.
   b. Connect the two inputs together. Measure the VTC of this inverter. How does the VTC for this inverter-connected NOR gate differ from the inverter in Fig. 1? Explain any observed differences.

IV. GATE CONNECTION-RING OSCILLATOR

(1) The ring oscillator configuration shown in Figure 2 is often used to measure the average propagation delay time.

(2) Wire up 5 CD4001 CMOS NOR gates to form a ring oscillator as shown in Figure 2. Use the oscilloscope to measure its oscillation frequency at supply voltages of 5, 7.5, 10, 12.5 and 15V. Also measure the current I_{DD} drawn from the supply at each voltage. From your results calculate the average propagation delay per gate, t_p, at each of these voltages. Explain the t_p vs. V_{DD} trend. Also compute the gate power-delay product at each voltage (gate power dissipation x t_p). Explain its variation with V_{DD}.

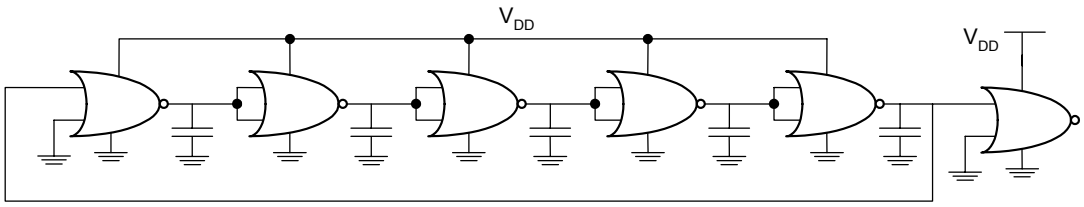

Figure 2

(3) Load each of the five output nodes of your ring oscillator with the same capacitance value of 50pF. Measure the oscillation frequency at V_{DD} = 10V. Assume that propagation delay is a linear function of total capacitance at the output node of a gate (a good assumption), and calculate the approximate equivalent capacitance (due to internal

nodes, package, and external wiring) present at the output of each gate with no capacitors added.

V. LAB 4 PREPERATION

(1) The circuits in lab 4 use many transistors and the wiring is relatively complicated. Therefore, wire the circuit shown in Figure 1a of Lab 4 BEFORE YOU LEAVE LAB TODAY. (See Section II. Part (1) of Lab 4.)