

Tinoosh Mohsenin

Electrical and Computer Engineering Department

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AREA OF INTERESTS

High performance and energy efficient signal processing and error correction algorithms, architectures and chip implementation, including multi-gigabit LDPC decoders and many-core processor architectures.

EDUCATION

Ph.D., Electrical and Computer Engineering, UC Davis, expected May 2010

M.S., Computer Engineering, Rice University, Sept. 2003

B.S., Control Systems, Sharif University of Technology, Tehran, Iran, Sept. 1999

PROFESSIONAL EXPERIENCE

UC Davis, Electrical and Computer Engineering Department

Research assistant, adviser: Prof. Bevan Baas

May 2005-present

1) Algorithms and architectures for very high throughput and high energy efficiency Low Density Parity Check (LDPC) decoders

- Invented Split-Row, Multi-Split, and Split-Row Threshold decoding algorithms and architectures, which significantly reduce wire and circuit complexity when compared with conventional algorithms.
- Analyzed error performance of floating point and fixed-point implementation of various LDPC decoding algorithms in C and MATLAB.
- Wrote sophisticated Perl scripts to parallelize and run simulations on 156 multi-core workstations to study the low error rate performance of LDPC decoders.
- Developed a post processing algorithm to improve the error floor of the Split-Row decoder.
- Devised architectures for very high throughput and high energy efficiency architectures for fully parallel LDPC decoders.
- Implemented decoder chips for 10GBASE-T standard LDPC code using various decoding methods in 0.18 um and 65 nm CMOS using Synopsis Design Compiler and Cadence Encounter. Performed timing simulation, Synthesis, Verilog behavioral and gate netlist verification, chip place and route, timing and area optimization.
- Currently working to architect and tapeout a very low power 10GBASE-T encoder and decoder LDPC chip with on-chip noise generator in 65 nm.

2) Many-core processor architecture design and chip implementation

- Was a key member in a team of graduate students that architected and taped out a high performance and energy efficient 167 processor, 55 million transistor chip in 65 nm in less than a year. Responsibilities include: RTL coding, application programming, synthesis, system integration, place and route, HDL simulations to verify functionality, formal/timing verification, DRC and LVS.
- Tested a fabricated chip using GPIB and lab instruments to verify chip functionality and gather data for power and max operating frequency variations.

UC Davis, Electrical and Computer Engineering Department
Graduate researcher

Dec. 2003-Sept. 2004

10 Gbps optical CDMA encoder-decoder design and BER performance analysis.

- Worked in a team of post doctorates and graduate students to implement and demonstrate a 10 Gbps optical CDMA transceiver system. Responsibilities include writing Verilog RTL description of an LDPC decoder and encoder, performing timing simulations and implementing the decoder and encoder on a 6 Virtex-II Pro chip platform.

Rice University, Electrical and Computer Engineering Department
Research assistant, adviser: Prof. Scott Rixner

Sept. 2002-Sept. 2003

Design and Evaluation of FPGA-Based Reconfigurable Gigabit-Ethernet/PCI Network Interface Card (NIC)

- Designed and architected the first generation RiceNIC, which is a reconfigurable and programmable Gigabit Ethernet network interface card (NIC) with significant computation and storage resources used for research on future network interface architectures. Implemented the system in Verilog, verified the design on a Virtex-II Pro FPGA prototyping board, measured RiceNIC performance on an Opteron server using various TCP payloads.

Nokia Research Center, Irving
Summer intern

May 2002-Aug. 2002

Prototype design for the next generation of cellular systems

- Worked in a team that designed the near final prototype for the next generation of CDMA system. Responsibilities include: IF interface digital design for frequency switching, AGC design, RTL coding with HDL Designer, logic verification and timing simulation, implementation on FPGA and physical system testing on an RF platform.

Towzin Electric Engineering Inc, Tehran, Iran
Design engineer

Oct. 1999-May 2001

- Designed and implemented various automatic weigh station systems with Intel 8051 microcontrollers. Wrote the memory controller, keyboard and LCD interfaces in Assembly. Designed and built the controller platform using OrCAD PCB Designer.

SELECTED COURSE PROJECTS

- Designed and taped out a Huffman encoder and decoder chip in 0.5 um using Magic layout tool. Verified and fully tested the chip which was operating at 20 MHz and validated measured results with IRSIM simulations results.
- Designed and simulated an IEEE 802.11b WLAN transceiver system in emulated mobile channels using MATLAB and C. Performed experiments to empirically measure the performance of an IEEE 802.11b system in a broad spectrum of emulated mobile environments. Implemented the system on a TI C64x DSP.
- Designed, verified and synthesized a 100 MHZ, 32-point, pipelined, fixed-point, 14-bit FFT processor concentrated on (signal to quantized noise ratio) SQNR improvement in 0.25 um.
- Designed and implemented a fully functional CDMA transmitter (including baseband transmitter, upsampling, filtering and AGC units) with a full testbench in 0.25 um.

- Designed and simulated various switch fabric circuits (cross bar, Banyan, Batcher Banyan) in Spice in 0.13 um. Modeled energy consumption and optimized circuits for low power.

REFEREED PUBLICATIONS

Tinoosh Mohsenin and Bevan Baas, "Trends and Challenges in LDPC Hardware Decoders," To appear in Asilomar Conference on Signals, Systems and Computers (ACSSC), November 2009, **Invited**.

Tinoosh Mohsenin and Bevan Baas, "High Throughput and Energy Efficient LDPC Decoders using Multi-Split-Row Threshold Method," To appear, TECHCON, Sept. 2009.

Tinoosh Mohsenin, Dean Truong, and Bevan Baas, "Multi-Split-Row Threshold Decoding Implementations for LDPC Codes," IEEE International Symposium on Circuits and systems (ISCAS '09), May 2009.

Tinoosh Mohsenin, Dean Truong and Bevan Baas, "An Improved Split-Row Thresholding Decoding Algorithm for LDPC Codes," IEEE International Conference on Communications (ICC'09), June 2009.

Dean N. Truong, Wayne H. Cheng, Tinoosh Mohsenin, Zhiyi Yu, Anthony T. Jacobson, Gouri Landge, Michael J. Meeuwsen, Christine Watnik, Anh T. Tran, Zhibin Xiao, Eric W. Work, Jeremy W. Webb, Paul V. Mejjia, Bevan M. Baas, "A 167-Processor Computational Platform in 65 nm CMOS," IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 4, pp. 1130-1144, April 2009.

Tinoosh Mohsenin, Pascal Urard and Bevan Baas, "A Thresholding Algorithm for Improved Split-Row Decoding of LDPC Codes," Asilomar Conference on Signals, Systems and Computers (ACSSC), MA8b1-8, October 2008.

Dean Truong, Wayne Cheng, Tinoosh Mohsenin, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejjia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas, "A 167-processor Computational Array for Highly-Efficient DSP and Embedded Application Processing," In Proceedings of the IEEE HotChips Symposium on High-Performance Chips, (HotChips 2008), August 2008.

Dean Truong, Wayne Cheng, Tinoosh Mohsenin, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejjia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas, "A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling," Symposium on VLSI Circuits, pp. 22-23, June 2008.

Tinoosh Mohsenin, Bevan M. Baas, "High-throughput LDPC Decoders Using A Multiple Split-Row Method," In Proceedings of the 32nd International Conference on Acoustics, Speech, and Signal Processing (ICASSP'07), vol.2, pp. II-13-16, April 2007.

Tinoosh Mohsenin, Bevan M. Baas, "Split-Row: A Reduced Complexity, High Throughput LDPC Decoder Architecture," In Proceedings of the IEEE International Conference of Computer Design (ICCD '06), pp. 320-325, October 2006.

Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Dean Truong, Tinoosh Mohsenin, Bevan Baas, "AsAP: An Asynchronous Array of Simple Processors," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 3, pp. 695-705, March 2008.

Ryan Apperson, Zhiyi Yu, Michael Meeuwsen, Tinoosh Mohsenin, Bevan Baas, "A Scalable Dual-Clock FIFO for Data Transfers between Arbitrary and Halttable Clock Domains,"

IEEE Transactions on Very Large Scale Integration Systems (TVLSI), vol. 15, no. 10, pp. 1125-1134, October 2007.

Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Tinoosh Mohsenin, Dean Truong, Jason Cheung, "AsAP: A Fine-grain Multi-core Platform for DSP Applications," IEEE Micro, vol. 27, no. 2, March/April 2007, invited.

Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Daniel Gurman, Chi Chen, Jason Cheung, Dean Truong, Tinoosh Mohsenin, "Hardware and Applications of AsAP: An Asynchronous Array of Simple Processors," In Proceedings of the IEEE HotChips Symposium on High-Performance Chips, (HotChips 2006), August 2006.

Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Tinoosh Mohsenin, Mandeep Singh, Bevan M. Baas, "An Asynchronous Array of Simple Processors for DSP Applications," In Proceedings of the IEEE International Solid-State Circuits Conference, (ISSCC '06), pp. 428-429, February 2006.

P.Murphy, J.P.Frantz, E.Welsh, R.Hardy, T.Mohsenin and J.Cavallaro, "VALID: Custom ASIC Verification and FPGA Education Platform," Microelectronic Systems Education Conference, (MSE'03), pp. 64-65, June 2003.

PUBLICATIONS IN REVIEW AND PREPARATION

Tinoosh Mohsenin and Bevan Baas, "A Split-Decoding Message Passing Algorithm for Low Density Parity Check Decoders," Submitted for review to TCASI: IEEE Transactions on Circuits and Systems I.

Tinoosh Mohsenin and Bevan Baas, "VLSI Architectures for Multi-Split-Row Threshold LDPC Decoders," to be submitted to IEEE Transactions on Very Large Scale Integration Systems (TVLSI).

INVITED/ SELECTED TALKS

Tinoosh Mohsenin, "High Throughput and Energy Efficient LDPC Decoder Implementations," National Taiwan University (NTU), May 21, 2009

Tinoosh Mohsenin, "High Throughput and Energy Efficient LDPC Decoder Implementations," National Chiao Tung University (NCTU), May 15, 2009

Tinoosh Mohsenin and Bevan Baas, "An 18 Gbps 2048-bit 10GBASE-T Ethernet LDPC Decoder," IEEE International Solid-State Circuits Conference (ISSCC) Student Forum, February 2, 2008.

Tinoosh Mohsenin, "High Throughput and Low Power LDPC Decoders Using Split Decoding Methods," Plato Networks, Santa Clara, Ca, February 26, 2008.

Tinoosh Mohsenin, "High Throughput and Low Power LDPC Decoders Using Split Decoding Methods," Invited speaker by NASA JPL at Caltech, Pasadena, Ca, March 13, 2008.

COMPUTER SKILLS

- Programming languages: C, MATLAB, Perl, C-Shell, Latex, Tcl
- Hardware and CAD: Verilog, VHDL, Xilinx ISE, Synopsis (Primitime, HSPICE, Design Compiler, Nanosim), Cadence (SoC Encounter, NCVerilog, SimVision, ICFB (Virtuoso)),

Mentor Graphics (Calibre DRC/LVS, ModelSim, HDL Designer, HyperLynx, DxDesigner, Expedition), Magic, IRSIM, GPIB, and instrumentation knowledge

PROFESSIONAL ACTIVITIES AND MEMBERSHIP

- Member of IEEE, IEEE Women of Engineering, IEEE Circuit and System Society, IEEE Communications Society
- Reviewer of IEEE Journal of Solid-State Circuits (JSSC), IEEE Transactions on Circuits and Systems-I (TCAS-I), IEEE Transactions on Signal Processing (TSP), IEEE International Conference on Communications (ICC), IEEE International Symposium on Circuits and Systems (ISCAS), IEEE International Conference on Computer Design (ICCD)
- Student volunteer at IEEE GLOBECOME 2006 and SiPS 2008 conferences

REFERENCES

References are available upon request.

IMMIGRATION STATUS

Permanent resident