The circuit uses two inputs:

1) PWM - the same PWM signal that you use for a single N-MOS drive
2) F/R - (forward/reverse) a CMOS compatible logic signal, $1 \Rightarrow \text{forward}, 0 \Rightarrow \text{reverse}$

The circuit has four outputs to connect to the bridge:

The schematic is on page 2. $V_{off}$ should be set to about $1\text{V}$, which causes the hysteretical comparators’ thresholds to be about $0.52\text{V} \& 1.12\text{V}$. When the gates of all MOSFETs are $< 0.52\text{V}$, 'OFF' will be high, signifying that the bridge is off and it is safe to change directions if desired. The flip-flops are clocked at 1kHz and keep track of the present and previous states of F/R.
$U_1, U_2 = CD4013, U_3 = LM6484, U_4, U_5 = CD4001, U_6 = CD4011,$
$U_7 = MM 54C906, U_8 = CD4009$

This circuit has not been tested
The two flip-flops driven by F/R are used to
1) de-glitch the F/R signal
2) ensure that F or R are turned off and
the PWM output is disabled until the H-bridge
is off.

The four comparators with hysteresis are
used to check whether the H bridge is off
or not. If you switch from F to R (or vice
versa), without ensuring the bridge is off,
you may turn on M_{IF} and M_{IR} or M_{IR}
and M_{IF} simultaneously, which destroys the bridge.

The open-drain buffers (U7) drive the bridge
transistors. The top transistors are either off
or on and the bottom ones are pulse-width
modulated. You can't set the PWM frequency
too high or the gates won't be able to switch
fast enough. About 5-6 kHz is good.

The +13 V supply was chosen as a compromise
between being sure M_{IF} & M_{IR} can be fully
on when V_{Bat} is high (~8 V) and not
breaking down the gate oxides when the
car is going slow and the back end in
the motor is low ($V_{max} = 10 V$).