Harvesting and Transferring Vertical Pillar Arrays of Single-Crystal Semiconductor Devices to Arbitrary Substrates

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***Abstract*—Development of devices that can be fabricated on amorphous substrates using multiple single-crystal semiconductors with different physical, electrical, and optical characteristics is important for highly efficient portable and flexible electronics, optoelectronics, and energy conversion devices. Reducing the use of single-crystal substrates can contribute to low-cost and environmentally benign devices covering a large area. We demonstrate a technique to harvest and transfer vertically aligned single-crystal semiconductor micro- and nanopillars from a single-crystal substrate to a low-cost carrier substrate while simultaneously preserving the integrity, order, shape, and fidelity of the transferred pillar arrays. The transfer technique facilitates multilayer process integration by exploiting a vertical embossing and lateral fracturing method using a spin-coated polymer layer on a carrier substrate. Electrical contacts are formed using a bilayer of metal and conducting polymer such as gold (Au) and polyaniline (PAni). In this method, the original single-crystal substrate can be repeatedly used for generating more devices and is minimally consumed, whereas in conventional fabrication methods, the substrate is employed solely as a mechanical support. This heterogeneous integration technique potentially offers devices with low physical fill factor contributing to lower leakage current and noise, reduced parasitic capacitance, and enhanced photon–semiconductor interactions, and enables heterogeneous multimaterial integration such as silicon with compound semiconductors for rapidly expanding large-scale applications, including low-cost and flexible electronics, displays, tactile sensors, and energy conversion systems.**

***Index Terms*—Compound semiconductors, heterogeneous material integration, integrated multifunctional devices, micro/nano-pillars, photon traps, vertical device arrays, 3-D material integration.**

I. Introduction

NEW trends in the semiconductor-based electronics and photonics industry cast new challenges in device capability and generate motivation for monolithic integration of multifunctional semiconductor materials and devices for electronics, photonics, sensing, energy storage, and energy conversion. Several techniques, including epitaxial liftoff [1]–[3], wafer bonding [4]–[11] and heteroepitaxy [12]–[19], promised disruptive technology solutions for an exciting array of applications, including ultrahigh-density logic, memory, photovoltaics, displays, integrated optoelectronics, and devices with ultrawide spectral responses for imaging and sensing. However, these techniques of combining different semiconductor materials on a single substrate have been limited by technological challenges, low throughput, and high manufacturing cost despite significant progress in material synthesis and many promising research device demonstrations. These impediments include the difficulty of developing mass-manufacturable techniques to grow and integrate a variety of materials and devices on a host of surfaces/substrates, CMOS incompatibility due to extreme physical growth conditions such as high temperature, the loss of a complete starting substrate contributing to substantial cost, interface defects, vacancies and traps in heteroepitaxy of mismatched materials, and the resulting unpredictable performance degradation.

Multifunctional material integration with CMOS-compatible electronics and photonics, realized through monolithically integrating multiple elemental, compound, and organic semiconductors with diverse bandgap and physical properties on a variety of low-cost substrates with arbitrary topology, will provide an enormous cost-effective economic opportunity for applications in multispectral imaging, sensing, energy conversion, and photovoltaics. The associated technological hurdles can be circumvented by fabricating high-quality single-crystal and vertically oriented micro-/nanoscale pillars via transformative "top–down" or synthetic "bottom-up" methods of a variety of materials [20]–[22] and then harvesting them while consistently preserving the array morphology in coating a target substrate or surface.

Numerous methods and techniques for integrating high-quality crystalline semiconductors on separate low-cost and often flexible thin carrier substrates such as metal foils and plastic sheets have been reported. These are achieved either by direct growth [16], [23]–[27] or by techniques to transfer them from a starting (mother) substrate onto a carrier substrate [28]–[33]. The market pull for this field has been driven by the demand in flat panel displays, digital imagers, flexible photovoltaic systems, and general proliferation of portable consumer electronics. Plastic substrates, for example, possess many advantages, including lower cost, flexibility, lightweight, biocompatibility, and optical transparency. Unfortunately, the low melting temperature of plastics (often

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$< 220\ ^{\circ}$C) renders them incompatible for growing high-quality inorganic semiconductors using conventional microfabrication processes. Therefore, the technique of directly growing the materials has been limited to refractory metal foils [27] and quartz substrates [16], while for plastic substrates, transfer methods such as dry transfer [30], [34]–[37], wet transfer [28], [38], [39], and contact printing [40]–[50] have been pursued.

In the direct-growth approach, Tsakalakos *et al.* [27] grew randomly oriented Si nanowires on a metal foil at 600 °C–800 °C using a Ta_2N buffer layer and demonstrated solar cells with $\sim$12% efficiency. Based on a similar approach, we demonstrated an ultrafast photoconductor on a silicon dioxide substrate with a response above 30 GHz [17]. Various heterogeneous transfer techniques have been pursued by Rogers *et al.* who have demonstrated the transfer of microstructured single-crystalline silicon ribbons from a silicon-on-insulator substrate using polydimethylsiloxane (PDMS) and a soft-lithography process to remove structures that were fabricated via a planar 2-D dry- or wet-etching process [40], [44], [46], [51], [52]. Javey *et al.* [29] transferred Si nanowires grown on a Si wafer surface via a friction-assisted contact transfer process onto a 2-D surface. Huang *et al.* [53] embedded Si nanowires into a polymer [poly(3-hexylthiophene)] for enhancing the performance of hybrid solar cells. Spurgeon *et al.* [54] grew arrays of Si wires on a Si surface and coated the substrate with a PDMS polymer film that was later removed by scraping with a blade knife while maintaining the vertical pattern fidelity. This mechanical removal process (scraping) is not mass manufacturable and has yet to be shown to maintain the quality of the material transfer for a large area repeatedly, although the concept of substrate reusability has been well discussed.

All of the previously cited transfer methods either do not preserve the vertical orientation of the nanopillar/wire array order on the carrier substrate or are not amenable to vertical process integration and have been limited to 2-D single-crystal film transfer.

In the current approach, we demonstrate an experimental method to harvest and transfer vertically aligned single-crystal semiconductor micro-/nanoscale pillars (MNPs) from a template (mother) substrate to a receiving low-cost carrier substrate while simultaneously preserving the integrity and fidelity of the transferred free-standing pillar arrays by way of vertical embossing or imprinting into a transfer material (typically a polymer) and exercising a lateral fracturing force. Both passive and active devices are demonstrated by fabricating a photoconducting device where the electrical contacts for subsequent vertical process integration [26] are formed using a bilayer of metal and conducting polymer such as gold (Au), polyaniline (PAni), and poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS).

II. Method of Micro-/Nanopillar Transfer

Fig. 1 shows the transfer mechanism of semiconductor (Si) micropillars from the mother substrate using a combination of shear- and bending-stress-induced fracture. A phase-change transfer material, for example, a polymer, is spin coated to a thickness (h_{tm}) onto a low-cost carrier substrate (mechanically held fixed), and the mother substrate with the micro-/nanopillars [array spacing (s_{array}) and height (h_{pillar})] is aligned and vertical pressure is applied with a gliding support to embed the pillars into the polymer, thus resulting in a gap between the two substrates of height of h_{gap}, an embedded height of h_{embed}, and a residual polymer thickness of h_{edge}. The mechanism for transferring the vertical pillars relies primarily on the fracture strengths of the pillar material and the associated mechanical boundary conditions upon application of a general combined loading of bending, compression, tension, shear, and torsion. The pillars are transferred by application of physical force that controllably exceeds the critical material stress limit of the pillars, which, in turn, initiates material separation by fracture-assisted material failure at the pillar–substrate interface. In addition, the material-fracturing process is also influenced by the mechanical properties of the polymer-pillar interfaces at the atomic level. For example, the adhesion strength between polymer and micro-/nanopillars plays an important role during the transfer process. The sources of the adhesion forces are mostly electrostatic and van der Waal's forces that provide high resistance to pillar pullout. Preliminary studies by Pyrz [55] show that the calculated interfacial shear stress of a silicon nanowire–polymer matrix to be 150 MPa with an applied tensile load. This result shows that the interfacial shear transfer stress of the system is significantly higher than that of many traditional fiber-reinforced composite systems. Hence, the mechanical stability and robustness of the polymer micro-/nanopillar matrix is highly advantageous in ensuring the harvesting process integrity.

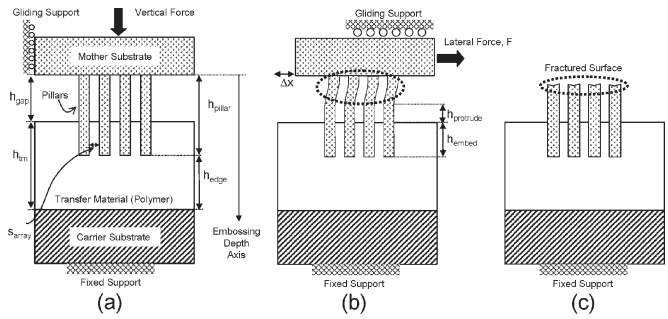

Fig. 1. Schematic for the method of device transfer from an original single-crystal substrate to a secondary carrier substrate. (a) Devices in the shape of micropillars are embedded into a transfer polymer matrix. (b) Both substrates are moved relative to each other in opposing direction to successfully transfer from the mother substrate to the carrier substrate through shear and bending fracturing. The narrower the gap separation h_{gap} between the substrates, the more effective the shearing is and vice versa for bending fracture. (c) Pillar-shaped devices are embedded in polymer-coated carrier substrate.

The state of the polymer during embedding should ideally be viscous and elastic during lateral fracturing. This condition requires that, for example, in case of a thermoplastic polymer such as polymethylmetacrylate (PMMA) or polycarbonate, pillar embossing is achieved when the polymer is heated above its glass transition temperature and laterally fractured after cooling to room temperature and vice versa for curable polymers such as SU-8 (a negative-tone resist), KMPR (a negative-tone resist), and PDMS. Since the elastic moduli of the transfer polymers are typically much lower than that of the crystalline mother substrates, the mechanical boundary conditions of the

embedded pillars prior to lateral fracturing resemble a free end with some allowable rotational and displacement freedom compared to the rigid fixed boundary at the mother substrate. The actual stiffness lies between the extremes of fixed-glided and free-fixed boundary conditions, given by

$$k_{\text{fixed}-\text{glided}} = \frac{12EI}{h_{\text{gap}}^3} \tag{1}$$

$$k_{\text{free}-\text{fixed}} = \frac{3EI}{h_{\text{pillar}}^3} \tag{2}$$

where E is the Young's modulus and I is the area moment of inertia of the pillar. If the carrier substrate is held fixed and the mother substrate is moved relative to it (e.g., mechanically, ultrasonically, etc.), there will be a critical differential load leading to fracture between the semiconductor pillars and the mother substrate.

This is apparent by analyzing the relative magnitudes between the pertinent parameters, as shown in Fig. 1 of h_{gap}, h_{tm}, h_{embed}, and h_{pillar}. By varying these parameters, together with the choice of the polymer, a shear fracture or a combination of shear and bending stress fracture can be achieved. If $h_{\text{gap}} \gg h_{\text{embed}}$, then the fracture mechanism is a small combination of shear and a larger bending stress failure, and if $h_{\text{gap}} \ll h_{\text{embed}}$, shear stress failure mainly dominates. For the latter, it is crucial that the fracture load does not exceed the allowable tensile stress of the polymer with thickness h_{tm} or the adhesion force with the carrier substrate. The elastic moduli of the transfer polymers may range from ~0.3 MPa to 3 GPa, which are orders of magnitude smaller than that of the semiconductors; therefore, for bending fracture, each pillar may be approximated as a fixed-free cantilever with a stiffness given by (2) (for $h_{\text{gap}} \gg h_{\text{embed}}$). The maximum bending stress $(\sigma_{\max})$ theoretically occurs near the vicinity of the root of the micro-/nanopillar with the substrate and can be quantified by both static experimental methods based on classical Euler elastic beam theory with the appropriate boundary and loading conditions. Upon application of a point load F, the maximum bending stress can be expressed as

$$\sigma_{\max} = \frac{4Fh_{\text{pillar}}}{\pi r^3} \tag{3}$$

where r is the radius of a cylindrical pillar [56]. For transfer-by-fracture to occur, from (3), the maximum bending stress needs to be larger than the fracture strength of the material $\sigma_{\max} \geq \sigma_{\text{FS}}$. The ordered array of N pillars acts as columns with parallel stiffness and thus increases the required applied lateral load by a factor of N for the same fracturing displacement identified by the linear Hooke's relationship

$$F_{\text{array}} = Nk_{\text{pillar}}\Delta x. \tag{4}$$

Numerous studies have been conducted on the fracture strength of prominent crystalline materials. Using bridged Si nanowires and applying a static force with an AFM tip, the critical bending strength of nanowires epitaxially connected to a single-crystal surface was found to be ~500 MPa [57], which is about ~0.3% of the Young's modulus. Hoffmann *et al.* [58] reported higher values by more than an order of magnitude

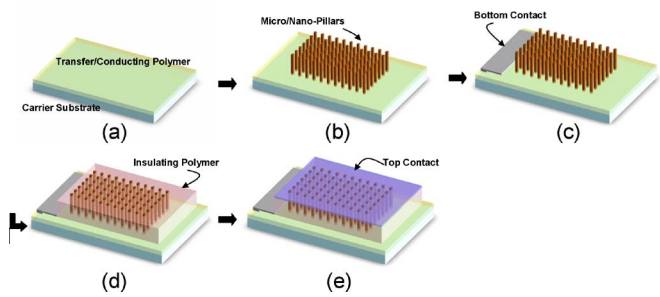

Fig. 2. Schematic for the device transfer process. (a) Conducting polymer (e.g., a mixture of PMMA–PAni) is spin coated on the glass substrate. (b) Devices in the shape of Si micropillars are embossed into the polymer to the required depth, while the substrate is kept at a temperature of 140 °C and a lateral force is applied to the Si substrate, consequently separating the substrate from the pillars by shear/bending fracturing. (c) Bottom-contact metal is evaporated on the conducting polymer outside the device region. (d) Insulating PMMA is spin coated at low RPM, and a partial etch back is done with RIE to expose the Si pillar top. (e) Transparent conducting electrode, e.g., ITO, thin metal is then evaporated by shadow masking.

by using an AFM inside an SEM to estimate the average Si nanowire fracture strength and found it to be ~10 GPa, which is within ~6% of the Young's modulus. Hence, it is widely acknowledged that, for Si micro-/nanopillars, there is a large scatter in data for the measured $\sigma_{\text{FS}} \sim 0.01 - 20$ GPa [59] due mostly to various defects during fabrication and growth. Generally, the fracture strength of most nanoscale semiconductors will be significantly lower than their respective Young's modulus, as noted for silicon nanowires [59], germanium nanowires [60], GaN nanowires [61], ZnO nanowires [62], [63], and SnO nanowires [64].

Hence, any single-crystalline inorganic semiconductor can be practically fractured during the transfer in the polymer matrix by any combination of bending, shear, tensile, compressive, or torsional loading. The thickness of the polymer (h_{tm}) and the corresponding material properties would determine the largest area of the pillars that may be successfully transferred without the polymers failing either by losing adhesion with the carrier substrate or through tensile failure. The common electrically insulating polymers used in the microfabrication processes have a range of allowable tensile stress, for example, PMMA of ~50–80 MPa, polyimide of ~140–230 MPa, KMPR/SU-8 of ~34 MPa, and PDMS of ~2–3 MPa, while conductive polymers like PAni and PEDOT:PSS (Sigma-Aldrich) have a tensile strength of ~25–55 MPa.

III. Results and Discussion

The feasibility of the method was demonstrated with three different polymers as the transfer layer: KMPR (a negative epoxy photoresist from MicroChem), PDMS (Dow Corning), and PMMA (MicroChem). The technique to transfer the high-aspect-ratio vertical micropillars can be classified generally into two schemes. In Fig. 2, a PMMA or PMMA–PAni mixture of thermoplastic film is first spin coated onto the carrier (glass) substrate to a thickness of 6–10 μm, about ~0.5 of the micropillar height. The Si micropillar substrate is then placed atop the PMMA-coated glass substrate on a customized aluminum jig attached to a hot plate. The film is then heated above the glass transition temperature (T_g =105 °C) to a temperature

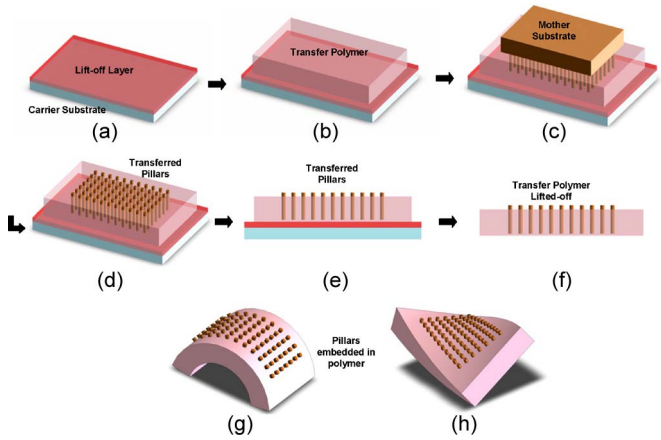

Fig. 3. Schematic for the device transfer process with liftoff. (a) Liftoff layer (e.g., SiO_2, metal, and photoresist) is either grown, deposited, or spin coated on the glass substrate. (b) Transfer polymer PMMA, PDMS, or KMPR is spin coated. (c) Substrate is heated, and the Si pillar is then imprinted into the polymer to the required depth. (d) and (e) Lateral force is applied to the Si substrate to separate the substrate from the Si pillars by shear/bending fracturing. (f) Embedded Si pillars in polymer are then lifted off by removing the released layer. (g) and (h) Conceptual model indicating the flexibility of the released polymer device with embedded Si pillars.

range between 140 °C and 200 °C, depending on the required viscosity of the polymer, the duration of embossing, the area of array transfer, and the applied pressure. The micropillar substrate was then imprinted into the PMMA polymer using embossing forces ranging from 10 to 100 N suitably applied on the mother substrate for a duration of ∼2 min. The applied force can be adjusted to the desired depth of embedment of the micropillar as the viscous PMMA polymer is forced to flow conformally around its surface. The substrates are then cooled down to room temperature. A combination of lateral static force and impulse is applied on the mother substrate, thus separating the micropillars through shear and bending stress fracturing. To isolate the top and bottom electrodes, an insulating polymer (PMMA) is spin coated at a low spin speed and baked at 95 °C. A partial etch back in O_2 reactive ion etching (RIE) is done to expose the silicon micropillar top, followed by a shadow mask evaporation of the top electrode of ITO or thin metal.

Alternatively, the mixture of PMMA–PAni can be prepared to act simultaneously as the mechanical and electrical transfer layer. The mixture ratio should be optimized to preserve the thermoplastic property of PMMA and the conductivity of PAni. Using a ratio of 3 : 2 of PMMA to PAni, the mixed polymer was heated to 140 °C so as improve the adhesion and load uniformity [65] but not to severely degrade the PAni conductivity, while the micropillars were embossed. PAni conformally coats the pillars contributing to a conducting semiconductor–polymer interface, and the evaporated metal layer enhances the conductance of the bottom electrode. The sample is baked at 80 °C for 1 min. Another option is to transfer the micropillars onto a flexible polymer substrate. From Fig. 3, an additional liftoff release layer is either grown, deposited, or spin coated onto a glass substrate prior to a transfer polymer layer. The sequence to transfer is as before but with an additional step of wet/dry processing to release the device layer.

Prior to the transfer process, high-aspect-ratio vertically oriented silicon ($\rho < 0.01\ \Omega \cdot \mathrm{cm}$) micropillars were fabricated

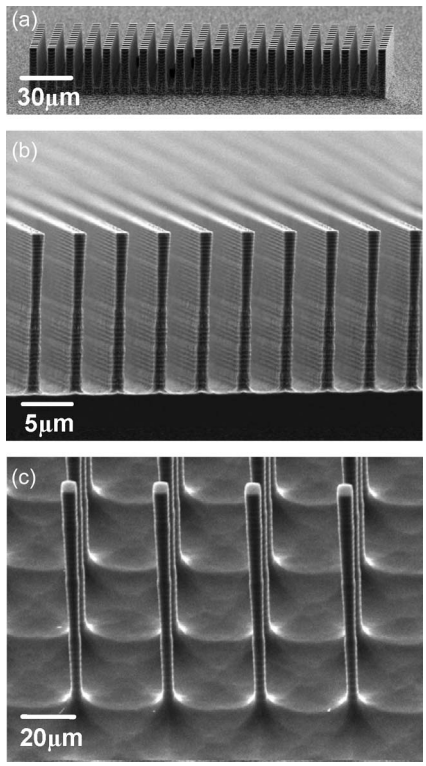

Fig. 4. SEM micrographs of the high-aspect-ratio silicon micropillars fabricated using DRIE processes. (a) 20 × 20 pillar array with a diameter of ∼5 μm and a length of ∼25 μm. (b) Cross-sectional view of uniformly patterned pillars throughout a 4″ wafer. (c) Wafer surface nonuniformity due to the scalloping effect of the BOSCH etch–passivation process can be made smoother by DRIE process optimization and thermal oxidation with a final wet etching (using BOE).

with the deep RIE (DRIE) process using the BOSCH recipe of cyclical passivation and etching. A highly doped p-type Si(100) substrate with a doping concentration of $\sim 10^{19}$ cm^{-3} was patterned with a 2-μm dot etch mask for the subsequent DRIE process. The processing was done while keeping the substrate at 10 °C with SF_6 and C_4F_8 flows of 300 and 150 sccm, respectively, a source RF power at 1800 W, and a substrate power at 20 W for a total etching time of ∼6 min. The individual etching-to-passivation cycle ratio was 6 : 3 s, and an O_2 10-s clean was executed before and after the process. The pressure of the chamber was regulated by holding the gate valve position at 42%. The resulting fabricated Si micropillars are shown in Fig. 4. Two different patterns were etched: a 20 × 20 pillar array [Fig. 4(a)] of dimensions ∼20 μm (height) × 2 μm (diameter) and a uniformly patterned pillar array [Fig. 4(b)] of dimensions ∼1.4 μm (diameter) × 20 μm (height). The scalloping sidewalls seen in Fig. 4(b) are a direct result of the DRIE process parameters in the etching–passivation BOSCH cycle. This surface imperfection can be smoothened by either optimizing the process or using thermal oxidation, followed by buffered oxide etch (BOE), as shown in Fig. 4(c) [66].

The mother substrate with the Si pillars was then prepared for the transfer process to a receiving substrate (in this case, a glass substrate) by spin coating first a transfer polymer. Three different polymer candidates were explored: KMPR, PDMS, and PMMA. The mother substrate was then cleaved to a smaller die of size of ∼5 mm by 5 mm. The polymers were

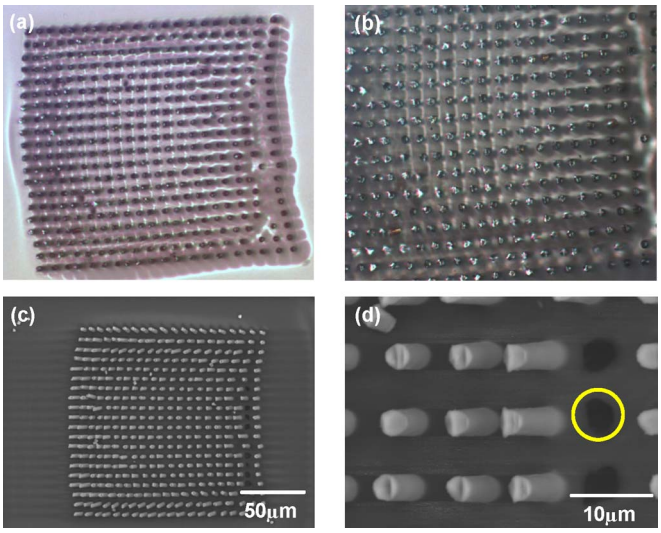

Fig. 5. Vertically transferred 20 × 20 array of devices in the shape of micropillars into a negative epoxy polymer (KMPR). (a) Top view of an optical image of the transferred Si micropillars. (b) Close-up of the pillars with some optical specular reflections from the crystalline fractured surfaces. (c) SEM image of the array. (d) Close-up showing the fractured crystalline surface. The circled area highlights an example of untransferred pillar leaving an imprint pattern. This could be a result of nonuniform fracturing pressure being applied locally.

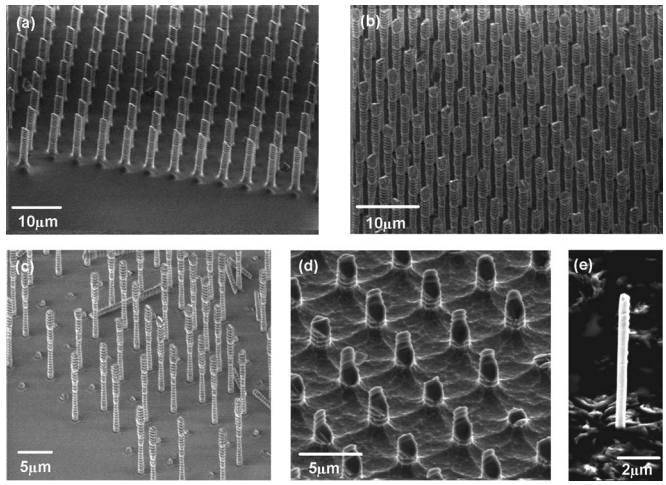

Fig. 6. Vertically transferred aligned Si micropillar array from a mother substrate into a flexible polymer substrate. Tilted view of the transferred array in (a) polydimethylsiloxane (PDMS)/glass and (b) polymethylmethacrylate (PMMA)/glass. (c) Tilted view of the transferred array depicting the broken and unbroken pillars embedded in PMMA. (d) Mother substrate after the transfer with the remaining fractured roots of the micropillars. The substrate can be reused through standard wafer polishing. (e) Vertically transferred oriented Si nanowires grown using the VLS technique in a PMMA/PAni composite polymer.

separately spin coated onto individual glass substrates of size of $\sim 1'' \times 1''$. Both KMPR and PDMS layers have the advantage of room-temperature embossing, while PMMA requires a heated substrate at 140 °C–220 °C. The embossing of Si micropillar onto a KMPR spin-coated glass substrate was achieved using a force load of ∼10 mN on an array pillar contact area of $\sim 5.7 \times 10^{-9}$ m^2 for an applied pressure of ∼1.8 MPa. The depth of embedding was ∼10 μm. After the two substrates have been baked at 100 °C for 5 min, lateral forces using a micropositioner were applied to fracture, separate, and transfer the pillars. The resulting transfer images are shown in Fig. 5. The optical specular reflections seen in Fig. 5(a) and (b) are from the crystalline fractured surfaces. Fig. 5(c) and (d) shows also that the fracturing force was not applied uniformly, as evidenced by the vacant imprint left by some pillars that were embossed but had not been fractured.

A similar embossing–fracturing process sequence was applied on a glass substrate that was spin coated with PDMS, except that the pre-embossing curing was done for 6 h at room temperature. Fig. 6(a) shows the tilted SEM view of the transferred Si micropillar arrays that clearly demonstrates the preservation of the original array pattern fidelity over a large printed area. An embossing force of ∼10 mN was applied on an array pillar contact area of $\sim 9.2 \times 10^{-7}$ m^2 for an applied pressure of ∼10.8 kPa. The depth of embedding was ∼5 μm. For the transfer onto a thermoplastic polymer PMMA, the carrier substrate was first heated to a temperature of 220 °C. The micropillar die was then placed on the PMMA surface with simultaneous application of an embossing force of ∼100 mN on a pillar array contact area of $\sim 3.7 \times 10^{-7}$ m^2 for an applied pressure of ∼0.27 MPa. The "bonded" substrates were allowed to cool to room temperature prior to the lateral fracturing. The depth of embedding was ∼6 μm, and the resulting transfer images are shown in Fig. 6(b) and (c). After the lateral fractured transfer, there are still some remnant roots of the micropillar on the mother substrate, as seen in Fig. 6(d). The fractured surfaces of the pillars are crystalline planes and are hence sufficiently smooth for making electrical contacts. The surface nonplanarity of the mother substrate can be either chemically etched away or planarized using chemical–mechanical polishing such that the substrate is rendered reusable. Other than the top-down DRIE-etched micropillars, large areas of Si nanowires grown by the vapor-liquid-solid (VLS) CVD technique [67], [68] on a Si(111) substrate $(\rho \sim 4 - 6\ \Omega.\text{cm})$ were also transferred into a PMMA/PAni conducting thermoplastic polymer, as shown in Fig. 6(e). The nanowires were grown from an annealed 2-nm gold thin film that produced a varying range in the distribution of diameter and length. Prior to the deposition of the catalyst, the Si(111) substrates were cleaned with acetone, methanol, and isopropyl alcohol, followed by a 30-s dip in BOE, and blown dry with ultrahigh-purity nitrogen. The sample was placed in the CVD chamber and annealed in hydrogen for 20 min at 10 torr and a temperature of 600 °C to form Au–Si eutectic droplets. Subsequently, a mixture of SiH_4 (15 sccm) as a precursor and H_2 (3 slpm) as ambient gas was made to flow for 30 min at 10-torr pressure and a temperature of 680 °C to form dense Si nanowires. For consistency in the transfer process, a patterned ordered array of uniform diameter and length of Si nanowires is currently being pursued.

It has been duly noted that the micro-/nanopillar-based structures offer the potential for trapping incident photons through subwavelength diffractive effects between the pillars and multiple reflections in the dense network, resulting in a high absorption of photons in the active absorption materials [69]–[72]. We measured the optical transmission of the transferred Si micropillars in KMPR, PDMS, and PMMA using an Ocean Optics spectrometer with normal incident light from 400 to 900 nm. The results presented in Fig. 7 show that the transfer

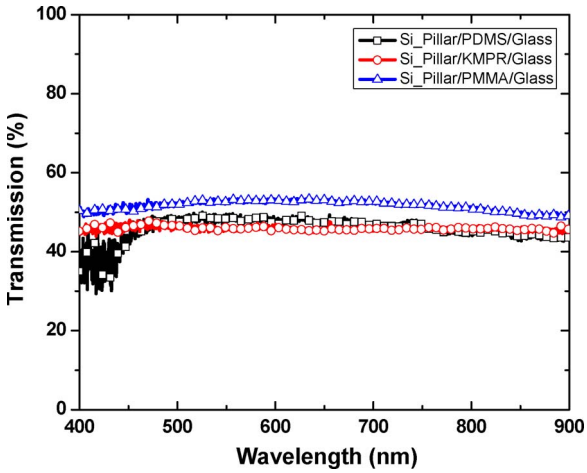

Fig. 7. Optical transmission data at normal incidence for the transferred devices in the shape of micropillars onto the respective polymer-coated carrier substrates. The transmission curve of each sample is normalized to its individual reference without the device (micropillars). The devices on each sample absorb a fraction of incident photons, reducing the total transmission. (-●-) Transmission spectrum of Si micropillars embedded in KMPR coated on a glass substrate. (-□-) Si micropillar embedded in PDMS coated on glass substrate. (-Δ-) Si micropillar embedded in PMMA coated on a glass substrate.

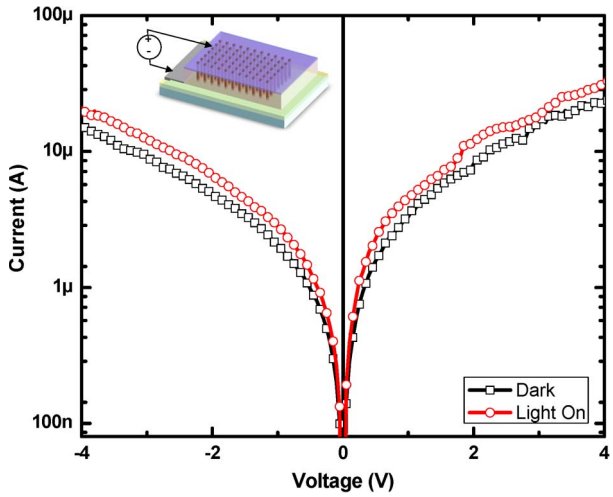

Fig. 8. Electrical current-voltage (I–V) measurement of the transferred Si-micropillar photoconductor with and without optical illumination (of white light) subsequent to contact formation. There is an increase in photocurrent averaged about ∼35% at ±4 V. The intensity of the light is < 5 mW/cm^2. The I–V curves show electrical continuity and demonstrate the feasibility of electrical interfacing of the semiconductor devices in the shape of vertical pillars with flexible electrode materials: Ti/PAni (bottom electrode) and Au (top electrode) during and subsequent to the transfer process. (Inset) Schematic of the test structure.

of silicon micropillars has increased the absorption properties of the carrier substrates for the wavelength of interest. This high absorption and reduced reflectance ($< 5\%$) are very important for enhancing the efficiency in optical detectors and solar cells. The phenomenon of significant light trapping offers enormous opportunity for designing novel micro-/nanopillar-based photonic devices with simpler physical structures and better performance. The absorption can be further enhanced by increasing the fill factor and fabricating the pillars with nonuniform diameter along the length [73].

Characterization was done to study the electrical connectivity of the transferred pillars in PMMA with a conducting polymer/metal composite. Fig. 8 shows the current-voltage (I–V) characteristics of electrically connected ordered Si micropillars under optical illumination (white-light intensity < 5 mW/cm^2). The bottom electrode is a PAni/Ti bilayer, and the top electrode is a thin Au film probed by Osmium probe tips. The I–V curves for the dark and photocurrents demonstrate the feasibility of interfacing the semiconductor pillars with electrode materials during and subsequent to the transfer process. At present, the unoptimized conducting polymer composite demonstrates a large contact resistance with the embedded Si micropillars compared to that of metal–Si ohmic contacts [74], [75] due to inefficient electron exchanges between semiconductor and electron/hole-transporting polymers [76]. Efforts are currently underway to decrease the contact resistance by optimizing the conducting polymer-metal composite and forming a thermoplastic metal nanoparticle conducting polymer [77].

The fracture transfer process employing three different polymers has been shown to reproducibly preserve the integrity of aligned micropillar patterns during transfer from a rigid mother substrate (wafer) to an integrated multimaterial-based device platform. This process is particularly desirable for transferring highly crystalline materials to a wide variety of substrates. It offers several important features such as the following: 1) device fabrication with highly crystalline materials at low temperature to minimize the impact of thermal expansion and shrinkage (specifically important when devices are fabricated on plastics, textile, and other low-cost substrates and in a multilayer stack with different semiconducting MNPs connected via several layers of conducting materials); 2) low fill factor potentially contributing to lower leakage current and reduced parasitic capacitance; 3) higher efficiency of light absorption due to path-length enhancement through effective phototrapping; and 4) reusability of expensive substrate for repeated reproduction of 1-D pillars contributing to significantly reduced material consumption. It is also well identifiable that our approach offers a more general method in that the ordered array of 3-D micro-/nanostructures is preserved in their vertical orientation (direct 3-D to 3-D) after transfer with an increase in the volume density of the final device compared to 2-D film transfer. The choice of the transfer polymers (mainly insulating polymers) from off-the-shelf products is not limited to PDMS, PMMA, polyimide, polystyrene, polycarbonate, or SU-8.

IV. Conclusion

We have demonstrated the fabrication of a dense array of semiconductor pillars and developed the processes for applying both insulating and conducting polymers for transferring and electrically interfacing the devices on a secondary substrate for further postprocessing. Transfer of an area of ∼25 mm^2 was obtained for simple photoresistive devices on a glass and a flexible polymer surface. This method allows the saving of the original single-crystal substrates for repeated generation of single-crystal devices contributing to lower cost of device fabrication. With the development of high-performance soft-contact materials for interfacing 1-D semiconductor pillars, this technique will lead to 3-D heterogeneously integrated device manufacturing concepts by integrating multiple elemental, compound, and organic semiconductors on a wide range of

substrates for significantly low-cost, flexible, and portable applications, including energy conversion, data storage, imaging, solid-state lighting, displays, tactile sensing, and silicon photonics.

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