Proceedings of 2005 5th IEEE Conference on Nanotechnology
Nagoya, Japan, July 2005

Dramatically Improved Yields in Molecular Scale Electronic Devices Using Ultra-smooth Platinum Electrodes Prepared By Chemical Mechanical Polishing

M. Saif Islam,† Z. Li, S-C Chang, D. A. A. Ohlberg, D. R. Stewart, S. Y. Wang and R. Stanley Williams

Quantum Science Research, Hewlett-Packard Laboratories, 1501 Page Mill Rd, Palo Alto, CA 94304, USA

†Integrated Nanodevices and Systems Research, Electrical and Computer Engineering, University of California, 3139 Kemper Hall, Davis, CA 95616, USA Fax: (530) 752-8428, Email: saif@ece.ucdavis.edu

***Abstract* — We report a dramatic improvement in the yields of molecular scale electronic devices by using ultra-smooth platinum (Pt) electrodes made with chemical mechanically polishing (CMP). A large number of measurements were carried out in order to investigate the surface roughness of freshly deposited Pt films using atomic force microscopy (AFM) and a root-mean square (RMS) roughness of 7Å was observed. We developed and applied a CMP process to achieve ultra-smooth Pt surfaces with less than 1Å RMS roughness and grew two different types of molecular monolayers, i.e. SAMs of alkoxynaphthalene thiols and Langmuir-Blodgett (LB) monolayers of eicosanoic acid on polished Pt electrodes defined by optical lithography. Using AFM, contact angle measurements and ellipsometry, we observed a dramatic improvement in the packing and orientation of both types of monolayer. An impressive 100% device yield in the molecular devices made of LB monolayer and ~35% yields in the devices made with SAM monolayer of alkoxynaphthalene thiols molecules with device sizes varying from 1μmx5μm to as big as 20μmx5μm were observed.**

***Index Terms* — Molecular electronics, CMP, SAM, Langmuir-Blodgett, Device yields.**

I. Introduction

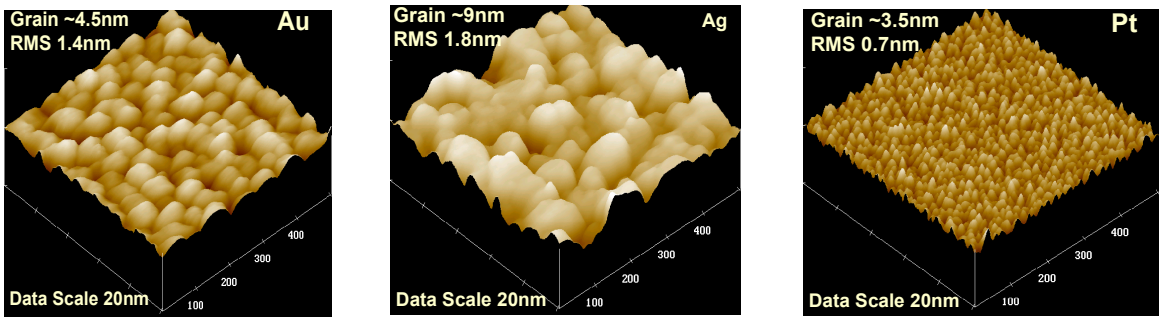
Molecular scale electronics has a potential of becoming the building blocks of future memory and logic circuits in which the critical dimension is naturally associated with molecular sizes. Researchers have accomplished and reported significant progress in the fabrication of molecular devices demonstrating tunneling junctions, electrically configurable switches and transistors made from a single molecule. [1-6]. Although considerable milestone has been reached in the development of manufacturable fabrication process, a critical issue of high density of "shorted" and in some cases "open-circuit" devices has raised a strong concern. A defect tolerant architecture has been proposed to overcome the issue of high defect density in the molecular circuits [7]. Researchers have been using nanopores [1], breaking junctions [3], in-situ STM or and AFM [8] for making contacts to molecules in order to make the devices with diminishingly small size. Although a great deal of understanding has been developed using these research based approaches, these are not suitable for massively large array of devices for future electronics with molecules. In this paper, we present our work on a dramatic improvement in the yields of molecular scale electronic devices fabricated with both LB and SAMs and chemical mechanically polished Pt electrodes.

II. Issue of Low Device yields and our proposed solution

We carried out a large number of measurements in order to investigate the surface roughness of freshly deposited platinum (Pt) films using atomic force microscopy (AFM) and observed a root-mean square (RMS) roughness of 7Å. In addition, the average height of the grains on the freshly deposited Pt surfaces was measured to be around 30Å with a high density of more than 50Å high grain clusters. Fresh surfaces of silver (Ag) and gold (Au) metal films were also measured and even larger grains were observed. The height of the grains in all these surfaces is much larger than that of molecules and we believe it is a potential cause of device shorting in molecular scale electronic devices. If a method of metal deposition can be developed that will ensure atomically flat surfaces (such as ~1Å level RMS roughness) suppressing the grain clusters in the electrode surfaces, the shorting issue can be curtailed or completely eliminated. Unfortunately, none of the existing metal deposition process is capable of depositing metal with acceptable roughness suitable for the fabrication of molecular device.

The CMP process for conventional microelectronics industry has experienced an ongoing development over several years and a great deal has been accomplished in terms of precise control of removal rate, surface smoothness, reduced micro-scratches, local and global

0-7803-9199-3/05/$20.00 ©2005 IEEE



(a) (b) (c)

Figure 1: AFM topographies and surface plots of freshly deposited Au (a), Ag (b) and Pt (c) surfaces. Ag film is the roughest one with average grain size of ~9nm. The grain size of Au is ~5nm and Pt is ~3.5nm.

uniformity. Although feature sizes are shrinking to diminishingly small dimensions, the devices and interconnects in a microprocessor or memory array are much larger than the residual surface roughness that an optimum CMP process can offer today. However, as the device feature size further decreases and research community looks for alternative materials for electronic devices; such as DNA, organic molecules or carbon nanotubes; the requirement for CMP is going to be more stringent and the traditional CMP process will need to go through enormous improvements to be applicable in the fabrication of nanodevices. New types of metals such as Ag and Pt are being increasingly explored in the research community. Many of the future nano-devices are expected to be smaller than the typical grain-size of freshly deposited metals.

Figure 1 depicts the surface topology of freshly deposited (a) Au, (b) Ag and (c) Pt surfaces. Clearly, the grain-sizes are larger or comparable to the sizes of typical molecules used in molecular electronic devices and there has been an issue of extremely low device yields due to shorting caused by the spikes and grains of freshly deposited metals. A mechanism is needed to eliminate the surface roughness of metals in order to fabricate predictable and repeatable nano-devices.

III. Chemical Mechanical Polishing for Electrode Fabrication

We developed a two step polishing scheme using two different slurries for generating ultra-smooth Pt surfaces. First, we applied a low pressure mechanical polishing process using a colloidal silica (SiO_2) slurry (Cabot SS-12) and grind-reduced the size of the grains of Pt by ~50%. The average grain size has been reduced from 3.5nm to 1.2nm and sharp spikes have been considerably eliminated. This polishing step involved only mechanical polishing due to the chemistry of the slurry which was designed for SiO_2 planarization.

In the second stage of polishing the Pt surfaces, we used proprietary colloidal alumina slurry made by DuPont-EKC (ZCX-206) with an oxidizer (ZCX-206B) mixing with a ratio of 3:7. Pt is difficult to remove due to a very slow oxidation rate and require a long polish time. An average removal rate for Pt was found to be ~2nm/min with a pressure of ~2PSI on a 4" wafer. In both the steps of polishing, we used a slurry flow rate of 250ml/min, a rotational speed 35rpm for both polishing plate and wafer carrier. A 50% sweeping was applied during the polishing process maintaining a low frequency. A pad (Rodel IC-1000/Suba IV) with concentric grooves and a soft bottom provided uniform instantaneous pressure distribution at the wafer-pad interface. In-situ conditioning of the pad was employed during polishing process to ensure elimination of agglomeration of slurry particles. Although the removal rate was found to be extremely slow, we observed an effectively complete elimination of roughness from Pt surfaces applying a polishing process for ~2 minute. No end point detection was used in our polishing process. The focus was to generate ultra-smooth surface. Details of the polishing process are described elsewhere [9].

With the application of an optimized polishing process, we achieved better than 0.1nm RMS roughness in Pt surfaces with an average grain size of 0.5nm as shown in Figure 2. A within-wafer-non-uniformity of ~15% has also been measured in 4" wafers.

In order to fabricate molecular electronic devices with SAMs of alkoxynaphthalene thiols and Langmuir-Blodgett (LB) monolayers of eicosanoic using the ultra-smooth Pt electrodes, we deposited monolayer of molecules on two different substrate containing optical lithographically defined dog-bone shaped bottom Pt

electrodes. A shadow mask was used to delineate the top electrode with Ti metal. For the purpose of characterizing the monolayers grown on polished Pt surfaces, we used 4" Si wafers coated with a 1000Å of thermally grown SiO_2 layer and grew molecular monolayers using both LB and SAMs.

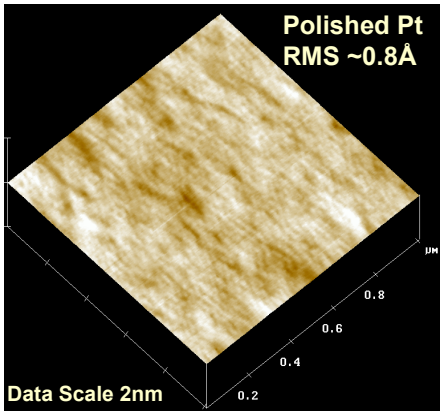


Figure 2: AFM topographies and surface plots of a polished Pt surface. The grain size of polished Pt is less than 1nm making it a very suitable for molecular scale electronics.

IV. Results and Discussions

We measured the water contact angle of SAMs of alkanethiolates with varying carbon (C) lengths. Figure 3(a) shows the contact angle for water on SAMs deposited on Pt surfaces. The water contact angles appear to be 111±2° when the carbon number of the alkane chain is larger than 10 and 12 for the monolayers on CMP Pt and fresh-deposited surface, respectively.

Optical ellipsometry was applied as a convenient and precise means of determining the average monolayer thickness of the films and following the progress of film growth. The ellipsometric thicknesses of monolayers of alkanethiols on both polished and unpolished Pt surfaces are collected in Figure 3(b). The film thicknesses of SAMs on gold are shown as a reference. The abscissa is the number of the carbon in alkanethiols. This observation suggests that no multilayers of thiols are present on the platinum surfaces. The best fit to the lines gives a slope of 1.43 and 1.57 Å per CH_2 for the SAMs of alkanethiolates on fresh-deposited and CMP Pt, respectively. These slopes are greater than that for SAMs on gold surface (1.13 Å per CH_2) indicating that alkanethiols on Pt surfaces are more perpendicular to the surface normal than gold surface. These observations, similar to alkanethiols on plasma-treated platinum surfaces, suggest that well packed thin films are formed on polished Pt surface.

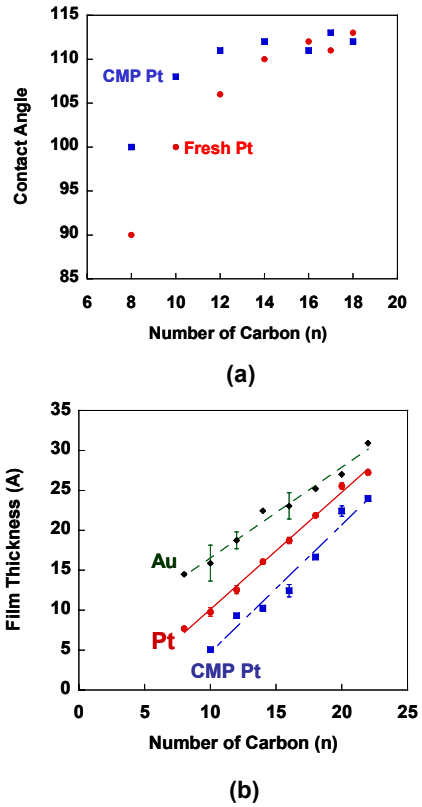


Figure 3. (a) Contact angle for water on SAMs of alkanethiolates appear to be 111 ± 2° when the carbon number of the alkane chain is larger than 10 and 12 for the monolayers on CMP Pt and fresh-deposited surface, respectively. These observation suggest that well packed thin films are formed on CMP Pt. (b) Thickness of monolayers of alkanethiolates on freshly deposited platinum (●), CMP Pt (■) and gold (◆) as a function of the number of carbon atoms (n) in the alkane thiol molecules.

Crossbar molecular devices were fabricated using patterned and polished electrodes and were measured using a semiconductor parameter analyzer in room temperature after the ''burn-in'' step, similar to that reported in [5]. The switching voltage for LB was ~2V as shown in Fig 3 and for LB film, it was ~1V. The resistance, before and after the switching is ~2kΩ and 4GΩ respectively. The molecular scale devices were found to switches with similar a characteristic as shown in Figure 4. We observed an impressive 100% device yield in samples with LB monolayer. Around 20 devices were measured with device sizes varying from 1µmx5µm to as big as 20µmx5µm. Previously more than 50% devices made with LB films with such sizes would short. This demonstrates significant improvement in device yield with polished Pt surface. On the other hand, around 35% of the 40 devices we tested with SAM monolayer of alkoxynaphthalene thiols molecules showed a diode like I-

V characteristics demonstrating a remarkable improvement in the device yield given that all of our previous yields were less than 5% even when electrode with extremely narrow dimension was used. We also used XPS survey scan of bare CMP-Pt and SAM of $C_{18}SH$ coated CMP-Pt to evaluate the surface cleanliness. Although there is a negligible trace of N_2 in the post-CMP surfaces, SAM could effectively remove the N_2 atoms ensuring a clean surface.

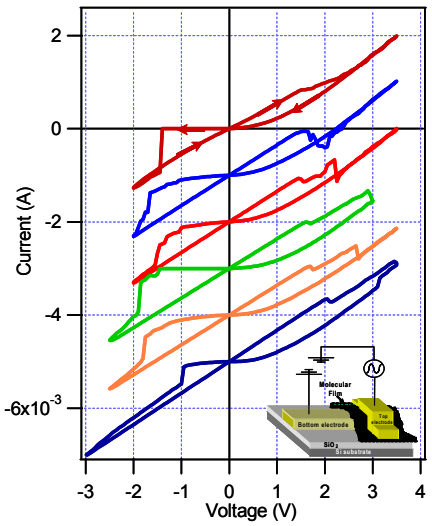


Figure 4. Electronic characteristic of a nanoscale molecular device with SAM of of alkoxynaphthalene thiols on polished Pt electrodes. The I-V curves are vertically shifted for clearer presentation. The resistance before and after the switching are ~2kΩ and 4GΩ. The inset shows the way a monolayer is sandwiched between two electrodes. The bottom electrode is the polished one.

Self-assembled monolayers (SAMs) of molecules form spontaneously on solid surfaces and offer the promise of low cost and thermodynamically driven speedy assembly for future ultra-dense electronic circuitry. It is widely known that a SAM is resistant to the intrinsic surface reconstruction, a widespread phenomenon that frequently causes rapid randomization of surface atoms. The dramatic improvement in the yields of the devices especially with SAM films will play an important role in designing reliable devices and circuits with molecular scale switching devices.

V. Conclusion

We demonstrated a huge improvement in the yields of molecular scale electronic devices by using ultra-smooth platinum (Pt) electrodes prepared with a CMP process developed for generating atomic scale surface roughness. An ultra-smooth Pt surfaces with less than 1Å RMS roughness was fabricated and two different types of molecular monolayers, i.e. SAMs of alkoxynaphthalene thiols and Langmuir-Blodgett monolayers of eicosanoic acid was grown on them. We observed a dramatic improvement in the packing and orientation of both types of monolayer. An impressive 100% device yield in the molecular devices made with LB monolayer and around 35% yields in the devices made with SAM of molecules with device sizes varying from 1μmx5μm to as big as 20μmx5μm were observed. Our results indicate the all-trans and well-ordered molecular mono-layers on CMP metal surface can go a long way to solve the existing yield issue of molecular devices making it stronger candidate for future ultra-high density functional nano-electronic circuits.

Acknowledgement

This work was partially supported under DARPA agreement MDA972-01-3-0005.

References

[1] M. A. Reed, C. Zhou, C. J. Muller, T. P. Burgin, and J. M. Tour, "Conductance of a Molecular Junction", *Science* vol. 278, p252, 1997.
[2] C. P. Collier, E. W. Wong, M. Belohradsky´, F. M. Raymo, J. F. Stoddart, P. J. Kuekes, R. S. Williams, and J. R. Heath, "Electronically Configurable Molecular-Based Logic Gates", *Science*, vol. 285, p391 1999.
[3] J. M. Tour et al., *J. Am. Chem. Soc*. vol 117, p9529.
[4] D. R. Stewart et al, *Appl. Phys. Lett*. Unpublished.
[5] Y. Chen et al, "Nanoscale molecular-switch devices fabricated by imprint lithography", *Appl. Phys. Lett*., 82 (10) p1610, 2003.
[6] Y. Chen et al, Nanotechnology,vol 14, p462, 2003.
[7] J. R. Heath et al, "A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology" *Science,* Vol. 280, p1716, 1998.
[8] G. Yang and G-Y Liu, "New insights for self-assembled monolayers for organothiols revealed by scanning tunneling microscopy", *J. Phys. Chem. B*, 107, p8746, 2003.
[9] M. Saif Islam, G.Y. Jung, T. Ha, D.R. Stewart, Y. Chen, S.Y. Wang, R. Stanley Williams, "Ultra-smooth platinum surfaces for nanoscale devices fabricated using chemical mechanical polishing", *Applied Physics A*, *Special Issue on Nanotechnology*, March, 2005.