Determination of Surface Depletion Thickness of p-doped Silicon Nanowires Synthesized Using Metal Catalyzed CVD Process

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Abstract— **An in-depth understanding of the distribution and impact of doping in nanowires is crucial for the rational design of future nanowire based devices synthesized using bottom-up techniques. We used a very slow wet chemical etchant for progressive reduction of the diameters of boron-doped, metal-catalyzed silicon nanowires with diverse diameters and lengths. The low temperature process helped avert the dopant segregation which is common in high temperature processes such as oxidation for diameter reduction. We ensured identical surface conditions subsequent to diameter reduction with wet-chemical etching and, using DC current-voltage measurements, found the resistance to increase with decreasing diameter. As the diameters were shrunk from a larger diameter to ~50 nm in diameter, they exhibited a strong non-linear increase of the resistance indicating complete depletion of the cross-section caused by surface charges. The dopant concentration of the nanowires was calculated to be $2.1x10^{18}$ cm^{-3} and the corresponding surface charge density was around $2.6x10^{12}$ cm^{-2}.**

Keywords-component; nanowires, doping distribution, surface depletion, impurity distribution

I. INTRODUCTION

Almost forty years after the first demonstration of nano-whiskers as reported by Wagner in 1964 [1], celebrations of this low-dimensional structure abounds. The principal story of this unique structure has long centered on the fundamental aspects of synthesis in various material systems and opportunities for novel devices with several ground breaking demonstrations [2, 3]. There have been an upwelling of recent interest in nanowires' electronic, optical, mechanical, chemical, piezo-resistive and other properties motivated by opportunities for further miniaturization of electronic devices, memory, logics, chem-bio sensors and other novel electronic and photonic devices. The capability of highly rational synthesis related to self-assembly property and the ability to synthesize nanowires with controlled characteristics (versus the hit and miss control over, say, carbon nanotubes) have made it a very suitable candidate for future nano-electronics.

Motivated by numerous potential applications, a large number of studies of devices on nanowires have been carried out in the recent past. However, although some consensus on the dominant mechanism of the device properties seem to be emerging, a complete understanding is not yet free from controversy. This happens due to the fact that most scientific experiments have been ignoring some inherent aspects of nanowire properties.

Surface properties of the nanowires play a very important role in the electrical properties of devices such as field-effect sensors or transistors. Nanowire based sensors hold great promise for detection of biological and chemical species. The detection is based on the principle of field-effect transistors (FETs) in which doped nanowires are used and the gating is achieved chemically by varying the surface charges when a species binds on the surface leading to the conductance variations. In general, the variation of either the resistance or capacitance of the sensor is measured and both properties are directly related to the surface charges. Unlike bulk surfaces, where the change in the structure are limited to the surface, the presence of a molecule impacts the carriers deep inside the core of the nanowire and this is why sensitivity of nanowire based sensors is dramatically higher. Therefore, it is important to know the surface charges and the resulting depletion layer thickness of nanowire based field effect devices, such as MOSFETs and sensors for optimal operation. Doping contributes to variations in the surface properties of a nanowire contributing to the variations in the electrical properties of devices such as field-effect sensors or transistors.

Electrical and optical properties of nanowires are usually measured by making contacts to nanowires placed on an insulating substrate, which is usually an oxidized silicon wafer. Placing nanowires on an insulating surface, however, cannot completely eliminate the unwanted current paths. For accurate measurements of the intrinsic properties, the nanowires need to be free from contact with any object and to be surrounded by nonconductive material to eliminate possible artifacts attributed to current paths other than those through the nanowires themselves. An ideal solution to this problem is direct lateral growth of nanowires in the form of suspended bridges between two pre-fabricated electrodes. Recently, we introduced such a bridging technique that connects a large number of highly oriented, suspended metal-catalyzed silicon nanowires between two electrodes to design nanodevices that could be integrated with modern electronic fabrication

technologies [4, 5]. In this work, we used our suspended nanowires between two electrically isolated, prefabricated silicon electrodes to avoid interaction of the surface of the nanowires with the surroundings.

II. EXPERIMENTAL METHOD

A silicon-on-insulator (SOI) wafer with 7 µm thick device layer and 150 nm thick buried oxide layers was used to fabricate the electrodes as described in Ref. 5. After fabricating the electrodes, a ~1 nm thick gold layer was deposited on one of the sidewalls of the electrodes. This layer acted as the catalyst for the growth of silicon nanowires. The sample was initially heated in a chemical vapor deposition (CVD) chamber in a hydrogen rich environment to form Si/Au alloy nanoparticles. These nanoparticles acted as catalyst for the growth of nanowires. Then the temperature was set to 640° C for the growth of nanowires. SiH_4, HCl and diborane (B_2H_6) gases were introduced into the chamber. While SiH_4 was used for the growth of nanowires, B_2H_6 was used for p-type doping. The nanowire grows across the gap toward the (111)-oriented side wall of the opposing electrode. When the nanowire reaches the opposite side wall, it is epitaxially bridged to the sidewall by continued catalyzed decomposition. Details of the process are described in Ref. 5.

Figure 1(a) and 1(b) shows the schematic of a nanowire fabricated between silicon electrodes and a top-view SEM image of one of the measured devices with a bridged nanowire. Current-voltage (*I-V*) characteristics of the nanowires were

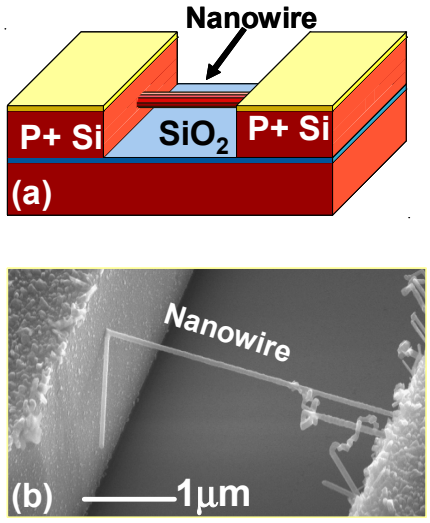

Fig. 1. (a) Schematic of device with a bridging nanowire. (b) SEM image of one of the devices from the top of electrodes.

measured by simultaneously applying DC voltage between the electrodes, and measuring current through the nanowires. The resistance between the probes and the electrodes was negligible with respect to the resistance of the nanowires (less than 0.1%). The current-voltage characteristics of the nanowires were linear, which shows that the nanowires made good electrical contact to the silicon electrodes [5]. The resistance between two un-bridged electrodes was measured to be 200±40 GΩ, which are more than two orders of magnitude higher than the resistance of nanowires throughout the size reduction experiments. Six devices with different number of nanowires were selected with diameters ranging from 90 nm to 160 nm. Most of the nanowires were found to be cylindrical, and some of them were tapered. For the most tapered nanowire, the diameter at the tip was 72% of the diameter at the root. Diameter reduction of the nanowires was done with successive isotropic silicon etching and native oxide etching.

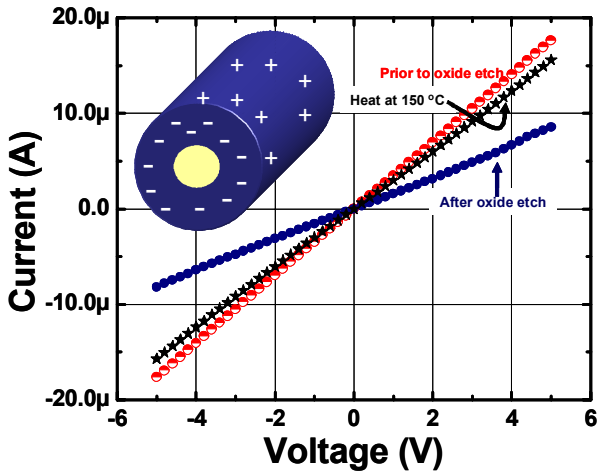

Fig. 2. The linear I-V characteristics of a nanowire during the native oxide etch and the heat treatment processes. The schematic shows a p-doped nanowire with positive surface charges and depleted region. There is a charge balance between positive surface charge and negative space charge in the depleted region.

We developed a low etch-rate isotropic etchant for silicon based on HF-HNO_3-CH_3COOH (HNA) solutions for isotropic etching of silicon at room temperature. The details of the etching process will be discussed elsewhere [6]. Initially we treated the devices with HF based native oxide etchant to observe the effect of H^+ ion rich solution on the resistance of the nanowires. As our nanowire was p-doped, positive surface charges created a depletion region close the surface of the nanowire. This reduces the conducting cross-sectional area of a nanowire. High concentration of hydrogen on Si nanowires terminates the dangling bonds of Si atoms on the nanowire surface and further increases the concentration of positive charges. After the HF treatment, we observed that the resistance of the nanowires increased. The increase is attributed mainly to the H^+ ions adsorbed to the surface of the nanowires [7]. The additional positive charges on the surface of p-doped nanowires increases the depletion layer thickness, which in turn decreases the cross-section area of the conductive inner core as shown in Figure 2. After the HF treatment, the resistance remained unchanged for more than 7 days if the devices were kept at room temperature. We heated the devices in an uncontrolled room ambient to sever the bonds between the surface and the hydrogen ions, which decreased the positive charge density by desorbing H_2 from the surface. The devices were heated at 120, 150, and 180 °C for 1 minute. We did not further increase the temperature or the duration of heating in order to avoid any dopant segregation, which typically starts around 500 °C for bulk Si wafer surfaces. As the temperature was increased, we

observed a decrease in the resistance of the devices. Most of the devices were found to approach their initial resistance values, consistent with modification of surface charges by etching and annealing. Figure 2 and 3 show the results of current-voltage (I-V) measurements, and the corresponding resistance values. Immediately after each I-V measurement, the diameter and the length of the nanowires were measured with high-resolution SEM. The sample was then kept in an uncontrolled room environment for about two months and the resistance was measured again. We observed an increase of 30% in the resistance, which we attribute to oxidation of the surface contributing to the reduction of nanowire diameter. Formation of native oxide reduces both interface states and trapped charge by completing bonds at the oxide-silicon interface and terminating many of the remaining dangling bonds with hydrogen. As a result, the density of positive surface charges caused by the p-doping experience a relative increase. We estimated the thickness of the oxide layer to be ~3 nm.

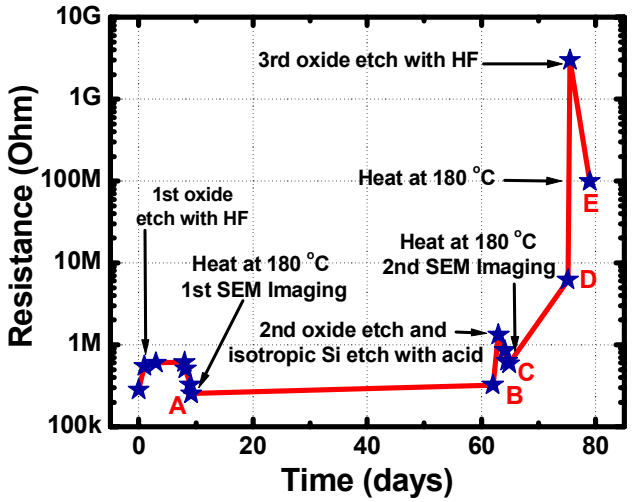

Fig. 3. Resistance of a measured as a function of time. As the diameter was reduced, the ratio of the resistance after the etch to the resistance before the etch increased, which shows that the increase of the depletion layer thickness due to additional H+ charges becoming more effective in increasing the total resistance. The identical states of the surface are indicated by letters; A, C, and E correspond to low surface charge state after the etching steps, B, and D correspond to surfaces with native oxide.

At this point, we used isotropic Si etch solution to reduce the diameter of the nanowires. Before applying the silicon etchant, we removed the oxide layer from the surface of the nanowires using diluted HF. We then etched the devices in isotropic silicon etch solution for about 1.5 sec and applied heat treatment similar to the previous case. As expected, the resistance of the device increased to a very high level after the isotropic etch due to the drastic reduction of the diameters of the nanowires and increase of surface charge caused by removal of oxide layer. With subsequent heat treatment the resistance decreased further, as shown in Figure 3. SEM measurements indicated that the diameters of the nanowires were reduced by ~37 nm. This showed that the etch rate of nanowires with the isotropic silicon etch solution was around 10 nm/sec, which was about 13 times faster than that of bulk silicon wafers. It is not clear yet why the etch rate of Si nanowires was more than an order of magnitude faster than that of bulk Si wafer. Several possibilities including the circular cross-section that causes different liquid-solid interface compared to a plane semi-infinite surface, catalyst assisted growth of nanowires at low temperature (~640 °C in our experiments) or the presence of catalysts (Au in this experiment) throughout the nanowire stem (as was reported by Perea et. al [8]) need to be investigated. Because of the high etch rate of the isotropic silicon etch solution, the final etch used for the wire thinning experiments was an oxide etch instead of the silicon etch. After the previous etch step, devices were exposed to air for 10 days, which was enough to form ~2 nm thick oxide layer on the surface, then etched using the oxide etch solution. The resistance of the devices increased after the native oxide etch, and decreased as the devices were heated, as observed in the previous etch steps.

III. RESULTS AND DISCUSSIONS

The results of diameter reduction by etching are shown in Figure 3 which shows the resistance of one of the devices measured during the size reduction process. Similar characteristics were also observed for other devices. The total process consisted of three etch steps followed by heat treatments. After etching and heating the devices at 180 °C, we assume that identical surface conditions are achieved as similar amount of H^+ ions were present in the etchant solution (points A, C, and E in Figure 3). Figure 4a shows the resistance per nanowire for the 6 devices used in the measurements. It is clear that the resistances of the nanowires increased as the diameters were reduced through steps A to E contributing to a reduction in the cross-section area of the conductive inner volume. We observed a nonlinear increase in the resistance of the nanowires as we did the final native oxide etch (Figure 4a). Although the amount of the reduction in the diameter was quite low when compared to the isotropic etch step, the effect of this final etch on the nanowire resistances was dramatically high. We calculated the ratio of resistance between steps C and E. Figure

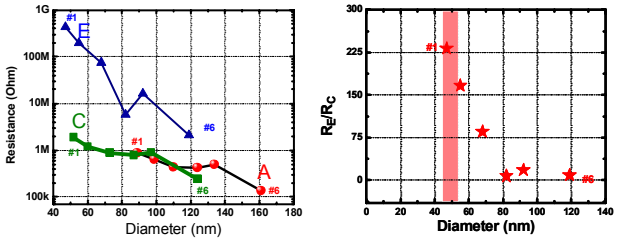

Fig. 4. (a) The resistance of 6 devices measured at process steps indicated by A (-●- after 1st oxide etch), C (-■- after isotropic silicon etch), and E (-▲- after 3rd oxide etch). (b) The resistance ratio of the devices after the final etch to the isotropic silicon etch. Although this ratio is almost same for large area nanowires, a non-linear increase can be seen for small area nanowires. This non-linear increase is due to the nearly complete depletion of the small-area nanowires. The shaded area shows the range of diameter over which the nearly complete depletion was observed.

4b shows that ratio (R_E/R_C) as a function of the nanowire diameter. It is seen that the resistance of small nanowires (two devices which had 47 and 55 nm final diameters respectively) increased more than 2 orders of magnitude in the final etching step. This is an indication of near complete depletion of the nanowires. We concluded that the depletion layer thickness for small area nanowires was around 25 nm for the surface charge corresponding to state E. The depleted layer occupies the majority of the volume, and the conductive cross-section area is much less than the physical cross-section for the nanowires, with the depletion layer thickness comparable to the nanowire radius.

By assuming a uniform density of dopant atoms throughout the cross-section of a nanowire, we estimated the doping concentration of the nanowire. The resistance of the nanowire is given by:

$$R = \rho \frac{L}{A_{con}} = \rho \frac{L}{\pi\left(\frac{d}{2} - \delta\right)^2}$$

where A_{con} is the cross-section area of the conductive region, ρ is the resistivity of the nanowire, d is the diameter of the nanowire, and δ is the depletion layer thickness. After calculating the resistivity, we estimate the dopant concentration to be $(2.1\pm0.60) \times 10^{18}$ cm^{-3}. It has previously been observed that the resistivity of highly doped Si nanowire is very similar to bulk silicon [9] and we also used the resistivity of bulk silicon to find the corresponding doping concentration of nanowires. The total charge of the nanowire is zero, which implies that the charges in the depleted region should be equal to the surface charges. Given the estimate for N_A above, the surface charge density is found to be $(2.6\pm0.75) \times 10^{12}$ cm^{-2}. This value is one order of magnitude higher than the value measured for the bulk silicon wafer [10]. Higher value of surface charges could have been caused by fixed oxide charge located in the ~3 nm of the SiO2-Si interface. In general, positive charges are trapped by imperfect oxide (Si rich) or by oxygen atom that lost an electron. In addition, the planes that bound the Si nanowires are not exactly of any particular orientation at the curvatures and trapped charges density might be higher in these regions. We also don't know if the dopant concentration is uniform or not across the nanowire cross-section. Any non-uniformity is likely to result in a uncertainty in the surface charge density.

By reducing the diameter of CdSe nanoparticles, it has been previously observed that the dopant atoms of Mn were higher in density close to the surface [11]. It is not clear yet how the dopant profile in Si nanowire is. Our experimental method of gradually reducing the diameter of nanowire would shed light on this significant aspect of nanowire. The knowledge of impurity profile in nanowires will be crucial for rational design of nanodevices based on nano-structures.

IV. CONCLUSION

In conclusion, we developed a slow isotropic silicon etchant to reduce the diameter of nanowires in room temperature. By comparing the resistance of nanowires with identical surface conditions throughout the etching process, we found a depletion layer thickness of ~25 nm for the nanowires doped to ~ 2.1×10^{18} cm^{-3}. Our observation indicates that a non-negligible depletion layer thickness is present in the doped silicon nanowires and it needs to be carefully evaluated for designing nanowire-based devices. In our work, we assumed a constant radial dopant profile. However, a careful study is needed to determine the actual dopant profile in the cross-section of a nanowire with cylindrical symmetry. More investigation on the impurities of p and n-doped nanowires will open door to an accurate understanding of dopant distribution and will facilitate the prediction of device properties with high precision. The results of this work will aid in the development of 1D nanowire based devices and circuits for future electronic and photonic systems.

V. ACKNOWLEDGMENT

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