Scaling Self-Timed Systems Powered by Mechanical Vibration Energy Harvesting

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Passive energy harvesting from mechanical vibration has wide application in wearable devices and wireless sensors to complement or replace batteries. Energy harvesting efficiency can be increased by eliminating AC/DC conversion. A test chip demonstrating self-timing, power-on reset circuitry, and dynamic memory for energy harvesting AC voltages has been designed in 180 nm CMOS and tested. An energy scalable DSP architecture implements FIR filters that consume as little as 170 pJ per output sample. The on-chip DRAM retains data for up to 28 ms while register data is retained down to a supply voltage of 153 mV. Circuit operation is confirmed for supply frequencies between 60 Hz and 1 kHz with power consumption below 130 μW. Reaching the limits of miniaturization will require approaching the limits of power dissipation. We extrapolate from this DSP architecture to find the minimum volume required for mechanical vibration energy harvesting sensors.

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General Terms: Design, Measurement

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1. INTRODUCTION

With the amount of functionality integrated into a single die or package continuing to multiply, the problem of deploying a large-scale wireless sensor

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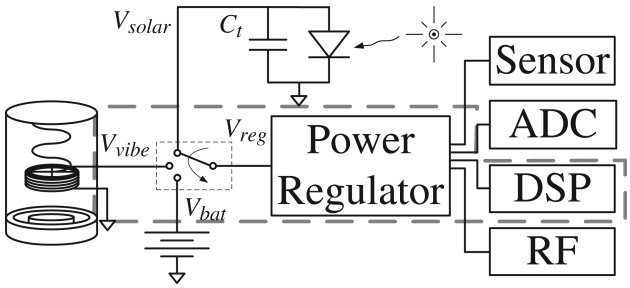


Fig. 1. Block diagram of an energy harvesting wireless sensor node with the power switch, power regulator, and DSP highlighted. Energy sources include solar (V_{solar}), vibration (V_{vibe}), and battery (V_{bat}).

network has become much more tractable. Typically, commercial wireless sensors consume about 70 mW while active and 17 μW when idle [Jiang et al. 2005; Moteiv 2006]. Battery or capacitor energy storage is one option for providing this power, but system lifetime is limited by volume, energy density, and the high maintenance costs associated with battery replacement. A cubic centimeter-sized Li-ion battery can run for about five years at 10 μW, so for a ten-year lifespan we would need to average 5 μW [Calhoun et al. 2005]. An alternative is to harvest energy from environmental sources, such as the sun or mechanical vibrations. Typically smaller sensors are more desirable and these methods can deliver power levels in the microwatt to few milliwatt range in volumes of about 1 cubic centimeter. If power consumption can be reduced then energy can be harvested from the environment while keeping system volume low [Roundy et al. 2003a]. Low-volume, long-lifetime systems are desirable for wireless sensor network applications, such as monitoring industrial machinery or environmental gas detection, and become even more critical for heart rate monitoring, drug delivery, prosthetic actuation, and other Body Area Sensor Network (BASN) applications [Hanson et al. 2009].

Two approaches to energy harvesting include converting mechanical vibration in the system environment to electrical energy for circuit consumption and converting photons to electricity using photovoltaics. Figure 1 shows an example system for an energy harvesting wireless sensor node. It includes multiple power sources including vibration and solar energy harvesting, along with battery or supercapacitor storage. A power regulator interfaces power sources to mixed-signal circuits. The system includes a low-power sensor, such as a carbon nanotube gas sensor consuming 8–185 μW [Amirtharajah et al. 2005; Cho et al. 2007]; an A/D converter using anywhere from 70 pW while idle to 3.1 μW while active [Scott et al. 2003]; a Digital Signal Processor (DSP) requiring 560 nW (at 1.2 kHz throughput, 250 kHz clock [Amirtharajah and Chandrakasan 2004]) to 5.9 μW (at 500 kHz [Warneke and Pister 2004]); and a wireless interface requiring 1 mW for transmission and 450 μW for receiving [Otis et al. 2005]. The average power budget can be maintained in the tens of microwatts range by using very low duty cycle operation for high-power subsystems, such as the sensor and RF circuits. DSP power can be decreased by exploiting the low processing throughput requirements inherent in sensor networks. Power can

be further reduced by increasing the efficiency of the power electronics, which is typically between 18%–85% [Siebert et al. 2005; Guilar et al. 2009b], or by drastically simplifying the power electronics as proposed in this article.

Theoretical and experimental studies on three main types of vibration-based energy harvesting transducers (electromagnetic [Amirtharajah and Chandrakasan 1998; Lee et al. 2003], electrostatic [Meninger et al. 2001; Roundy et al. 2002], and piezoelectric [Roundy et al. 2003b]) indicate that output powers between one and a few hundred microwatts are expected for typical parasitic mechanical vibrations, which have frequencies between 60 Hz and 1 kHz and amplitudes between 2.5 μm and 5 μm. An additional approach is to exploit integrated passive pixels (similar to imager pixels) to form a CMOS photodiode to harvest solar energy. Preliminary experiments show power yields around 225 pW/μm^2 or 5 μW in 150 μm $\times$ 150 μm area [Guilar et al. 2006]. These examples indicate that integrated energy harvesting limits power budgets to the microwatt range in system volumes of about a cubic centimeter, and all circuits, including power electronics, must be designed to fit within this budget.

Low-voltage processors for wireless sensor nodes have been an area of active research. Most proposed solutions operate in the subthreshold region to minimize power consumption but neglect power electronics [Seok et al. 2008; Wang and Chandrakasan 2004; Calhoun and Chandrakasan 2005]. Even when DC-DC conversion is accounted for, the required converter input voltage is lower than what most power sources can provide, thus requiring an additional converter [Kwong et al. 2009]. Interfacing digital circuits directly to the rectified AC voltage output from a mechanical vibration energy harvester avoids complex power electronics, which, if off-chip, increases system cost and volume and incurs losses when converting from AC to DC voltage. Significant computation can be performed with the AC voltage because the supply frequency (60 Hz–1 kHz) is orders of magnitude lower than the datapath frequency. This is in sharp contrast to previous work on RFID tags using a high-frequency AC supply which also provides the clock [Briole et al. 2004]. Such a design precludes circuit optimization for subthreshold operation since functionality must be guaranteed over a wide range of supply voltages, from subthreshold to superthreshold, while minimizing power consumption. Although asynchronous circuits, with large tolerances for process, voltage, and temperature variations, could be considered previous work for AC supplies, they typically do not take into account deliberately time-varying voltages with wide swings [Spars 2001]. Recent work has investigated the use of asynchronous logic in subthreshold operation [Lotze et al. 2001], but because an AC supply can dip below the usable voltage level at any time, requiring a quick power-on when proper levels are restored for brief periods of time [Wenck et al. 2007], asynchronous circuits are a possible starting point, but not necessarily a full solution to the AC supply problem.

This article describes a 180 nm CMOS test chip which implements a digital signal processing module that interfaces directly to an AC supply voltage. A block diagram can be seen in Figure 2. Power regulation has been eliminated completely, except for an integrated CMOS full-wave rectifier [Ghovanloo and

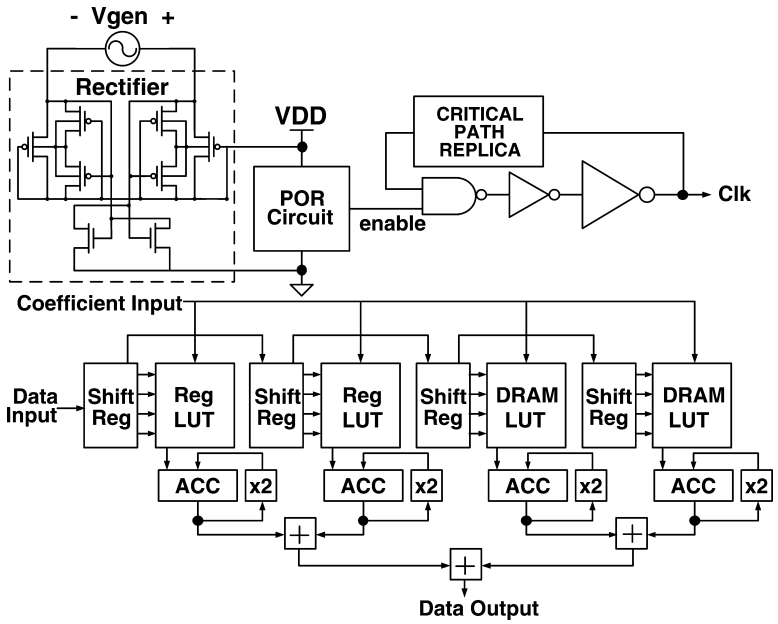


Fig. 2. AC supply test chip block diagram.

Najafi 2004], which supplies a power-on reset circuit with a fast time constant, a critical-path ring oscillator, and a 16-tap programmable FIR filter implemented using a variable-length flip-flop shift register memory and two types of Look-up Tables (LUTs): one based on registers and the other based on a 3T DRAM. Preliminary results from this work have appeared in Siebert et al. [2005], Amirtharajah et al. [2006], and Wenck et al. [2007]. This article expands upon those reports by providing an in-depth discussion of circuit design issues and extensive test chip measurements. Self-timed circuits, especially the power-on reset, are discussed in detail in Section 2, while Section 3 provides a more detailed discussion of robust AC memory design for an energy scalable architecture. The methodology and results from comprehensive experimental characterization of the entire test chip will be presented in Section 4. Section 5 builds on the test chip results to explore theoretical and empirical limits to energy harvesting system miniaturization. Conclusions are presented in Section 6.

2. SELF-TIMING

Typical AC/DC conversion for energy harvesting is 18%–85% [Siebert et al. 2005; Guilar et al. 2009b] efficient due to the circuit overhead of the power electronics and volume constraints that place a lower bound on switching frequency by limiting the size of off-chip passive components. One approach is to change the logic style of the digital circuits to tolerate wide voltage variations from an AC supply. The output of a vibration energy harvester only needs to be rectified using an easily integrated passive circuit, such as a MOSFET

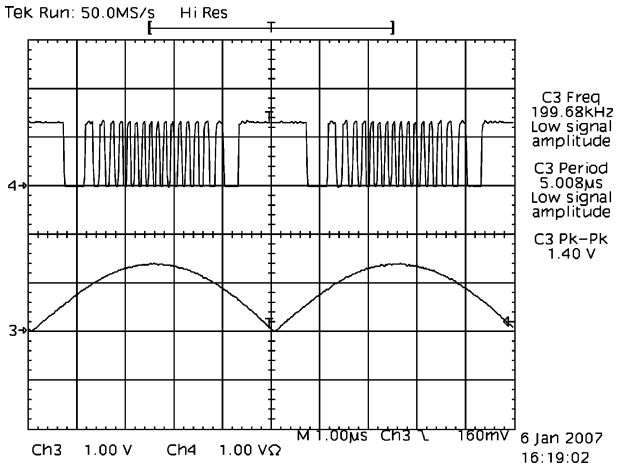


Fig. 3. AC supply input provided by a function generator (bottom) and the buffered ring oscillator's measured output (top) [Wenck et al. 2007].

full-wave rectifier. Total energy harvester system volume can be reduced by minimizing or eliminating the rectifier output filter capacitance. Since the frequency of the AC supply voltage is usually very low, between 60 Hz to 1 kHz, self-timed circuits can be used for the digital blocks since the supply looks like DC on the microsecond to millisecond time scale, which can correspond to hundreds of clock cycles for modern CMOS circuits.

2.1 Self-Timing

For each energy harvesting power supply cycle, the load circuit must power on, perform computation, and turn off. Circuits must also operate correctly over large supply voltage variations. Self-timed circuit design is quite robust under many parameter variations, including supply voltage. The lowest overhead way of implementing self-timing is to use a ring oscillator based on the critical path of the self-timed circuit as shown in the top half of Figure 2. For our design the critical path was a 16-bit ripple carry adder. A replica of the adder critical path was incorporated into the ring oscillator and tracks process, voltage, and temperature variations to guarantee that timing is met throughout the AC power supply cycle. Robustness to voltage and temperature was demonstrated in simulation using a self-timed clock for the Finite-Impulse Response (FIR) filter implemented using distributed arithmetic with 16-bit ripple carry adders [Amirtharajah and Chandrakasan 2004], shown in the bottom half of Figure 2. Performance of the self-timed datapath degrades as supply voltage is reduced, but the datapath still operates correctly. Logic design is identical to traditional synchronous logic design with deep combinational logic networks divided into stages by pipeline registers, but the clock frequency varies.

Figure 3 shows two AC supply cycles and a measured ring oscillator clocking waveform. Once the voltage gets above a certain threshold, the oscillator turns on and the frequency increases as voltage increases and then decreases as the

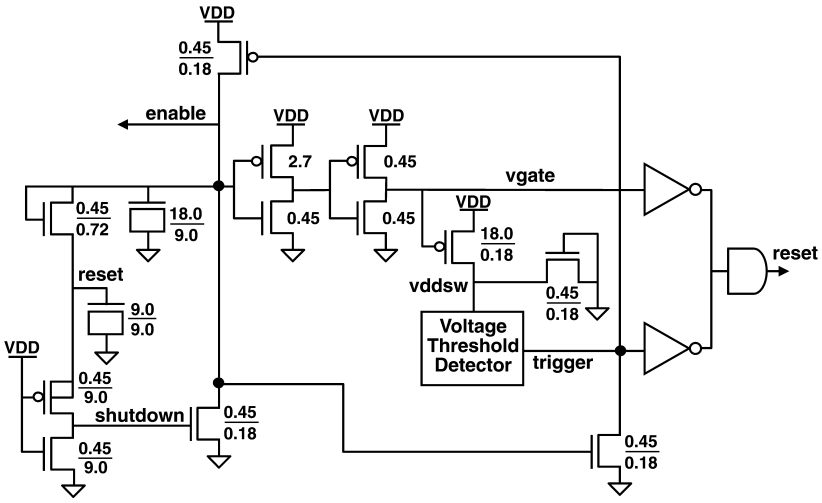


Fig. 4. Proposed power-on reset circuit with fast turn-on transient. An example threshold detector is shown in Figure 5. W/L ratios are given in micrometers.

voltage decreases, eventually turning the clock off. Although not demonstrated in Figure 3, oscillation could begin at different voltages without a Power-On Reset (POR) circuit. To maintain correct system operation, the self-timed datapath must be initialized for each AC supply cycle to ensure a consistent turn-on point for the ring oscillator. This requires a POR circuit that will be introduced in Section 2.2.

2.2 Power-On Reset

A POR circuit for AC supplies ideally turns on in deep subthreshold to maximize the fraction of the AC power supply cycle during which the load circuit operates. To function correctly with a low turn-on voltage for vibrations between 60 Hz and 1 kHz, the POR circuit must generate a reset pulse independent of power supply frequency.

A state machine best illustrates how the POR functions. Consider a state machine with three states defined by two state variables, **reset** and **enable**. When the power supply is below the minimum threshold voltage needed for correct system operation, the circuit is in the INITIAL state and both the **reset** and **enable** signals are low. Once the power supply reaches a high enough voltage it enters the RESET state and **reset** goes high. After a delay, caused by charging a capacitor, the circuit enters the NORMAL state where **reset** goes low and **enable** is high, which allows the ring oscillator and datapath to function [Wenck et al. 2007].

Conventional POR circuits for DC supplies rely on long RC time constants [Yasuda et al. 2001] and potentially consume significant current, which is not acceptable in an energy harvesting context with a time-varying supply requiring fast turn-on. The POR circuit in Figure 4 takes a different approach and

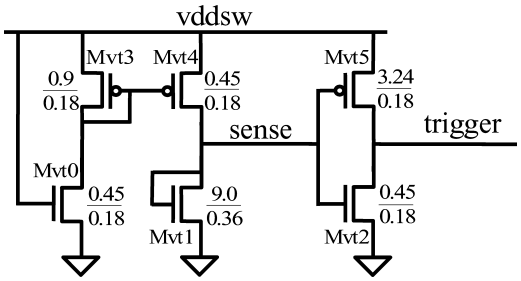


Fig. 5. NMOS threshold $V_{t,n}$-based voltage threshold detector for power-on reset circuit in Figure 4. W/L ratios are given in micrometers [Siebert 2005].

relies on several threshold detection circuits. V_{DD} and the POR **enable** voltages identify the three different states discussed earlier. The initial state (V_{DD} off, POR circuit on, **reset** held low) corresponds to the beginning of a power supply cycle. When V_{DD} crosses the turn-on threshold, the voltage threshold detector circuit lowers **trigger** (signaling that V_{DD} is sufficiently high) and **reset** is asserted to initialize the relevant circuits. After a delay caused by charging the enable capacitor, **enable** is asserted and the POR circuit turns off, driving **reset** low when **vgate** goes high two inverter delays after **enable**. This state represents the normal operating condition for the chip. A different reset circuit asserts **shutdown** when V_{DD} goes below the switching threshold of an inverter, whose power supply is connected to a capacitor, which is charged when **reset** goes high. This assertion causes **enable** and **reset** to go low and reinitializes the POR circuit for the next AC supply cycle.

The voltage threshold detector is the heart of the POR. The first proposed circuit for this block attempts to achieve a consistent pulse height in the subthreshold region over process, frequency, and temperature variation. A schematic is shown in Figure 5. The threshold voltage of an NMOS transistor (Mvt0) is used as a reference for comparison against V_{DD}, sampled through a PMOS transistor at node **vddsw**. The drain current of an NMOS transistor with source to ground and gate to V_{DD} can be used as an indicator of the magnitude of V_{DD}. In the region where $V_{DD} = V_{GS}$ is less than $V_{t,n}$, subthreshold current is described by Eq. (1) [Rabaey et al. 2003]

$$I_D = I_S e^{\frac{V_{GS}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right)(1 + \lambda V_{DS}), \tag{1}$$

where V_T is the thermal voltage kT/q, V_{DS} is the drain to source bias voltage, λ is the channel length modulation parameter, and n is the subthreshold slope factor. I_S is given by

$$I_S = \mu C_{ox} \frac{W}{L}(n-1)V_T^2 e^{\frac{-V_{t,n}}{nV_T}}. \tag{2}$$

The exponential dependence of I_D on V_{GS} makes it possible to use a single NMOS transistor as a sensitive, subthreshold voltage-to-current converter with the threshold voltage as a reference. In the 0.18 μm process used here, nominal $V_{t,n} = 0.44$ V.

A current mirror formed by Mvt3 and Mvt4 mirrors the current through Mvt0 (which is controlled by V_{DD}) into the diode-connected transistor Mvt1. As this current increases, the voltage drop across Mvt1 increases. When this voltage crosses the inverter switching threshold of Mvt2 and Mvt5, the trigger signal switches from high to low. It is this transition in **trigger** that indicates the power supply is on and the POR circuit should transition to the next state.

Transistor sizing for this circuit is a critical design point. Current should be kept small in order to minimize power dissipation. For this reason, Mvt0 is minimum size and the current mirror (Mvt3, Mvt4) is ratioed 2:1. The output inverter (Mvt2, Mvt5) is skewed high to increase the trigger threshold. The diode-connected transistor Mvt1 is the most critical component in the entire circuit. Extensive simulations that swept width and length were used to find a size that generates a correct reset pulse over all process corners, frequencies from 60 Hz to 1 kHz, and temperatures from 0°C to 85°C. The POR circuit using the constant pulse height threshold detector was simulated using a postlayout netlist with extracted parasitics in Spectre. For a peak V_{DD} of 1.8 V, the turn-on voltage varied between 300 mV and 610 mV with average power consumption between 100 pW and 410 nW, and peak power consumption between 7.5 nW and 4.32 μW. Under the same range of simulation conditions, the circuit proposed in Yasuda et al. [2001] turns on at an average voltage of 1.17 V with average power consumption of 2 μW and peak power consumption of 0.7 mW [Siebert 2005] . The average duty cycle (percentage of the AC supply voltage half-period during which **enable** is asserted) for the proposed POR circuit is 85% versus 70% for the circuit in Yasuda et al. [2001].

The approach described thus far is essentially open-loop and tries to turn on the system at a consistent voltage. Another approach uses replicas of load circuits in the POR voltage threshold detector circuit such that correct operation is guaranteed. An example of this second approach is to replicate the DRAM circuit (Section 3.3) used to remember data across AC supply cycles, and size the transistors such that the trigger signal is only lowered once a logic one can be written reliably to the storage node [Siebert 2005].

3. ENERGY SCALABLE FIR FILTER AND MEMORY DESIGN

Since energy harvesting cannot guarantee a stable and constant power supply, a load circuit, such as the DSP highlighted in Figure 1, needs to be designed using an energy scalable architecture that enables a trade-off between power consumption and output accuracy. This allows the computation requirements to be matched to the available harvested energy. The selected architecture was based on Distributed Arithmetic (DA), which is a bit-serial method of computing the dot product of a constant vector and a variable vector [White 1989]. This approach is particularly useful for implementing energy scalable FIR filters due to its low overhead [Amirtharajah et al. 1999; Zhou 2004].

3.1 Distributed Arithmetic Energy Scalable Filter

To evaluate the circuit techniques proposed in this article, a 16-tap energy scalable FIR filter was implemented using DA. Because DA requires

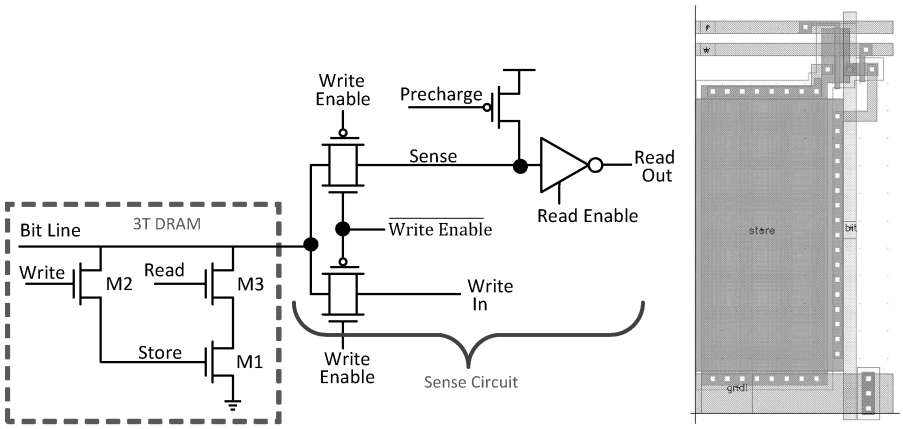
precomputation of all of possible vector combinations, building this filter using a single LUT would require 256 16-bit words to be stored. A memory this size would be unnecessarily large, so four 4-tap filters were built instead and three additional adders accumulate the results. Each 4-tap filter is implemented using a shift register, a 16-entry LUT, an accumulator, and a hardwired left shift. A block diagram of the filter is shown in the bottom half of Figure 2.

Two types of memory are necessary for DA. The data input memory must serially shift data around and through the filter, with bit slices through the data words used to address the LUTs. The data shift memory was built using variable-length shift register chains. As will be discussed in Sections 3.2 and 3.4, DRAM and registers were used to create two different coefficient LUT implementations, thus enabling an experimental comparison between the two approaches.

3.2 Memory Design

The combination of an AC power supply and a small power budget places strict limits on the types of memory that can be used for the LUT. Circuits requiring DC bias current must be eliminated. In addition, memory cells for AC supplies must hold their state while the supply is low without requiring frequent refreshes, which can degrade system performance. A DRAM implementation, which can be integrated into commodity CMOS logic processes, helps decrease system cost and volume. One of the most common difficulties for embedded DRAMs (e-DRAMs) is that cell storage capacitance is often much lower, offering on the order of microsecond retention times [Ishibashi et al. 2006], compared to a dedicated DRAM process that can provide retention times in the millisecond range [Kirihata et al. 2004]. Large retention times are particularly useful for AC supplies, which can potentially go up to a millisecond without an adequate supply voltage. Low voltage e-DRAMs also need to maintain an acceptable Signal-to-Noise Ratio (SNR). Without having access to thicker oxides or a high-k dielectric, one of the best structures to maintain SNR is the 3T gain cell from the early 1970's, which is low-voltage capable, relatively small and simple, and compatible with logic processes [Itoh et al. 2004].

Just such a 3T cell structure, shown in Figure 6(a), was used. The cell includes an NMOS write transistor (M2) and two NMOS devices in series to form the storage capacitance (M1) and read access device (M3) [Siebert et al. 2005]. The bitline and sense node are precharged high and, depending on whether the gate of M1 is high or low, the bitline and sense node are either discharged or left floating. The sense amplifier is a simple CMOS inverter with a tristate enable, which eliminates the static power dissipation of an analog sense amplifier. Memory read and write operations are single ended, as opposed to differential, since the DRAM is designed for LUT implementation and the amount of memory is small, so bitline voltage swings can be relatively large. Device M1 must be sized large enough to maintain state, despite leakage, while the supply voltage is below the turn-on threshold. The gate of M1 and the source of M2 comprise the storage node capacitance.



(a) 3T DRAM cell and sense circuit (b) cell layout

Fig. 6. 3T DRAM cell and sense circuit schematic and cell layout.

3.3 DRAM LUT Cell Design

For vibration-based energy harvesting the AC supply frequency range of interest is between 60 Hz to 1 kHz. The electronics function when V_{DD} is between approximately 400 mV and 1.8 V. At 60 Hz the power supply would be below the functional supply voltage for up to 1.2 ms. This represents the amount of time between a 400 mV falling and rising edge. The retention time required for a supply frequency of 1 kHz is 72 μs. For lower AC supply frequencies, or an interruption in mechanical vibration, data stored in the memories would be lost. Depending on the system requirement, a battery or nonvolatile memories could provide a backup, but this is beyond the scope of this work.

To determine the gate area of M1 needed, simulations were performed on the DRAM cell, setting the storage transistor width and length equal and sweeping them from 450 nm to 19.35 μm. For each storage transistor size, a logic 1 at 400 mV was written for 2.7 μs and the time for the maximum voltage on the storage node to fall 20% was measured. These conditions emulate a write operation just before the supply voltage drops below a usable value, while the write time fits within the ring oscillator period at 400 mV. Temperature was swept from 0°C to 85°C in 5°C increments as well. The simulation results are shown in Figure 7. A line indicating the 1.2 ms worst-case hold time for the storage node to maintain its value is also shown. Simulation indicates that over 147 μm^2 of gate area is required to meet the specification up to 85°C. This is quite large, and is neither practical nor acceptable. To reduce this size, the temperature range was restricted to between 0°C and 50°C, which is reasonable for wireless sensor node applications. In addition, higher temperatures are accommodated by higher power supply frequencies, such as a hold time of 240 μs at 300 Hz, while lower temperatures would allow for lower supply frequencies. With temperature limited to below 50°C (shown with the vertical line in Figure 7), an area of 46 μm^2 satisfies the hold requirement with an

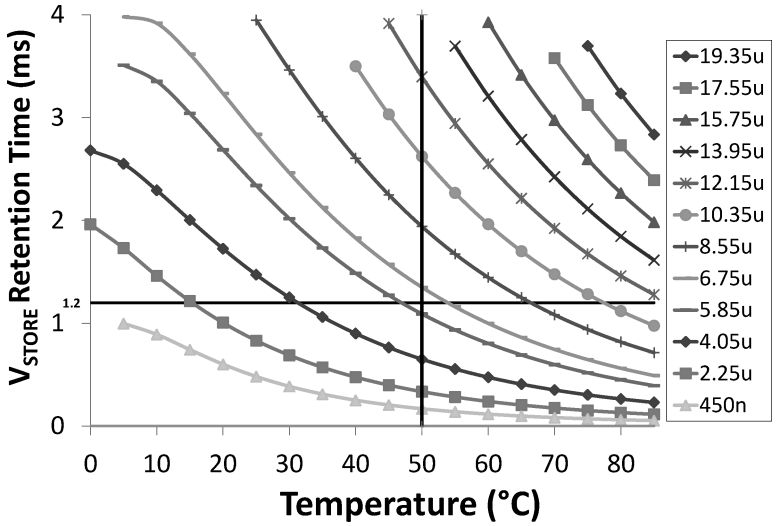


Fig. 7. Simulated 100%–80% fall times for various DRAM cell storage node sizes over temperature. The horizontal line indicates the 1.2 ms requirement and the vertical line shows the 50°C range the design was restricted to.

equivalent node capacitance of approximately 300 fF. This also accounts for a source diffusion capacitance to ground added by the write transistor, M2, which is minimum-sized to minimize leakage and maximize write voltage. In the 180 nm DRAM implementation, M1 has a $W/L = 4.59\ \mu$m/9.9 μm. The length was chosen to be longer than the width to prevent the transistor from turning on due to charge coupling from the read transistor, M3, onto the storage node when a logic zero is held. The longer length increases the time to discharge the bitline when the cell is holding a logic one. A value of 9.9 μm was chosen to simplify the layout by pitch-matching to the address decoder. The measured DRAM retention time will be discussed in Section 4. Two 16×16 memory arrays on the test chip use this DRAM cell with the schematic and layout shown in Figure 6.

3.4 Flip-Flop LUT Cell

Half of the LUTs in the DA filter use the 3T DRAM cell while the other half utilizes a more standard flip-flop-based approach. These register LUTs ensure that the test chip still functions in some capacity if the DRAM LUTs fail to work properly, for example, if the power supply frequency or operating temperature exceeds the designed DRAM retention time window. Including registers also allows the Data Retention Voltage (DRV) to be measured in a way similar to SRAM DRV [Qin et al. 2005]. Depending on the DRV, it is possible to use the register memory in conjunction with an external supply bypass capacitance so that the chip can operate using a supply voltage with very large ripple that approaches, but does not cross, the flip-flop DRV.

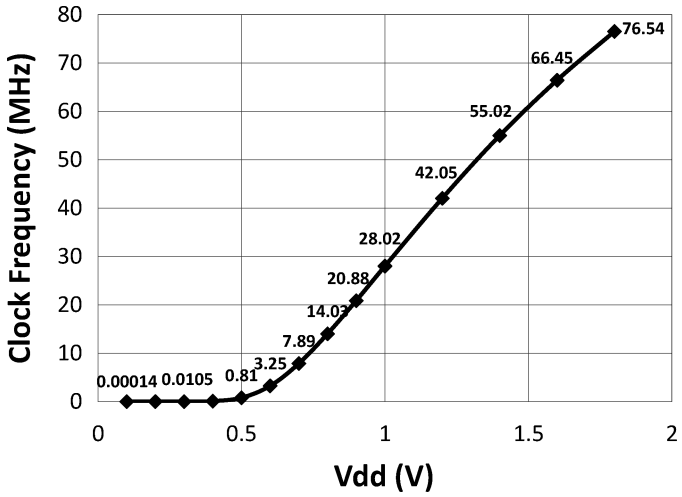


Fig. 8. Measured self-timed clock frequency vs. supply voltage.

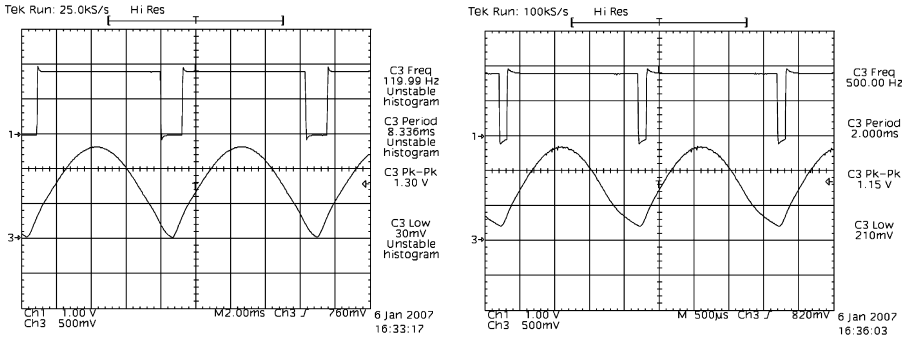
4. MEASURED RESULTS

The test fixture for evaluating the test chip, with the functionality illustrated in Figure 2, employed a custom printed-circuit board along with an adapter to fit the socket for the chip's 68-pin leaded chip carrier package. The chip is programmed and fed input data by a Digilent Pegasus FPGA board [Digilent 2004] that runs a synthesizable version of the same test bench used for pre-silicon verification. On-chip First-In, First-Out (FIFO) memories are used to capture the input bitstream for the DA filter and the LUT contents. These structures and the I/O pads use a separate DC supply voltage, V_{CC}, to allow the power of the circuits under test to be measured independently.

4.1 Self-Timing

Figure 3 shows the frequency variation of the ring oscillator on the fabricated chip [Wenck et al. 2007] as the AC supply voltage varies. On the bottom oscilloscope trace is the AC input, which is a rectified sine wave provided by an arbitrary waveform generator with a frequency of 200 kHz and a peak to peak voltage of 1.4 V. The top scope trace is the output of the ring oscillator buffered through a separate supply to reduce loading. As the magnitude of the AC signal increases the frequency of the ring oscillator also increases.

The frequency of the self-timed clock versus supply voltage is plotted in Figure 8. To quantify the design margin built into the self-timed internal clock period, an external clock source was used to clock the FIR filter, bypassing the internal ring oscillator. The external clock frequency was increased until logical failures were observed. At the nominal 1.8 V DC supply, the filter functioned up to 261 MHz compared to the self-timed clock frequency of 76.54 MHz at the same voltage. The self-timed clock is running at less than 30% of the maximum clock frequency. Although significant performance has been lost, the self-timed



(a) 60 Hz AC input [Wenck et al. 2007] (b) 250 Hz AC input

Fig. 9. Measured rectified waveform and POR output for 60 Hz AC input (a), and 250 Hz AC input (b).

clock has improved robustness because it has sufficient margin to operate over a very wide range of process, temperature, and voltage.

4.1.1 *Minimum Functional Supply Voltage.* To minimize power consumption from a DC supply, and to provide the most clock cycles of operation when using an AC supply, the lowest supply voltage that allows the FIR filter to operate correctly should be known. An external clock is used to decouple the minimum operating voltage results from the self-timed internal clock. The flip-flop-based memories and DRAM-based memories were tested separately by operating the FIR filter in the appropriate 4-tap mode.

The flip-flop-based 4-tap FIR filter operated at 719 mV using an external clock of 5 kHz, while the DRAM based 4-tap FIR filter functioned at 807 mV using an external clock of 100 kHz. The flip-flop-based filter achieves a lower operating voltage because it benefits from the ability to operate at an arbitrarily low clock frequency, while the DRAM-based filter has a minimum functional clock frequency based on the DRAM cell's retention time. The minimum voltage for the DRAM filter should be higher because of the NMOS threshold voltage drop affecting the cell write voltage. Both results are higher than the expected minimum for a 180 nm process given by presilicon simulations. Nanosim-VCS simulations of the test chip show that there is a dramatic change in skew between the clocks in the V_{CC} domain of the on-chip stimulus circuits and V_{DD} domain of the circuits under test. This causes the shift register operating on the V_{CC} supply to shift early, resulting in the V_{DD} voltage domain receiving data one clock cycle too early, causing a failure. This timing inconsistency results in the unexpectedly high minimum supply voltage, which is not limited by the memory cell performance for this test chip as originally intended.

4.2 Power-On Reset

Figure 9 shows the power-on reset circuit's **enable** signal on the top and the output of the on-chip rectifier on the bottom [Wenck et al. 2007]. The rectifier

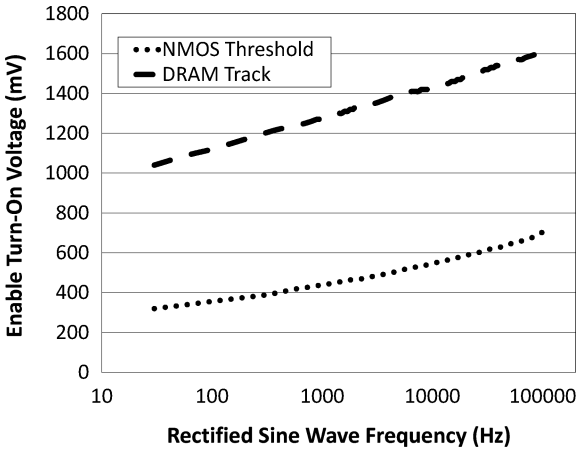
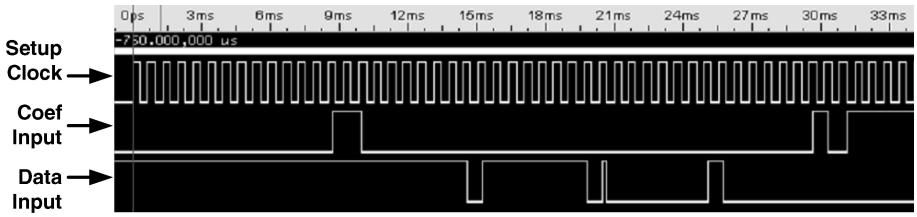


Fig. 10. Measured enable turn-on voltage vs. rectified sine wave frequency for both NMOS threshold $V_{t,n}$-based and DRAM replica-based POR circuits.

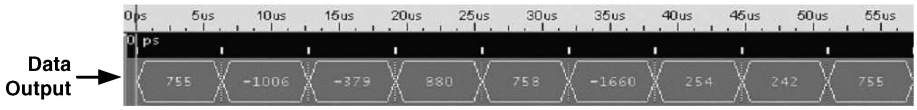
output is the AC input to the POR circuit. The **enable** signal is low until the AC voltage reaches the turn-on threshold and then it goes high and stays high until the AC voltage is too low to sustain correct logic and memory operation. Parasitic capacitance filters the 250 Hz AC input, shown in Figure 9(b), enough to raise the minimum voltage, thus increasing the percentage of the AC supply cycle time that **enable** is high.

The delay of the POR was tested by applying a step voltage to the input supply, V_{DD}, and then measuring the time between the 50% points of both the supply and **enable** signal rising edges. The POR circuit using the NMOS $V_{t,n}$-based voltage threshold detector (Figure 4) has an average delay of 140 ns. The POR circuit based on the DRAM replica voltage threshold detector has a much longer average delay of 67μs, which is expected since the inherent threshold voltage drop across the write transistor decreases the written voltage, which increases the required turn on voltage, and the large capacitance of the DRAM cell takes more time to charge.

The consistency of the turn-on voltage was tested by applying a rectified sine wave from an arbitrary waveform generator to the V_{DD} supply and sweeping the frequency. The measurements, shown in Figure 10, agree with simulation results in that the NMOS $V_{t,n}$-based turn-on voltage varies between 340 mV and 436 mV for frequencies between 60 Hz and 1 kHz at room temperature (0.10 mV/Hz sensitivity), while the DRAM replica circuit varies between 1090 mV and 1270 mV over the same frequency span (0.19 mV/Hz sensitivity). The uncertainty of the turn-on voltage detector was measured by using a digital oscilloscope to sample V_{DD} when triggered on the **enable** signal. The average turn-on voltage using 32 samples was recorded along with the magnitude of the voltage range for which the **enable** signal turned on. The NMOS $V_{t,n}$-based turn-on voltage had an uncertainty of $\pm$7.7% at 60 Hz and $\pm$8.7% at 1 kHz while the DRAM replica turn-on voltage had an uncertainty of $\pm$3.3% and $\pm$5.79% at 60 Hz and 1 kHz, respectively.



(a) serial input data



(b) parallel output data

Fig. 11. Logic analyzer screen outputs for a setup clock, serial input filter coefficients, and 8-bit 2-tone serial input data in (a), and low-pass filtered 16-bit parallel output data in (b).

4.3 FIR Filter Energy Scalability

Matlab was used to create both input data and filter coefficients to validate the energy scalable FIR filter performance using two-tone tests. Filter coefficients were modified manually to reduce the possibility of accumulator overflow. A logic analyzer screen output in Figure 11(b) shows the result of an 8-bit 2-tone input (fed in serially in Figure 11(a)) being processed by the DSP configured as an 8-tap low-pass FIR filter. The results are 16-bit output data because all additions are done with 16-bit precision internally.

To determine the leakage power, the filter was configured as a 16-tap low-pass filter with a 16-bit white noise input applied for several cycles to initialize the LUTs and internal circuit nodes. The clock was then stopped and current was measured for various supply voltages. Leakage power varied from 30 nW at 0.4 V to 265 nW at 1.8 V. The energy per output sample is computed by taking the ratio of average power to the output data rate. The scaling of energy per output sample with input sample word length (resolution) can be seen in Figure 12. The energy scales linearly with word length, which results in linear power scaling for a fixed output sample rate. This confirms that the FIR filter design is indeed energy scalable and not dominated by fixed power consumption such as leakage or static power.

4.4 DRAM Retention Time

To test the DRAM retention time, the FIR filter was allowed to run through one full memory cycle of accesses and refresh using an external clock provided by an FPGA. The clock was paused and then the cycle repeated. The time delay between each cycle was gradually increased until a bit error was seen at the filter output. The memory refresh takes up a nonnegligible amount of time and must be included in the DRAM retention time measurements. The DRAM retention time was tested at a clock frequency of 195 kHz, which allowed sufficient time for the DRAM to be written as well as for the bitline to be evaluated during a read. The results can be seen in Figure 13. It should be

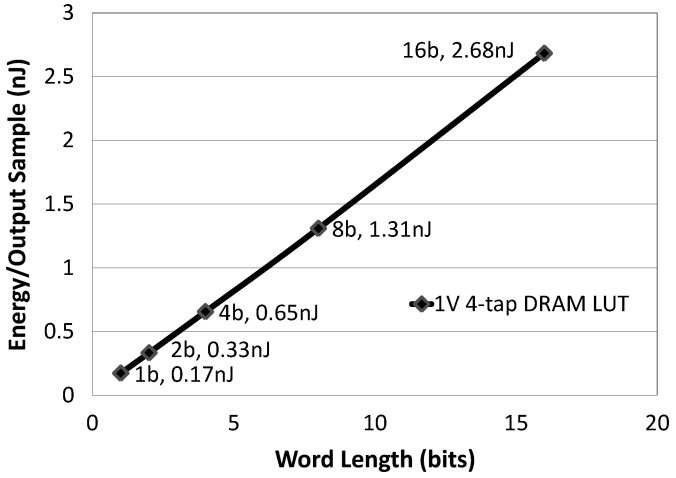


Fig. 12. Measured energy per output sample versus wordlength with a DRAM-based LUT 4-tap filter at 1 V.

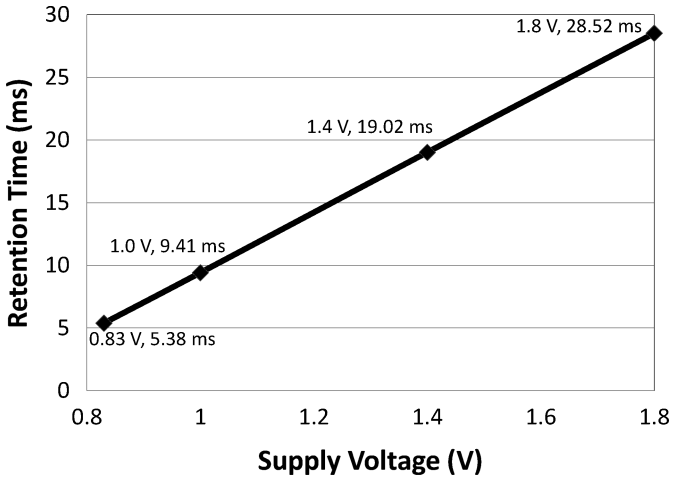
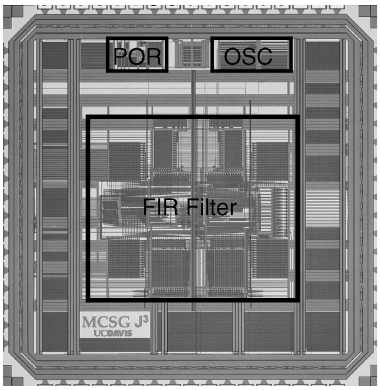


Fig. 13. Measured DRAM retention time versus supply voltage.

noted that the simulated 100%–80% fall times for the DRAM cell storage node shown in Figure 7 are conservative in that discharging the storage node further can still result in correct data recovery, provided sufficient time to evaluate the bitline within the clock period. The measured retention times of 28 ms at 1.8 V and 9.4 ms at 1 V would translate to AC supply frequencies of under 2.55 Hz and 7.59 Hz, respectively. Figure 13 indicates that DRAM retention time is a linear function of supply voltage above 800 mV, implying that leakage current is roughly constant. Further work can examine this trend at lower supply voltages, where devices operate further in the subthreshold region.



Technology	180 nm CMOS
Dimensions	2.6 mm x 2.6 mm
Transistors	135K
I/O V_{DD}	1.8 V
AC Supply (V_{PP} = 1.8 V)	60 Hz – 1 kHz
Core Freq. (max)	75.6 MHz
Power (Core)	127 – 113 μW

Fig. 14. Die photo and chip summary.

4.5 Flip-Flop Data Retention Voltage

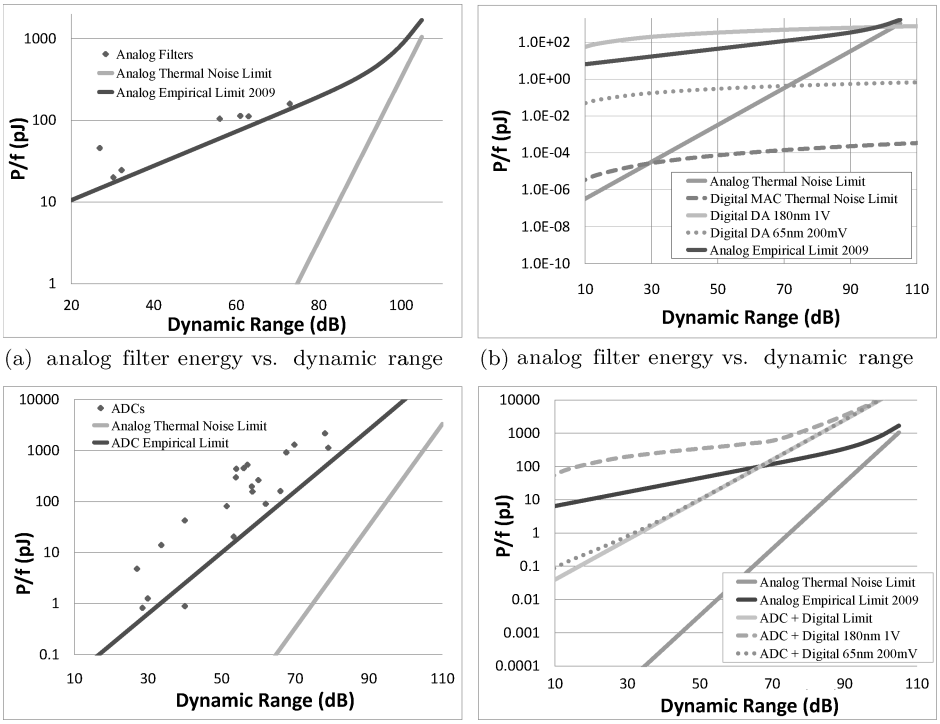
The flip-flop DRV was measured in a manner similar to SRAM DRV testing [Qin et al. 2005] by loading the flip-flop LUTs with known data and then accessing the data stored using a specific input bit pattern that reads the table entries without any shifting or addition. The filter was clocked with a gated external clock. When the clock was stopped, the supply voltage was lowered and then returned to 1.8 V. The clock was then resumed and the output was checked for any bit failures. This process was then repeated for gradually lower voltages until the first failure was detected. The average measured flip-flop retention voltage was 153 mV.

4.6 Die Photo and Summary

Figure 14 shows the die photo and a summary of the test chip, which includes both analog and digital subsystems and on-chip test structures such as FIFO memories, which load the FIR filter coefficients and a serial input data stream. There are about 135,000 transistors implemented in 180 nm CMOS. With an I/O supply of 1.8 V, and 1.8 V_{p-p} AC supply ranging from 60 Hz to 1 kHz, the maximum core frequency from the on-chip ring oscillator is 75.6 MHz and core power dissipation varies from 127 μW to 113 μW. The power numbers are obtained by operating the FIR filter with 16 bits of precision, and include the POR circuit and the ring oscillator. More power is consumed at lower supply frequency since the system is active for a higher percentage of the AC supply cycle. The self-timed datapath and POR circuit operate correctly using a DC supply, which enables a dual-supply system where energy can be harvested from multiple sources such as vibration (AC) or solar (DC) [Wenck et al. 2007].

5. SCALING MECHANICAL VIBRATION ENERGY HARVESTING SYSTEMS

Fifteen years ago, Vittoz presented a remarkably prescient paper on low-power design [Vittoz 1994] in which he outlined many techniques to decrease system power consumption and certain limits to low-power design for both digital and analog circuits based on theoretical considerations. Energy harvesting systems



(a) analog filter energy vs. dynamic range (b) analog filter energy vs. dynamic range

(c) ADC energy vs. dynamic range (d) analog and digital filter comparison

Fig. 15. Filter and ADC energy versus dynamic range. Power is normalized by twice the signal bandwidth and the number of taps.

offer an interesting context to explore the implications of these theoretical limits. For example, the limits determine the minimum volume requirements for a system that powers itself, since both vibration energy harvesting and solar energy harvesting scale poorly as volume shrinks [Mitcheson et al. 2004]. An energy harvesting system can have potentially unlimited operating lifetime while occupying a finite volume, so it presents an interesting limit study on how small an electronic system can be made. Wireless sensor nodes typically require low performance from each of their components (sensing and actuation, analog and digital processing, and RF communication) and therefore can be made very low power with aggressive application of well-known techniques such as voltage scaling and power/clock gating.

5.1 Comparison of Analog and Digital Filtering

With the world's information becoming increasingly collected and processed digitally it might seem pointless to consider analog processing of sensor data, but for an energy harvesting wireless sensor system, where every femtojoule of energy counts, it is worthwhile to revisit partitioning the system between the analog and digital domains. Vittoz looked into the possibility of analog filtering still being viable compared to digital filtering almost 20 years ago

[Vittoz 1990]. We will review the trade-offs between analog and digital filtering using theoretical limits and data from the literature to provide a guide for selecting a filter implementation in the energy harvesting context.

At a minimum, an analog antialiasing filter is required before any analog-to-digital conversion of a sensor output signal. A major argument against further analog filtering is that modulation schemes for modern wireless communications are digital [Otis and Rabaey 2007], which would require analog-to-digital conversion at some point in the signal chain, thus making the ADC power consumption fall out of the total system power equation in any comparison. If the conversion will be done anyway, why not do it at the front-end and use only digital signal processing? This argument breaks down for energy harvesting wireless sensor systems where the wireless communication can be aggressively duty-cycled to fit within an arbitrarily low power constraint. For example, if an analog low pass filter provides a moving average, which can be communicated only when needed, then the ADC on the back-end of an analog filter would be duty-cycled as well. This would allow ADC power to be neglected. For applications such as temperature or gas concentration monitoring, a low-power analog threshold detector could be used to turn on the radio only when an event occurs. If the wireless communication is done using an external interrogating RF field, then ADC power consumption can also be ignored because it too can be powered from the incident field. The power that needs to be controlled is that of the always-on components that are constantly sensing and filtering to ensure that results are available when needed.

5.1.1 *Analog Filtering.* In Vittoz [1990] the energy (defined as power, P, divided by the cutoff frequency, f) versus dynamic range for implementing one analog pole was found to be

$$\frac{P}{f} = 8kT\left(\frac{V_s}{V_n}\right)^2, \tag{3}$$

where an ideal amplifier is assumed and the system is limited solely by kT/C thermal noise. If we compare this to what is reported in the literature for discrete-time FIR filters as seen in Figure 15(a), most practical filters are far from this limit, especially for smaller dynamic ranges.[1] The y-axis is the total system power divided by the sampling frequency and number of filter taps. To track more closely with what has been reported, the following empirical formula for total energy is proposed:

$$\frac{P}{f} = 8kT \times 10^{(\frac{DR}{10})} + E_{OH} \times 10^{EF\times(\frac{DR}{10})}, \tag{4}$$

where P/f is the energy per sample, k is Boltzman's constant, T is absolute temperature, and DR is dynamic range. E_{OH} is the energy associated with any overhead, such as clocking, analog biasing, amplifier inefficiency, and compensation for added noise from differential nonlinearities, harmonic distortion, or

[1]Some of the values used were actually reported as Signal-to-Noise Ratio (SNR) or Signal-to-Noise and Distortion Ratio (SNDR), not Dynamic Range (DR).

mismatch. *EF* is the Efficiency Factor relating how well the overhead energy and additional energy are converted to increased Dynamic Range compared to the theoretical limit in Eq. (3). Eq. (4) contains the thermal noise limit, Eq. (3), to ensure it is never met at higher dynamic ranges. E_{OH} and *EF* of 4 pJ and 0.21, respectively, were found to fit data from the literature. These values are empirical and will likely change as technology scales and architectures and circuits improve.

5.1.2 *Digital Filtering.* The energy to implement a digital filter is largely a function of device scaling. Three different filters are compared in Figure 15(b): A 0.18 μm Distributed Arithmetic (DA) FIR filter at 1 V, that same filter scaled to 65 nm and 200 mV, and a MAC FIR filter based on the digital limit of $8kT$ per switching event, described in Vittoz [1994]. The DA filters require an energy per bit per tap of 42 pJ and 37.8 fJ, respectively. For the digital limit case each switching event requires $8kT$ or 0.03 aJ and we assume $40n + 30n^2$ transitions per result for n bits of precision. Figure 15(b) shows that the 0.18 μm filter consumes less power than the analog filter for high precisions, while the more modern 65 nm process operated at subthreshold voltages and the theoretical limit for digital filters are always better than current practical analog filters. The comparison is not quite complete, because we have not yet taken into account the cost of converting our signal to digital.

5.1.3 *Analog-to-Digital Conversion.* ADC's have been shown to be subject to similar theoretical limits as Eq. (3), but in practice require more energy per sample than the thermal noise limit. The trend in ADC design indicates that the energy required for each bit only doubles instead of quadrupling as the thermal noise limit would suggest [Moteiv 2008]. An empirical formula for ADC energy per sample versus dynamic range is the same as Eq. (4), but the data is fit using an E_{OH} and *EF* of 0.01 pJ and 0.6. These values could change with additional data points and will likely improve with further scaling and innovation in circuits and architecture; these improvements move the empirical line closer to the thermal noise limit or some other physical limit (such as device mismatch). Data from ADC's reported in ISSCC 2007 through 2009 are plotted along with the thermal noise limit and the empirical ADC limit in Figure 15(c).

5.1.4 *Analog and Digital Filtering Comparison.* Figure 15(d) compares digital to analog filtering by adding ADC energy to the digital filtering energy, for the 180 nm, 65 nm, and $8kT$ digital limit cases. Both the analog thermal noise and analog empirical limits are shown. It is important to note that everything has been normalized to a single filter tap, but as the number of taps increases, the cost of conversion would be amortized over the additional filtering capability. The graph indicates that the analog limit of energy efficiency remains a distant goal and that ADC performance ultimately limits energy efficiency for digital filters using a modern process and subthreshold operation.

5.2 Limits of System Scaling

The preceding analysis of theoretical limits and empirical trends of circuit power consumption enables a designer to compute lower bounds on system miniaturization by including energy and power density limits. An optimistic energy density for batteries is 2 nJ/μm^3. For comparison, MEMS-based vibration energy scavenging can generate power densities from 0.4–80 nW/mm^3 depending on the vibration frequency and amplitude [Mitcheson et al. 2004]. Suppose a sensor must include a single-pole analog antialiasing filter with 10 kHz bandwidth, a 16-bit ADC sampling at 20 kHz, and a 4-tap digital filter operating on 16-bit data at 1 MHz. Assuming the empirical models for the analog filter and ADC and a 65 nm 200 mV digital filter implementation, the total power consumption for this signal processing chain is 4.68 μW (1.64 μW for the analog filter, 620 nW for the ADC, and 2.42 μW for the digital filter). Using vibration energy harvesting, assuming the maximum power density, and 98.3% rectifier efficiency [Guilar et al. 2009] with an AC supply-tolerant self-timed DSP, the system would require a volume of 59.5 mm^3. If AC/DC conversion was required, the system would need 70.9–91.6 mm^3, a volume increase of 19–54%. The thermal noise limit of an ideal analog filter with 10 kHz bandwidth and SNR equivalent to 16-bit dynamic range is 22 pW. Using the $8kT$ digital switching energy limit, assuming 8320 switching events to compute the same 16-bit results at 1 MHz, yields a minimum power consumption of 276 pW. If the ADC contributes roughly the same power as the analog filter, the required volume would be 4.74×10^6 μm^3 (about 168 μm on a side) to harvest 381 pW, including the nonideal AC/DC switching efficiency. A battery-operated system at this power consumption and volume would run for 288 days. For comparison, a human red blood cell has a surface area of 150 μm^2 and a volume of 115 μm^3, while a grain of table salt is approximately 100 μm on a side. Clearly, it is necessary to approach the theoretical limits of circuit power consumption to miniaturize systems with greater than 1 year operating lifetime below 1 mm^3.

6. CONCLUSIONS

Appropriate load circuit design for energy harvesting can extend system lifetime, increase integration, and decrease system cost and volume. Exploiting the AC nature of mechanical vibration energy harvesting can increase efficiency and decrease cost further by using the following techniques: self-timed circuits, which guarantee timing despite wide voltage variations; fast POR circuits to initialize DSP pipelines for correct operation; and dynamic memories to maintain state across supply cycles. These techniques were demonstrated and verified on a test chip in a 0.18 μm digital CMOS process. Architectural choices, such as the use of DA, which allow the scaling of energy consumption by varying the clock, filter type, and data word-length have also been demonstrated and verified. The proposed POR circuit can also operate correctly under a DC supply voltage. In this situation, the POR circuit will produce a reset pulse during the supply voltage rise time. The self-timed ring oscillator simply matches the clock frequency to the constant supply voltage and the chip operates as a traditional DC supply system. This provides the potential for a dual-supply

system where energy can be harvested from multiple ambient energy sources. These circuits can also be generalized to interface with inductively powered devices, a growing area with applications such as biomedical implants, embedded sensors, and RFID tags [Briole et al. 2004]. The proposed power-on reset circuit was designed for low-frequency AC power supplies, but could be adapted for these higher-frequency applications. The current design operates correctly up to a supply frequency of 100 kHz. Analog circuits must also be included to realize a fully functional sensor system and would require a high power supply rejection ratio and a bias that stabilizes quickly, possibly by exploiting a digital preset stored in dynamic memory on initialization. If these needs were met, these circuits should be able to work properly over short time periods in the supply cycle. Theoretical considerations and empirical observations show that it is possible to scale vibration-based energy harvesting systems to below 1 mm^3 if analog and digital circuits can be designed to approach the thermal noise limit. This combination of minimal volume and unlimited lifetime will enable new devices for heart regulation, biofeedback, and others in the emerging field of Body Area Sensor Networks (BASNs) [Hanson et al. 2009].

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