27.9 Ultra-Low-Voltage Circuits for Sensor Applications Powered by Free-Space Optics

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Advances in photonics have typically been exploited in high performance systems, e.g. high-frequency, low-jitter clocks injected optically [1]. As solid-state lighting and free-space optical (FSO) communication expand, low-performance sensor systems can also benefit from photonics. Sensors can receive power, clock, and data from optical sources at different wavelengths with crosstalk eliminated through narrowband filtering by photonic devices (e.g., ring resonators [2]). Applications include indoor environmental sensing or biomedical devices implanted under the skin (transcutaneous optical power). However, significant challenges to realizing such systems exist. FSO power decreases quadratically (beam divergence) and exponentially (absorption) with distance, thus optically-powered sensors must be extremely low power to maximize operating range. Mixed-signal circuits must support energy-scalable operation with low area overhead (to maximize energy harvesting photodiode area) under variable low voltage (V_{DD} can vary significantly with light intensity near the maximum power point). They must process analog inputs near full-scale to maximize SNR. Energy harvesting photodiodes optimized for conventional CMOS have been developed [3]. In this paper, we describe optically-powered CDR and delta sigma modulator (DSM) circuits. Figure 27.9.1 shows a possible system context. Photodiodes supply power (from ambient light or interrogating beam) and capture optical data, e.g. timing configuration for the DSM clocks. The DSM output bitstream modulates a simple on-off keyed (OOK) transmitter or is saved to non-volatile memory (not shown).

The CDR circuit is composed of a charge pump phase-locked loop (PLL), two interleaved replica VCOs and digital logic [4,5]. The VCOs are built from 161-stage ring oscillators with internal RC loading provided by NMOS switches and capacitors. RC loading ensures balanced rise and fall times and a minimum oscillating frequency across a wide range of supply voltages. Figure 27.9.2 shows a block diagram of the circuit, a schematic of VCO_R and an example of a delay stage inside the oscillator. The data rate is carefully chosen near the minimum frequency attainable by VCO_R, and the data is 3b4b encoded to maximize transitions. VCO_R output signal R is compared to the REF signal by the Phase Frequency Detector (PFD). After a sufficient number of transitions, the PLL will have adjusted the frequency produced by VCO_R such that it approximately equals the data rate. The frequency output by VCO_T and VCO_C should also match the data rate since all VCOs are identical and have the same control voltage, V_{tune}. The data D_{IN} interleaves VCO_T and VCO_C producing the pulses T and C. These are XOR'ed to produce the recovered clock CLK, which samples D_{IN} on the falling edge. The retimed data D_{OUT} now has the rising edge of the recovered clock aligned in the center of the data. Mismatch in the VCO frequencies at fixed V_{tune} will produce a frequency deviation from the data rate. This poses a large problem in typical CDR circuits because these errors accumulate, causing the sampling edge to drift from the center of the data eye and only a certain number of bits will be sampled correctly before setup and hold times are violated. Interleaving VCO_C and VCO_T removes the accumulation of errors caused by oscillator mismatch and resulting frequency deviations from the data rate. This circuit can tune the PLL using the data or an external clock provided by the optical photodiodes. If an optical clock signal is applied at the reference input REF, the circuit can lock over a wide range of data rates (45kbps-200kbps) under an illuminance of 4.6 klx at the expense of extra photodiode area.

The DSM circuit meets the aforementioned design criteria by simplifying a passive architecture targeting high resolution and minimal power for wireless applications [6]. Energy scalability was achieved by using components which can scale power consumption by adjusting both sampling frequency and supply voltage over a wide range and eliminating static current. The DSM consists of two switched capacitor low pass filters which sample a differential input signal; the filtered signals are evaluated by a comparator to create a pulse width modulated digital output. The noise transfer function (NTF) produced by the low pass filter $H(z) = [(C_0/C_S + 1) - (C_0/C_S)z^{-1}]^{-1}$ approaches that of an ideal integrator ($H(z)=[z-1]^{-1}$) by increasing the C_0/C_S ratio. The passive LPF realization provides an attenuation which effectively increases the comparator's input-referred noise at the modulator inputs. This ultimately limits the resolution, trading resolution for reduced power consumption. The LPF was implemented with a bottom plate sampling switched capacitor circuit. Each LPF channel uses two capacitors, C_S=60fF and C_0=1.8pF and analysis of the NTF shows that a C_0/C_S ratio of 30:1 provides the best tradeoff between attenuation of quantization noise and minimization of capacitor sizes. The switching is done with minimum-sized full transmission gates and four external clocks buffered on-chip. The DSM requires two non-overlapping clocks ϕ_1 and ϕ_2, a delayed version of ϕ_1 represented by $\phi'_1$and a non-overlapping reset ϕ_3. During ϕ_1, C_S is reset high or low depending on the comparator output to implement the 1b DAC in the feedback loop, and the previous output is held on C_0. During ϕ_2, the modulator input is attenuated and averaged with the previous input on C_0. The comparator evaluates its inputs on ϕ_1, the result is latched on ϕ'_1 and the latch inputs are reset on ϕ_3. The comparator is a dynamic circuit without preamplification and is made from a cross-coupled inverter pair latch, gating transistors which eliminate static current and two slave latches. The cross-coupled latch and the capacitors were laid out in common centroid style to minimize the effects of mismatch. The latch transistors were oversized to minimize offset effects caused by mismatch in the transistor lengths. Clock ϕ_3 allows the cross-coupled latch to be folded into the master stage of two edged-triggered flip-flops which produce the DAC inputs, minimizing transistor count. The circuit uses 86 transistors in total including clock buffers. A circuit schematic for the modulator can be seen in Fig. 27.9.3 along with a timing diagram, a schematic for the comparator and one of the slave latches.

All the circuits tested used photodiodes to provide the power required for operation. The input data for the CDR was also provided optically. The photodiodes were illuminated with off-the-shelf 10mm white LEDs, and the transmit distance for the testing was one inch. The LED intensity can be varied under software control through a current DAC and a microcontroller. Figure 27.9.4 shows a plot demonstrating the CDR performance, an eye diagram of the recovered clock and data after 1.1 million data transitions. The data rate is 50kbps and the circuit operates at 300mV. The DSM performance is plotted in Figure 27.9.5 versus light intensity and input voltage range with a full scale voltage of 400mV, outputting samples at 256kHz with an input tone at 177Hz and a Nyquist rate of 4kHz (OSR=64). Figure 27.9.6 summarizes the measured results for both circuits. Power was measured by testing the circuits with an external voltage source. All chips were manufactured in a 1P9M 90nm digital CMOS process. Die photos are shown in Figure 27.9.7.

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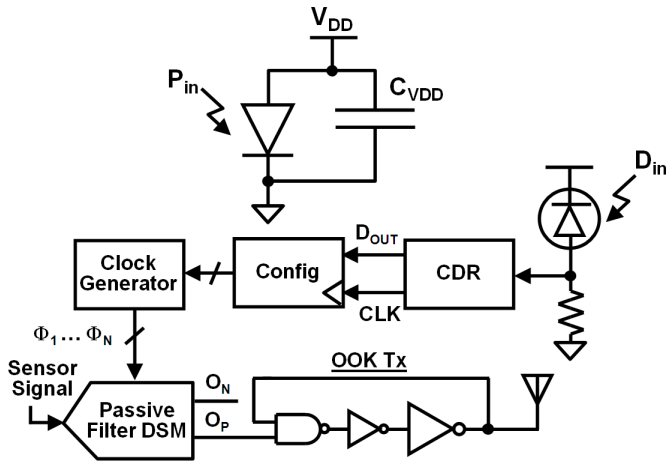

Figure 27.9.1: Simplified block diagram of the proposed sensor system.

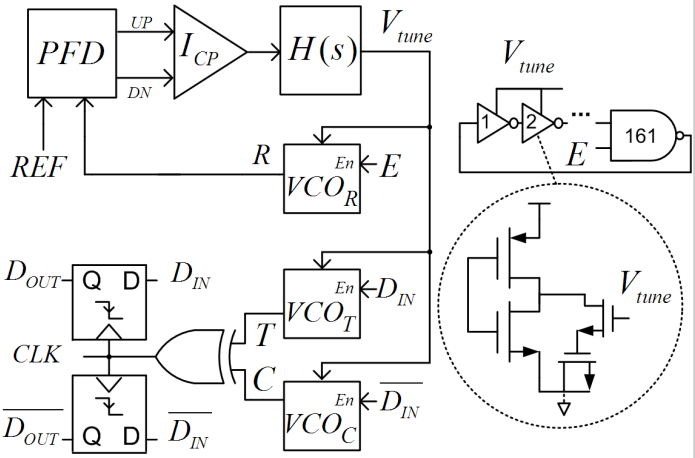

Figure 27.9.2: Clock data recovery circuit schematic.

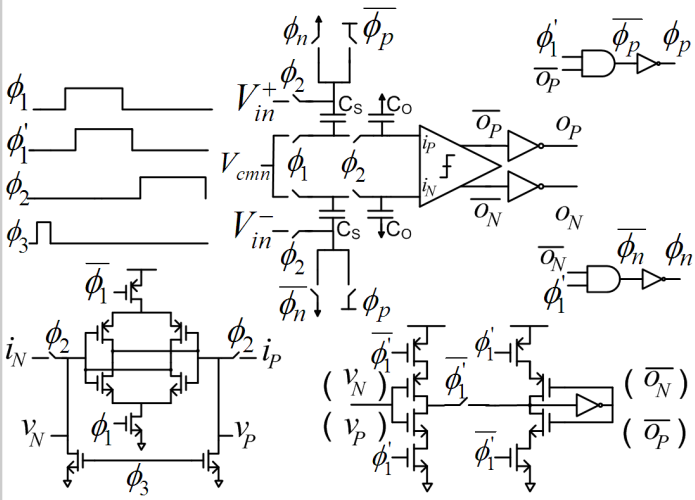

Figure 27.9.3: Circuit diagram for the passive filter-based first order delta sigma modulator.

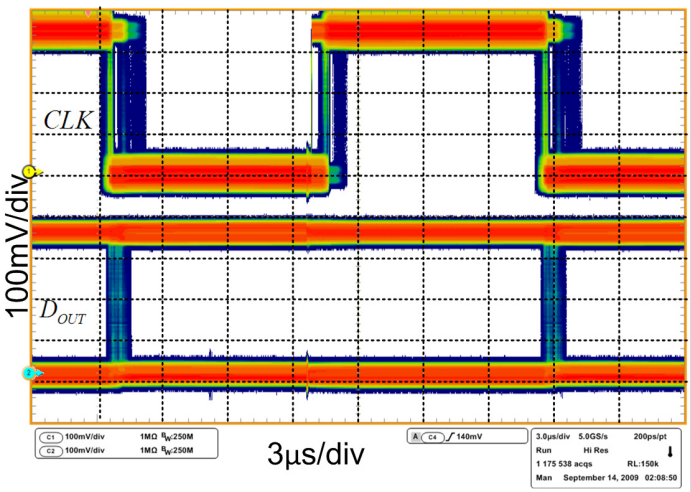

Figure 27.9.4: Measured recovered clock and data eye diagram.

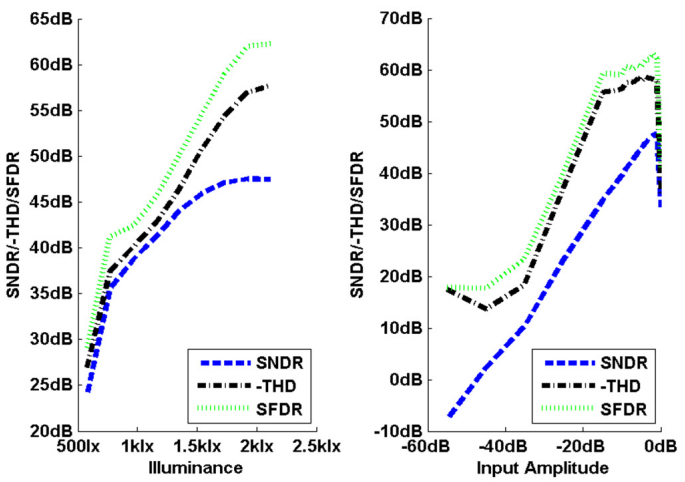

Figure 27.9.5: Measured DSM performance vs illuminance (lx) and input amplitude (dBFS).

Delta Sigma Modulator			Clock Data Recovery Circuit		
Power Source	Electrical	Optical	Power Source	Electrical	Optical
Power	102nW	-	Power	217nW	-
Sample Rate	1.6MHz	256kHz	Data Rate	200kbps	50kbps
SNDR	41 dB	47 dB	Acquisition time	54us	175us
fs (Nyquist)	32kHz	4kHz	Vdd	300mV	
FOM [7]	23fJ/Cs	-	Area	0.0349mm^2	
Vdd	400mV		Illuminance	4.6klx	
Area	0.0814mm^2				
Illuminance	500lx– 2.3klx				

Figure 27.9.6: Summary of measured results for both circuits.

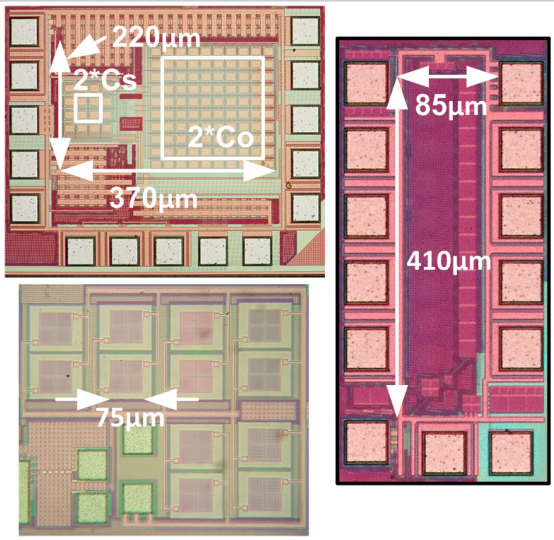

Figure 27.9.7: Die photographs showing the DSM (upper left), energy harvesting photodiodes (lower left), and CDR (right).

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