Integrated Solar Energy Harvesting and Storage

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***Abstract*—To explore integrated solar energy harvesting as a power source for low power systems, an array of energy scavenging photodiodes based on a passive-pixel architecture for CMOS imagers has been fabricated together with storage capacitors implemented using on-chip interconnect in a 0.35-μm bulk process. Integrated vertical plate capacitors enable dense energy storage without limiting optical efficiency. Tests were conducted with both a white light source and a green laser. Measurements indicate that 225 μW/mm^2 output power may be generated by white light with an intensity of 20 kLUX.**

***Index Terms*—Energy harvesting, low-power design, photodiodes.**

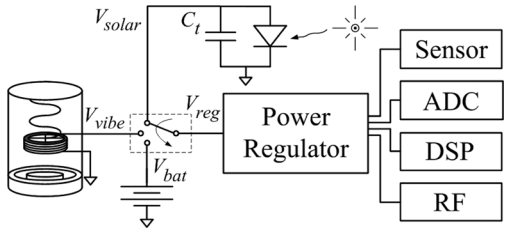

Fig. 1. Low power wireless system powered from energy scavengers and a battery. Energy sources include solar ($V_{\rm solar}$), mechanical vibration ($V_{\rm vibe}$) and a battery ($V_{\rm bat}$). A mux switches between the unregulated energy sources.

I. Introduction

THE emerging application of wireless sensor networks continues to drive the need for ultra low power system design. Wireless sensors can enable a variety of applications including interactive environments for medicine, environmental monitoring networks, military target tracking, and detection of chemical and biological weapons. In many of these wireless systems, the power source is a bottleneck that limits system lifetime and performance, adds manufacturing cost, and increases system volume and maintenance expenditures. Delivering power to wireless sensor network nodes is a significant system design challenge. Solar energy harvesting has been proposed to extend the lifetime of these networks beyond the limitations which have been previously imposed by batteries [1]. Prior works have successfully demonstrated powering wireless systems through discrete photovoltaic cells together with separate energy storage devices using board level designs [2], [3]. To reduce system cost and volume it is desirable to integrate energy harvesting and storage with data acquisition, data processing, and communication circuits. Recent advances in very low power signal processing architectures for sensors [4] has created the opportunity to use CMOS photodiodes, similar to those used in digital cameras, for solar energy harvesting. Moreover, the increase in interconnect capacitance as CMOS processes scale provides an opportunity to store the harvested energy without requiring battery materials to be integrated on-chip. This paper describes an array of photodiodes, modeled after a passive-pixel imager, integrated together with storage capacitors in a commodity CMOS process. Also described is the potential of this approach to increase the lifetime of wireless sensor nodes.

Fig. 1 shows a block diagram of a typical wireless sensor node, which is powered by a combination of energy scavenging and battery technology. The system consists of sensors that can observe the environment, an analog-to-digital converter (ADC) that can quantize the analog signal from the sensors, a digital signal processing (DSP) core that can analyze and encode the quantized data and a transceiver (RF) so that the node can transmit and receive information. Light energy is converted to electrical energy through a photodiode and mechanical vibrations are converted to electrical energy by an electromechanical transducer [4]. A multiplexer (mux) is used to switch between energy sources. The system's energy gathering ability will depend on environmental conditions, which can change over time. Hence, the scavenged energy needs to be regulated before being used by these functional blocks.

In general, these types of systems work on very low duty cycles, where the sensor node will be in a rest state for the majority of the time. Periodically, the sensor node will wake up, take a snapshot of the environment measured by its sensors, perform its computations, and transmit any data before returning back to the rest state. Each of the functional blocks shown in Fig. 1 has its own power requirement. Previous work has shown that efficient ADCs and DSPs can achieve average power levels in the sub-milliwatt range [5], [6]. However, low power ADCs usually suffer from diminished power supply rejection [5]. Minimizing the voltage ripple on the power supply for the ADC is important for maintaining accuracy. The RF block typically requires significantly more peak power than the other system blocks, and the DSP has the most relaxed supply ripple requirements due to the robustness (large noise margin) of the digital circuitry. For low duty cycles, the average power for the system (estimated from the literature [4]–[7]) can be under 5 μW.

In Section II, we illustrate the design of photodiodes for energy scavenging. Section III describes how interconnect

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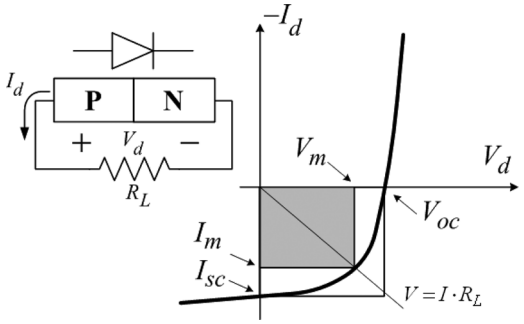

Fig. 2. Typical characteristics of a photodiode under illumination along with a schematic. The optimum configuration for harvesting energy is found with the load resistance R_L that maximizes the product of the current through the diode I_m and the voltage across the diode V_m.

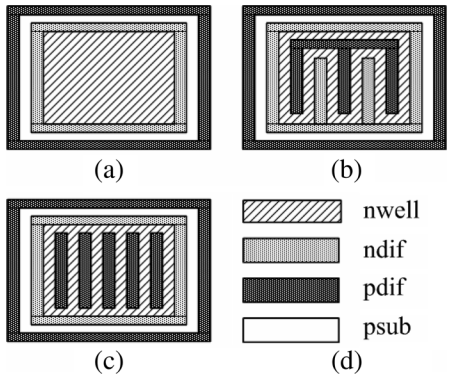

Fig. 3. Top view of photodiodes. (a) D1. (b) D2. (c) D3. (d) Layer key.

capacitance can be exploited for storing the scavenged energy. Section IV reports experimental integrated photodiode test results while Section V discusses trends in integrated energy storage. Finally, Section VI provides conclusions from this research.

II. Energy Scavenging Photodiodes

The layout and design of an integrated energy scavenging photodiode must balance several competing factors [8]. The charge generated in the depletion region of the photodiode is meant to be stored in on-chip capacitors; therefore the physical layout of the diodes should facilitate both the solar energy harvesting and capacitive energy storage. The light that reaches the photodiodes' depletion region must first pass through the passivation layers and avoid the metal storage capacitance, which is constructed on top of the diode to minimize area.

A figure of merit (FOM) is needed in order to quantitatively assess the performance of the photodiodes. The FOM used here is also known as the fill factor, which is defined as the maximum output power obtainable divided by the product of the open circuit voltage (V_{OC}) and the short circuit current (I_{SC}), for a given light intensity. Fig. 2 shows a schematic for a photodiode under illumination delivering power to a load resistance R_L on the left, along with an example IV curve shown on the right. The maximum output power is the product of V_m and I_m, which are in general functions of the incident light intensity. Graphically, the figure of merit can be seen as the ratio of the two rectangles in Fig. 2, and a FOM equal to one would be ideal.

To explore the photodiode design tradeoffs experimentally, three different geometries were fabricated and tested. Fig. 3 shows the top view layout for the three photodiodes along with a layer key. The first design, photodiode D1, is shown in Fig. 3(a) and is similar to a passive pixel structure used for a CMOS imager [9]. The p-substrate and n-well form the diode. The second photodiode design D2 is shown in Fig. 3(b). This structure has the addition of interdigitated p-diffusion and n-diffusion fingers inside the n-well. These fingers help to form the additional p-diffusion to n-well diodes, which can be wired in parallel with the well-substrate diode. The final design D3 is shown in Fig. 3(c). The D3 layout is similar to the D2 layout except the n-diffusion fingers are replaced with p-diffusion fingers allowing for more depletion region area and energy harvesting ability. In total, 11 different diodes were fabricated in three different sizes. Photodiodes for energy scavenging differ from imaging pixels in the way in which they are optimized. Imagers are designed to minimize noise, dark current, and lateral photocurrent (which can create pixel-to-pixel crosstalk), while photodiodes for energy scavenging are designed to optimize efficiency and output power. Imaging sensors are commonly designed to drive a high impedance capacitive load presented by a sense amp, while energy scavenging photodiodes are designed to drive resistive loads. Also, the energy storage capacitors which are beneficial for storing the harvested energy from the photodiodes would limit the refresh rate of an imager.

Larger photovoltaic cells were first discovered in the mid 1800's and had efficiencies of less than one percent. Since then, numerous advances in materials and technology have allowed for substantial increases in efficiency and size. Many commercially available silicon photovoltaic cells boast efficiencies near 17%. Recent advances have allowed silicon photovoltaic cells to reach efficiencies nearing 24% [10]–[12]. A commonly cited theoretical model [13] for the fundamental limits of silicon solar cells that takes into account Auger recombination and absorption puts the maximum efficiency at 29.8%. It is possible to overcome this theoretical limit by using photovoltaic cells that consist of stacked junctions of multiple materials. Each junction is designed to have a different band gap, and therefore to be responsive to a different optical wavelength. Together the multiple junctions in the solar cell can absorb a wide spectrum of light, thereby increasing its efficiency. For instance, three-junction InGaP/InGaAs/Ge solar cells have been able to achieve efficiencies of 37% [14]. More recently, the state-of-the-art solar cell has been able to achieve an efficiency of 50% with a 6 junction design [15]. In general, the more complex and efficient solar cell designs come with increased costs. It is common to use price per peak watt (Wp) as a metric for comparing commercial photodiodes. In recent years, the typical price for silicon photodiodes with efficiencies near 17% was in the range of \$3.5–4.5/Wp, with an estimated decrease to \$1/Wp for the near future [16].

The integration of the photovoltaic cells along with analog and digital signal processing circuits is of interest in this work. The scaling of a photovoltaic cell from large, standalone arrays to the integrated circuit level will impact the cell's output

power, efficiency, optimal load resistance, and optical properties of the photodiode. Energy harvesting systems with high power requirements may require a significant area allocation for integrated photodiodes. Although integrated photodiodes can also double as power supply bypass capacitors, the additional cost associated with the photodiode's footprint could potentially limit its usefulness to larger feature size technologies. True integration of photodiodes and active circuitry on the same die may require covering the active circuitry with a metal cap to block the incident light from potentially degrading signal integrity. A substrate trench, forming a barrier, can also be employed to help limit the lateral photocurrent [17], [18] traveling from the photodiodes to the active circuitry.

The construction of the storage capacitance and routing for the photodiodes must not degrade the optical efficiency (OE), which is defined as the fraction of incident light onto the chip's surface which reaches the photodiode [19]. In general, the optical efficiency is influenced by three loss factors: reflection loss, absorption loss, and critical angle loss. Once photons reach the photodiode, the quantum efficiency (QE) determines how many photons will generate electron-hole pairs. The product of OE and QE should be maximized by the geometry of the photodiode and storage capacitance to maximize both the energy harvesting ability and storage capacity.

III. Integrated Storage Capacitors

A. Capacitance Characterization

One goal of this work is to determine the maximum energy per area that can be gathered from solar energy and stored in a standard CMOS logic process. Determining the maximum stored energy requires first calculating the capacitance per area. The capacitance analysis will start with the stored energy relationship, which can then be divided up as a sum of two components: the energy stored in the metal capacitance and the energy stored in the junction capacitance. The total capacitance is given by

$$C_t = \frac{2 \cdot E_v}{\Delta V_{\text{solar}}^2} = C_m + C_d \tag{1}$$

where E_v is the energy stored in the capacitor, ΔV_{solar} is the voltage difference between the capacitor plates, and C_t is the total capacitance, which is made up of the metal capacitance C_m and the diode capacitance C_d.

When the mux in Fig. 1 switches to the solar cell, the total charge accumulated in the storage capacitance is shared with the capacitance at the input of the regulator. This charge sharing will yield a potential at the input of the regulator which is less than the initial stored potential before the switch. With ideal switching the voltage at the input of the regulator can be written as

$$V_{\text{reg}} = \frac{C_t}{C_t + C_r} V_{\text{solar}} \tag{2}$$

where C_r is the input capacitance of the regulator present at the right of the rotating switch in Fig. 1. It is seen here that to limit this attenuation factor the storage capacitance C_t should be made as large as possible.

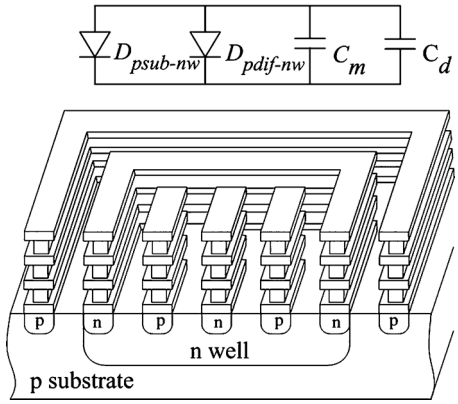

Fig. 4. Side view cutaway of photodiode D2. Metal connected to p- and n-diffusions correspond to top and bottom capacitor plates, respectively.

Fig. 4 shows a side cutaway of photodiode D2 with an interconnect metal storage capacitor built on top of the photodiode to minimize area and maximize energy density. A capacitor structure that simultaneously enables a high OE and a large capacitance density is the vertical parallel plate structure. The incident light will pass through the plates vertically before reaching the photodiodes. The interdigitated p- and n-diffusion fingers forming the photodiode junctions of D2 can align with the vertical plates allowing for easy routing to the capacitor plates. Here, the n-well p-diffusion diodes are wired in parallel with the n-well p-substrate diodes and the metal storage capacitance is added to the depletion capacitance of the junctions. Since the area between the storage capacitor's parallel plates also functions as the aperture for the light, an increased capacitance density will yield a smaller aperture and consequently a decrease in OE. This design has an inherent trade off between OE and metal capacitance density.

Capacitance simulations were carried out on geometries similar to those shown in Fig. 4 using the software package Momentum [20] assuming four metal layers, a minimum vertical parallel plate separation of 0.6 μm, a silicon dioxide dielectric of thickness 0.64 μm, and an average metal thickness of 0.71 μm. Photodiode D3 has less metal capacitance than the other two designs due to the need to connect the p-diffusion fingers together. For a diode area of 338 μm^2 in the given technology, the theoretical limit on the maximum obtainable interconnect capacitance (TL1) is close to 1 pF, while the semi-empirical upper bound (SEUB) is 0.616 pF, determined as in [21]. D3 has a capacitance density close to 42% of SEUB (neglecting diffusion capacitance C_d).

The total pn junction capacitance is the sum of the capacitances from the diffusion-well diode $D_{\text{PDIF}-\text{NW}}$ and the substrate-well diode $D_{\text{PSUB}-\text{NW}}$. This capacitance can be modeled by a particular capacitance per unit area, C_j and a particular side wall capacitance per unit length, C_{sw}. These capacitances are in general nonlinear (voltage-dependent). For photovoltaic energy scavengers, the photons incident on the depletion region will generate electron-hole pairs. The resulting charge separation from this generation will produce a potential drop across the photodiode resulting in a forward-biased pn-junction. Subsequently, the width of the depletion region will shrink with an

TABLE I
CAPACITIVE CHARACTERIZATION ($\mathrm{Area} = 338\ \mu\mathrm{m}^2$) CAPACITANCE

Capacitance	D1	D2	D3	TL1	SEUB
C_m 90 nm (pF) (9M)	8.938	8.938	7.741	34.40	19.93
C_m 90 nm (pF) (4M)	4.200	4.200	3.640	16.10	9.334
C_m 180 nm (pF) (6M)	1.452	1.452	1.203	5.544	3.225
C_m 180 nm (pF) (4M)	1.049	1.049	0.862	4.026	2.333
C_m 350 nm (pF) (4M)	0.254	0.254	0.216	1.004	0.616
C_{do} (pF)	0.070	0.178	0.285	–	–
C_d (pF)	0.113	0.286	0.460	–	–

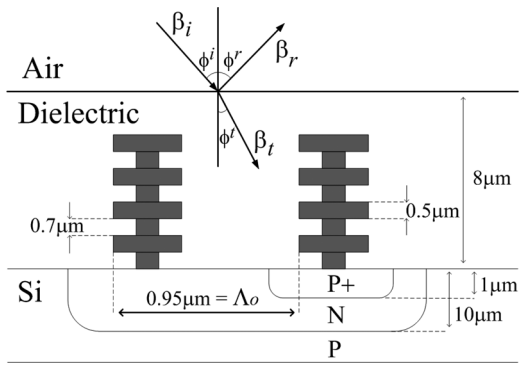

Fig. 5. Side view of the optical path for photodiode D2, dimensions are approximate for a 0.35-μm CMOS process.

increase in forward potential across the pn-junction. This decrease in depletion width will lead to an increase in the depletion capacitance, which can be modeled using a square root dependence with the potential voltage across the photodiode. Assuming an abrupt doping profile, the pn junction capacitances can be written as [22]

$$C_d = \frac{C_{\mathrm{do}}}{\sqrt{1 - \frac{V_{\mathrm{Solar}}}{\varphi_o}}} = \sum_{i=1}^{N} (C_{\mathrm{sw}} P_i + C_j A_i) \tag{3}$$

where φ_o is the built in potential of the junction, A_i is the area, and P_i is the perimeter of the ith diode. Table I summarizes the simulated capacitive characterization of the three diodes shown in Fig. 3. Table I also estimates C_m for 180 nm and 90 nm CMOS technologies given the same die area for different numbers of available metal layers. The C_d given here is calculated with a junction voltage of 0.55 V, which is close to the open circuit voltage of the photodiodes under normal indoor lighting conditions.

B. Optics

Fig. 5 shows the side view of the optical path for photodiode D2 with storage capacitance. The gray structures are the four metal layers with connecting vias which form the parallel plate capacitors. The numbers given for the geometry are approximate for a 0.35 μm process. This process uses a p-type substrate, which forms the anode of the photodiode, and an n-well, which forms the cathode. The incident beam must pass from the air through the dielectric region before it reaches the silicon substrate. Reflection losses will occur at the air-to-dielectric and dielectric-to-silicon boundaries. Commonly, the dielectric region is split into sub regions for each of the metal and via layers. The manufacturing process produces a slightly different dielectric constant for the metal layers than it does for the intermetal (via) layers. The resulting structure will have alternating horizontal layers of different dielectric constant in the dielectric region, and can be modeled as a periodic dielectric medium [23].

We now summarize the equations for the OE, QE, and the total external efficiency for the photodiode-capacitor structure. The OE for a single boundary can be written as

$$\eta_o = (1 - R)\,(1 - \exp(-\alpha d)) \tag{4}$$

where R is the percent of reflected energy, α is the power absorption coefficient, and d is the average depth of the pn junction. The QE for a photodiode is written as

$$\eta_q = \frac{\left(\frac{I_p}{q}\right)}{\left(\frac{P_{\mathrm{opt}}}{h\upsilon}\right)} \tag{5}$$

where I_p is the generated electrical current, q is the charge of an electron, P_{opt} is the incident optical power, h is Planck's constant, and υ is the frequency of the incident light. Equation (5) can be thought of as the ratio of number of carriers generated per incident photon. The external efficiency is the product of the OE and the QE, which gives us electrical power out divided by optical power in

$$\eta = \eta_o \eta_q = \frac{\text{Pout Elec.}}{\text{Pin Opt}}. \tag{6}$$

In general, this ratio is a function of electrical load and light conditions, and can be determined with the load that generates the largest output power for a given light intensity.

Calculations using the scattering matrix formulization method of multilayer optics [19], [24] for a normal angle of incidence and the geometries in Fig. 5 suggest a maximum optical efficiency near 65% with an incident wavelength of 532 nm. This number does not take into account the additional optical losses associated with the reflections from the metallic vertical parallel plate structures. Reflective losses from the air-to-dielectric and dielectric-to-silicon boundaries account for most of these losses, while optical absorption plays a somewhat smaller role. In many commercial photodiodes, random chemical texturing [25] is used on the top surface boundary, which by reducing the reflections can increase the optical efficiency beyond 90%. Since the n-wells protrude deep into the substrate, the optical absorption losses for the n-well to p-substrate photodiodes will be larger than those for the n-well to p-diffusion photodiodes. In most CMOS processes the junction depth will tend to increase with larger cross sectional junction footprints. Therefore, n-well to p-diffusion

photodiodes made of the minimum width will result in the highest optical efficiency.

The vertical parallel plate storage capacitors built on top of the photodiodes form a type of periodic grating structure [26]. Some of the incident light will diffract from this metal grating before reaching the photodiode in the substrate. This diffraction grating is a parasitic effect from having the storage capacitance double as the aperture for the photodiodes. The transmittance of light through the grating is wavelength dependent, and the transfer function between the incident and transmitted waves will typically have a band stop characteristic. The exact analysis of such grating structures can be quite challenging and requires solving the rigorous coupled-wave equations. Suppose Λ_{O} is the period of the grating, which is proportional to its resonant wavelength Λ_{R}. The resonant wavelength is the center wavelength of the stop band for the optical filter. In general, the exact relationship between Λ_{O} and Λ_{R} is a function of more than just geometry. The indices of refraction, angle of incidence, and polarization of the incident light also play important roles. Measured results from previous work have shown that at a normal angle of incidence a Λ_{O} of 950 nm (which is close to the dimensions used here) will yield a Λ_{R} near 1550 nm [27].

To optimize the density of capacitive storage in the prototype, the minimum dimensions of the 0.35 μm CMOS technology were used to space the vertical parallel plates. The work from [16] shows that the resulting geometry for the interconnect capacitance generated a diffraction grating with a resonance outside the absorbable wavelengths of silicon, and consequently shouldn't decrease the overall efficiency of the photodiode. However, as CMOS technology scales, Λ_{O} will decrease and the optical stop band will align itself within the spectral responsivity of silicon, consequently decreasing the OE of the photodiode. The fundamental property of the grating is to organize the transmitted and reflected light into discrete directions, called diffraction orders. The angles of the diffracted light are given by the grating equation

$$\phi_d = \sin^{-1}\left(\frac{\Lambda_0}{m\lambda} + \sin(\phi_i)\right) \tag{7}$$

where m is an integer which specifies the diffraction order, λ is the wavelength of the incident light, and ϕ_i is the angle of incidence. As the geometric grating period becomes smaller, the diffraction angles of the transmitted and reflected waves increase, limiting the optical throughput. By tailoring the ratio of metal width to metal spacing, periodicity, and depth of the diffraction grating a designer can have some control over its filtering effects. The top surface of the metal diffraction grating will tend to reflect the incident light, thereby increasing the optical losses. In order to minimize these reflective losses, the vertical parallel plate metal thickness should be kept as small a possible. Previous works have measured an optical transmittance of 53% through a similar periodic metal grating structure with metal width = metal spacing = 450 nm [28]. This is an additional 12% loss in optical efficiency from the previously calculated 65% when combining the integrated metal storage capacitance with the energy harvesting photodiodes.

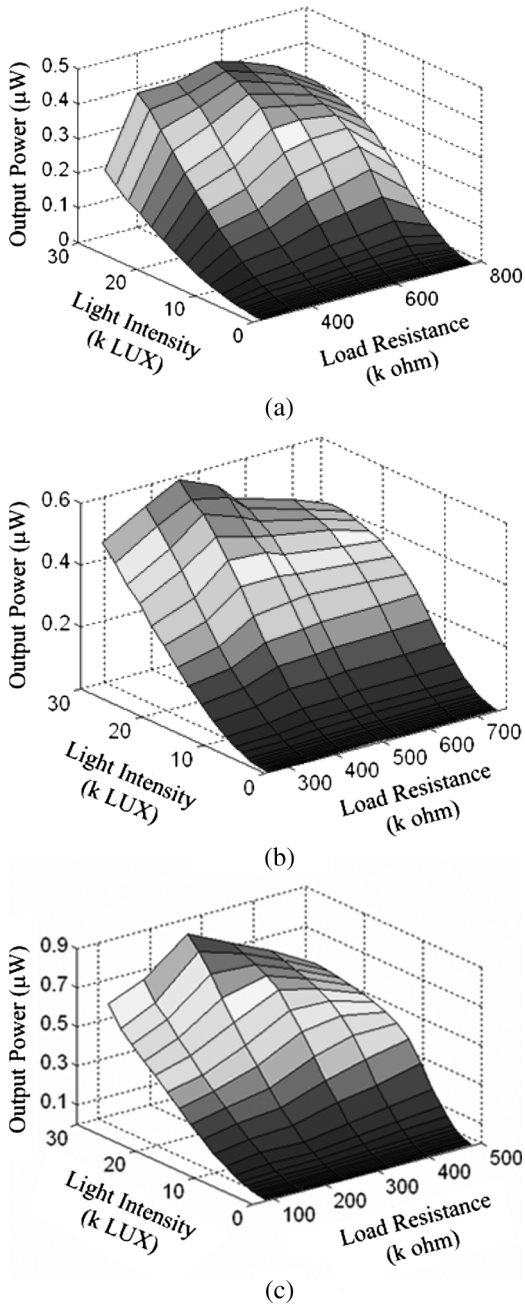

Fig. 6. (a) Output power versus incident light intensity and load resistance. Active area = 3000 $\mu\mathrm{m}^2$, photodiode D1 output power = 400 nW when RL = 500 kΩ and input intensity = 25 kLUX. (b) Photodiode D2 output power = 600 nW when RL = 400 kΩ and input intensity = 25 kLUX. (c) Photodiode D3 output power = 800 nW when R_L = 230 kΩ and input intensity = 25 kLUX.

IV. Experimental Results

A. White Light

Fig. 6(a) shows dc power measurements taken for a single series D1 diode powered by a normal 100-W tungsten filament light bulb. The generated power on the z-axis is plotted over input light intensity and load resistance. The light intensity is measured using an optical power meter in the unit of LUX, which is the SI unit for luminance defined as the amount of visible light per square meter incident on a surface. For photodiode

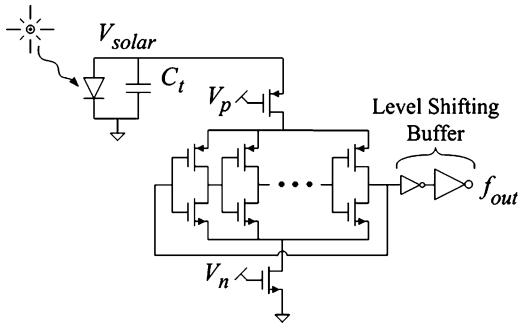

Fig. 7. Test setup showing photodiode, current starved ring oscillator, and level shifting output buffer.

D1, with an active area of 3000 μm^2, the peak power generated is a little more than 400 nW with a load resistance close to 500 kΩ and an input light intensity of 20 kLUX.

Fig. 6(b) shows the power measurements for photodiode D2. The same white light source was used and the active area of the photodiode was again 3000 μm^2. Here, the peak power for D2 is around 600 nW, which is about 50% more than with diode D1. This power was generated with a load resistance around 400kΩ, which is less than D1's optimal resistance for the same light intensity. This shift to a lower optimal resistance is largely attributed to the increased pn-junction area that D2 has over D1 due to the addition of the $D_{\mathrm{PDIF-NW}}$. This increase in junction area consequently decreases the photodiode's internal resistance. For maximum power transfer the load resistance should match the photodiode's internal source resistance.

Fig. 6(c) shows the power curves for the photodiode D3, with the same conditions as the tests for the previous two diodes. Out of the three varieties of photodiode, D3 has the highest peak power, close to 800 nW with a load resistance of 230 kΩ. This decrease in optimal resistance is again largely attributed to the increase in pn-junction area, due to the increased number of $D_{\mathrm{PDIF-NW}}$.

Another interesting observation is that the optimal resistance value changes as a function of the light intensity. This input optical light dependency on the internal source resistance is largely attributed to the nonlinearity of the photodiode's IV curve in the fourth quadrant of Fig. 2. Here, it can be seen that a higher light intensity will yield a lower optimal load resistance.

To further verify the operation of the photodiodes, a ring oscillator was constructed on-chip that uses the scavenged energy. Fig. 7 shows a schematic of the prototype system. It consists of a light source, integrated energy scavenging photodiodes, storage capacitance (C_t), a ring oscillator, and buffers to drive the signal off-chip. The nine-stage ring oscillator employs current starving techniques with both pMOS and nMOS transistors to enable frequency tuning of the oscillator.

A level shifting output buffer was used so that the oscillator's operation could be observed with little loading. Bias voltages V_p, V_n and the power supply for the output buffer were generated off-chip for testing purposes. In a single-well p-type substrate process, photodiodes working under forward bias drive the n-well below ground, potentially causing unwanted substrate currents to flow. Therefore, two test chips are required to

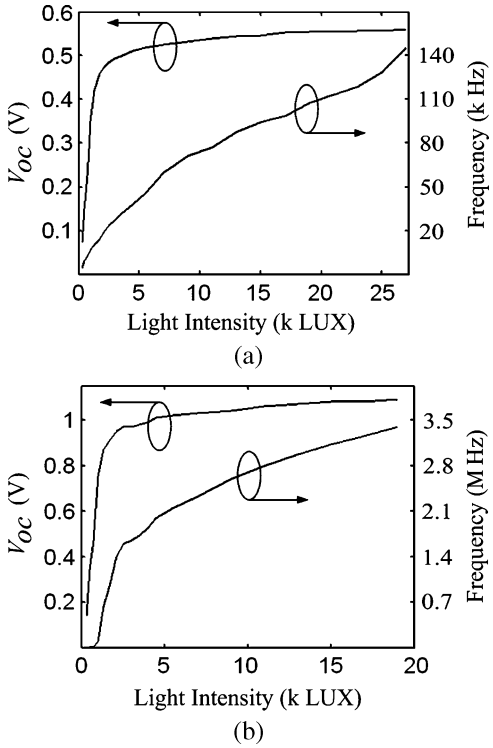

Fig. 8. (a) Measured plots of D3 showing VOC and ring oscillator frequency. (b) Measured plots showing VOC and ring oscillator frequency for two D3 photodiodes stacked in series.

demonstrate the oscillator. A twin- or triple-well process is able to eliminate this limitation with increased fabrication costs. Silicon-on-insulator (SOI) technologies, which, although they are becoming more common, are still relatively costly, are also able to get around this limitation. Alternatively, a different wiring approach can be taken. An n-well to p-diffusion photodiode can generate a usable positive voltage when the n-well is tied to ground, or any other positive voltage below the supply. By bringing the n-well voltage below the supply, additional substrate currents may flow from the photodiode thereby limiting its achievable efficiency.

The fabricated ring oscillator will vary its oscillation frequency in conjunction with the input light intensity. Thus, the oscillator works as a simple light intensity meter which converts intensity to frequency.

The output of the oscillator could then be used to clock an energy scalable system [29], [30], where the system clock rate will adapt automatically to the available energy in the environment. Fig. 8(a) plots the ring oscillator frequency and the open circuit voltage (V_{OC}) versus light intensity for a single D3 diode. With one series diode $V_{\mathrm{Solar}} = 0.55$ V and the oscillator dissipates 67.3 pW (0.48 fJ per cycle) at a maximum frequency of 140 kHz. The knee in the curve of the open circuit voltage is near 2.5 kLUX. By using several chips we are able to connect multiple diodes together. Fig. 8(b) plots the ring oscillator frequency and open circuit voltage for two D3 diodes stacked in series. A maximum open circuit voltage of 1.09 V and a ring oscillator frequency near 3.5 MHz is measured for this configuration.

Fig. 9 shows the figure of merit (FOM), plotted over the incident white light intensity. Photodiode D1 has the best FOM at

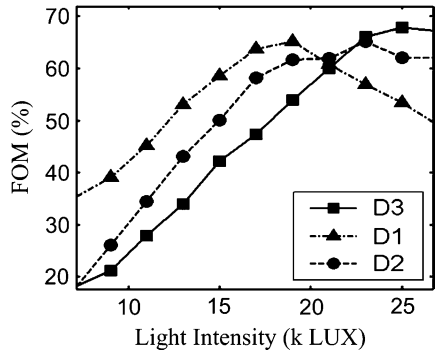

Fig. 9. Measured FOM plotted versus input light intensity.

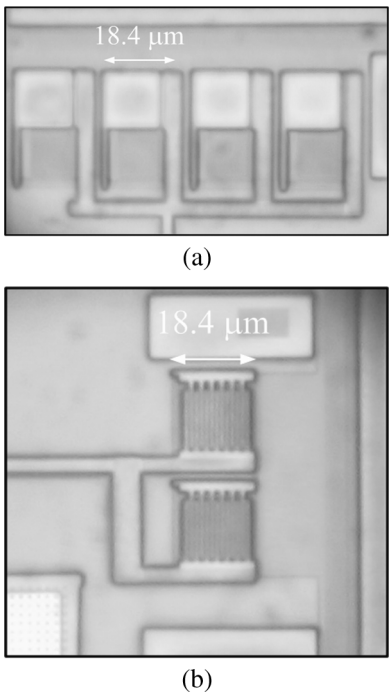

Fig. 10. (a) Die photograph showing four D1 photodiodes wired in parallel. (b) Die photograph showing two D3 diodes wired in parallel.

lower light intensities while photodiode D3 has the best figure of merit for higher light intensities.

One possible explanation for these results is that the introduction of the p-diffusion to n-well diodes in D2 and D3 increases recombination in the photodiode, which limits the FOM at lower light intensities. However, the same diffusion-to-well diodes help to increase the photodiode's energy harvesting abilities at higher light intensities.

Fig. 10 shows photographs of the diode test structures from a test chip. Fig. 10(a) shows four D1 diodes wired in parallel. Fig. 10(b) shows two D3 diodes wired in parallel. Each of these diodes are 18.4 μm on a side, and were constructed in a 0.35-μm CMOS process.

B. Green Laser

The measured data described thus far has been generated using an incandescent light bulb as the light source to illuminate the photodiodes. This light bulb worked well to test the power

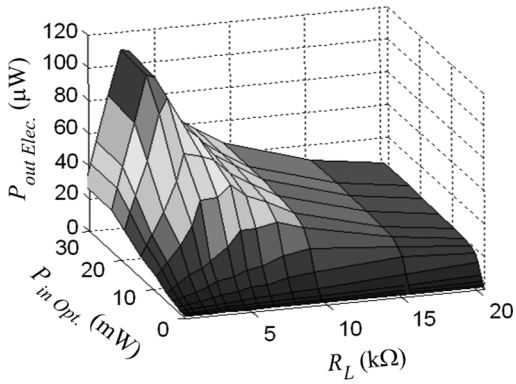

Fig. 11. Generated electrical output power for photodiode D3 versus green laser input light intensity ($\lambda = 532$ nm) and load resistance. Input optical power is for total chip surface.

generated from the photodiodes under normal environmental conditions, but we would also like to determine the overall efficiency of the photodiodes experimentally. To do this we first need to determine the total incident optical power reaching the surface of the photodiodes. The light generated from a tungsten filament has a wide spectrum, and to determine the total incident optical power would require integrating the light intensity over the entire absorbable spectrum of silicon. However, when illuminating the photodiodes from a narrowband collimated source such as a laser, the process of determining the total incident optical power can be greatly simplified. The chosen narrow band optical source for the efficiency measurements was a 30 mW green laser with a wavelength of 532 nm. The collimated beam generated from the laser is first reflected off multiple mirrors before being passed through a variable optical attenuator and then finally onto the chip's surface. The mirrors are used for fine tuning the beams position and the attenuator gives the ability to test the photodiodes at multiple optical intensities.

Fig. 11 shows the dc power measurements for diode D3 when illuminated by the green laser. Here, generated electrical power is plotted versus total incident optical power and load resistance. The incident power was measured using a solid-state optical power meter, which had been calibrated for the laser. The optimal load resistance is much lower than for a white light source, which is mainly due to the difference in power levels between the laser and incandescent bulb. In Fig. 11, the plotted optical power is the total optical power incident onto the chip, which is significantly larger than the photodiode. This mismatch in areas has two main effects: first, only a percentage of the input power actually reaches the photodiodes and second, the resulting ambient optical energy will excite lateral photocurrent, which will contribute to the output power.

An optical beam chopper, optical power meter, and oscilloscope were used to measure the beam diameter of the laser using the knife edge method [31]. The measured diameter of the optical beam was close to 0.8 mm, which is more than ten times larger than the photodiodes under test. With this large beam-to-photodiode area ratio, it is valid to use the top-hat approximation [32] for the optical power distribution, assuming the beam was centered directly on top of the photodiode. In

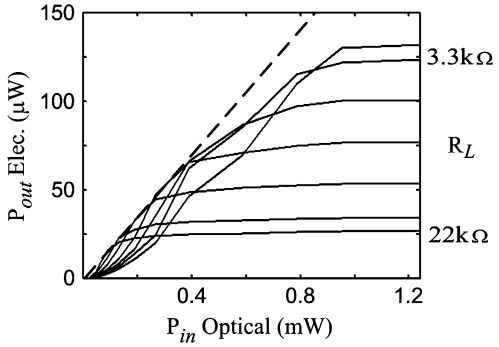

Fig. 12. Generated electrical output power for photodiode D1 versus input light intensity ($\lambda = 532$ nm) and load resistance. Dashed line represents linearized transfer function. Input optical power is calibrated for the photodiode area.

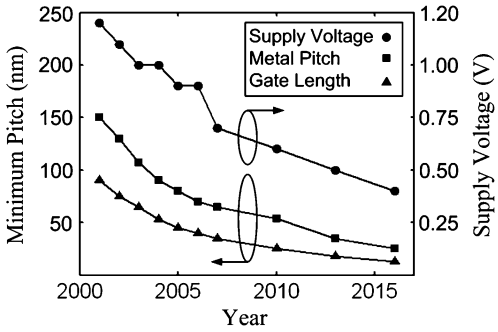

Fig. 13. Technology trends from ITRS roadmap. Minimum printed gate length, minimum pitch for metal interconnect, and supply voltage over time.

order to minimize the lateral photocurrent from the measurements, a differential approach was used. For the efficiency tests, power measurements were taken first with two identical photodiodes wired in parallel. Then, one of the photodiodes was removed by an ablation laser coupled to a microscope, and the power measurements were taken again. The difference in power between the two measurements is assumed to be the power generated from a single photodiode. Fig. 12 shows the results with the differential calibration of the green laser measurements for diode D1, which is a plot of optical power in vs. electrical power out. Each of these curves corresponds to a different load resistance between 3.3 and 22 kΩ. The dashed line represents the maximum linearized transfer function from optical to electrical power. With 25 mW of light incident onto the chip's surface, less than one-third of the generated electrical power from the photodiodes was observed to originate from lateral photocurrent traveling in the substrate.

V. Integrated Energy Storage Trends

If the size and the cost of the wireless sensor node allows for an off-chip storage element, a small capacitor or battery could be used instead of or in addition to the metal interconnect capacitance. In this section, we examine several electrical energy storage technologies which are compatible with system-in-package integration [33], [34]. Large energy storage devices are often the limiting factor for miniaturizing electrical systems, and it can be advantageous for cost and size to integrate passive components into the package or chip [35]. Also, it is common to achieve a higher efficiency through a larger quality factor [lower equivalent series resistance (ESR)] with in-package passive components than with on-chip components. We compare the energy density of ultracapacitors, ceramic capacitors, and printable microbatteries to what is achievable using metal interconnect capacitance on-chip below.

An ultracapacitor is an electrochemical capacitor typically made from carbon and with a high energy density due to a large surface area to volume ratio for the internal material. It has been previously shown that these ultracapacitors could reduce the high power demands on batteries in wireless systems by storing energy harvested from environmental sources [36], [37]. One advantage of ultracapacitors is the high number of charge/discharge cycles they can undergo before deterioration, which is approximately 100 000 cycles (roughly 100× better than contemporary battery technologies). Ultracapacitors thus far have primarily been used for hybrid vehicle applications with individual capacitor sizes reaching thousands of farads. In this section, we explore and compare the effect of technology scaling on interconnect capacitance density and ultracapacitor density. Fig. 13 shows information taken from The International Technology Roadmap for Semiconductors (ITRS) [38]. Here, the expected minimum pitch size for gate length (triangle), minimum pitch size for metal interconnect (square), and supply voltage (circle) are plotted over time. The ITRS predicts that by 2016 a transistor with a printed gate length of 15 nm will be powered from a supply voltage of 400 mV.

There are two major effects capacitance scaling will have on ultracapacitor density. First is the size of the capacitor. Fig. 14(a) shows a plot of reported capacitance density versus capacitance. These data points, which were taken from five manufacturers of ultracapacitors [39]–[43], show a strong correlation between capacitance density and capacitor size. The dashed line in Fig. 14(a) is the best fit linear model to the reported data points. The linear model predicts that a 10 μF and 100 pF ultracapacitor will have a capacitance density of 50 μF/mm^3 and 6 μF/mm^3, respectively. The scaling with size is attributed in part to the percentage of the volume consumed by packaging, which becomes greater with smaller capacitor values due to an increased surface area to volume ratio. This type of scaling will have minimal effect on the metal interconnect capacitance due to its high level of integration.

A second type of scaling which will affect the ultracapacitor energy density is supply voltage scaling. For many materials, the constraint on performance is governed by the maximum electric field, or energy density. By assuming the energy density of an ultracapacitor to be constant, from (1) we can decrease the maximum rated voltage and increase the theoretical limit of the capacitance [44], [45]. As technology scaling decreases the gate length and oxide thickness of MOS transistors, the supply voltage must also decrease in order to maintain the same electric field. Therefore, ultracapacitors that are designed to match current semiconductor technologies can see a potential increase in capacitance density resulting from voltage scaling. Fig. 14(b) plots the estimated capacitance density versus supply voltage: ultracapacitor (triangle), theoretical limit interconnect

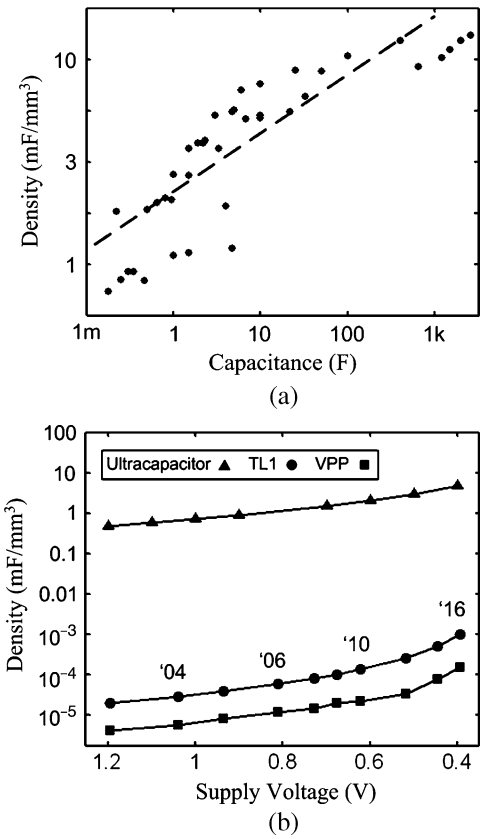

Fig. 14. (a) Ultracapacitor capacitance per unit volume versus total capacitance. Dashed line represents the linear best fit model. (b) Comparison of capacitance density versus supply voltage for a 10 μF capacitor for ultracapacitor technology, theoretical limit (TL1) of interconnect capacitance, and vertical parallel plate (VPP) interconnect capacitance. Supply voltage years correspond to the ITRS roadmap.

capacitance (circle), vertical parallel plate interconnect capacitance (square). The ultracapacitor density was generated from a second-order best fit model from reported data points for various supply voltages [39]. The increase in interconnect capacitance is due to a decrease in metal pitch, which is coupled to supply voltage through the ITRS predictions shown in Fig. 13. It is seen here that ultracapacitors have a much higher density than metal interconnect capacitors and as technology scales, the gap will shrink slightly. Ultracapacitors, however, also have certain drawbacks. In current technologies, ultracapacitors cannot store as much energy as a modern battery [46]. To achieve efficient energy transfer, ultracapacitors often require trickle charging (injecting pulses of current) which may require additional circuit overhead. The usable temperature of ultracapacitors is roughly $-40^{\circ} \sim 75\,^{\circ}$C while metal interconnect capacitors can work within the temperature range of the dielectric breakdown, which can exceed 200 °C for silicon dioxide [47]. Possibly the largest drawback of ultracapacitors is their large leakage current. A relatively small 140 mF ultracapacitor charged to 3.6 V has a rated leakage current of 5 μA [42] at room temperature, while a larger 4 F ultracapacitor charged to 2.5 V has a rated leakage current of 20 μA at room temperature [39]. Integrated metal storage capacitors in comparison achieve a negligible amount of leakage

TABLE II
ENERGY DENSITY ($V_{\mathrm{Store}} = 1$ V, $\mathrm{Volume} = 0.054$ mm^3)

Technology		Energy (J)	Charging Cycles
Ceramic (low quality)	[48]	110n	–
Ceramic (high quality)	[48]	50p	–
TL1**	[21]	9.15n	–
SEUB**	[21]	5.3n	–
FIREPower	[49]	7.35m	30
DC Sputter	[50]	7.53m	50
Electrochemical	[51]	1.87µ	–
Lithium Ion	[46]	3.18m	500
Ultracapacitor	[39]	26µ	100,000

** Interconnect energy calculated for a 90-nm process with nine metal layers

current as long as the oxide dielectric is relatively thick. This suggests a tradeoff between energy storage density with energy storage losses.

Ultra-small 201 package ceramic surface mount capacitors in current technologies have been able to provide up to 100 pF of high quality capacitance with low loss and a small ESR or up to 0.22 μF of a lower quality capacitor with a high ESR in a 0.6 mm $\times$0.3 mm $\times$ 0.3 mm package (0.054 mm^3) [48]. This corresponds to a capacitance density of 4.07 μF/mm^3 and 1.85 nF/mm^3, for the low and high quality capacitors, respectively. The higher quality capacitor is more than three orders of magnitude less dense than an ultracapacitor of the same capacitance.

Thin printable batteries compatible with system-in-package integration are currently under investigation [49], [50]. One type of printable battery that can be fabricated with ink jet technology has been projected to maintain an energy density of 350 Wh/liter (1.26 J/mm^3) over more than 30 discharge/charge cycles. So far these printable batteries have been limited by manufacturing techniques to have planar dimensions between 10–1000 μm and a thickness between 1–5 μm [49]. Another type of printable battery that is fabricated with high power dc sputtering techniques has been able to achieve thicknesses on the order of 2.4 μm while maintaining energy density for more than 50 discharge/charge cycles. These printed batteries have demonstrated an energy density of 1.29 and 0.675 J/mm^3 with a voltage of 2.15 and 1.5 V, respectively [50]. Rechargeable lithium ion battery technology has thus far not been able to achieve the miniaturization of printable batteries. Commercially available lithium ion batteries report an energy density of 1.53 J/mm^3 with a stored voltage of 3.6 V over 500 charging cycles [46]. Another type of thin electrochemical capacitor, based on mesocarbon microbeads, has been demonstrated to have thickness ranging between 15 and 100 μm. With a footprint of 25 mm^2 these electrochemical capacitors can achieve a capacitance density of 34.66μF/mm^3 [51].

The energy stored in the volume of a 201 package (0.054 mm^3) at 1 V for the technologies described above is listed in Table II. It is clear from Table II that interconnect capacitance energy storage is not competitive in terms of density with almost all system-in-package alternatives. Although the density of low ESR ceramic capacitors is lower than the interconnect capacitance, these components are more suitable for signal processing

TABLE III
MEASURED RESULTS (25°C, Diode Area = 338 μm^2)

Parameters	D1	D2	D3	[10]
Power (nW)	50	63	76	–
Energy Stored (fJ)	26	35	31	–
FOM (%)	65	66	62	79
Capacitance, C_m (pF)	0.245	0.254	0.216	–
V_{OC} (mV)	465	525	533	669
I_{SC} (nA)	165	182	230	–
Pmax (μW)*	5.4	5.7	8.2	–
Pavg (μW)*	3.3	3.4	5.3	–
η (%)	16*	17*	24*	18-21

* $P_{\text{in Optical}} = 34.2\ \mu$W, green laser ($\lambda = 532$ nm)

applications than for energy storage. If the application can tolerate extremely small amounts of energy storage or the cost of a system-in-package solution is prohibitive, then on-chip interconnect may be a viable alternative.

VI. CONCLUSION

Table III summarizes and compares the results of the integrated photodiodes and storage capacitances with a commercially available solar cell [10]. Unless otherwise noted these measurements were conducted with an incident white light intensity of 20 kLUX, similar to being outside on a sunny day. Integrated photodiodes have similar overall efficiencies to commercial crystalline silicon solar cells. The differences shown in the last row of the table can be attributed to different measurement conditions (green laser illumination in our experiments versus solar illumination in [10]).

Based on these results, design D3 with area 150 μm $\times$ 150 μm can deliver 5 μW to power the system described in Section I above. D1 needs 184 μm $\times$ 184 μm and D2 needs 164 μm $\times$ 164 μm to deliver 5 μW. Without illumination, the system energy must be supplied by the integrated storage capacitors. For a 25 mm^2 total photodiode area consisting of 3 diodes in series with the metal storage capacitances for each diode connected in parallel, D1, D2, and D3 can supply enough energy for the DSP in [4] to produce 687, 745, and 903 output samples respectively. The energy density of fully integrated storage capacitors is not competitive with system-in-package solutions such as ultracapacitors or printable batteries, even with scaling to the end of the ITRS roadmap. However, for applications with very low energy storage requirements or cost constraints which limit system-in-package integration, exploiting interconnect parasitic capacitance for storage may be a viable solution. The combination of integrated solar energy scavenging and storage can enable a new generation of low cost, long lifetime, small volume systems for future wireless sensor networks or RFID applications.

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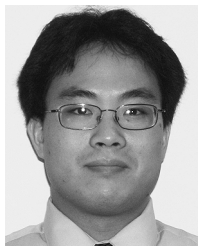

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