Integrated Energy-Harvesting Photodiodes With Diffractive Storage Capacitance

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Abstract—Integrating energy-harvesting photodiodes with logic and exploiting on-die interconnect capacitance for energy storage can enable new, ultraminiaturized wireless systems. Unlike CMOS imager pixels, the proposed photodiode designs utilize p-diffusion fingers and are implemented in a conventional logic process. Also unlike specialized solar cell processes, the designs utilize the on-chip metal interconnect to form a diffraction grating above the p-diffusion fingers which also provides capacitive energy storage. To explore the tradeoffs between optical efficiency and energy storage for integrated photodiodes, an array of photovoltaics with various diffractive storage capacitors was designed in a 90-nm CMOS logic process. The diffractive effects can be exploited to increase the photodiodes' response to off-axis illumination. Transient effects from interfacing the photodiodes with switched-capacitor DC–DC converters were examined, with measurements indicating a 50% reduction in the output voltage ripple due to the diffractive storage capacitance. A quantitative comparison between 90-nm and 0.35-μm CMOS logic processes for energy-harvesting capabilities was carried out. Measurements show an increase in power generation for the newer CMOS technology, however at the cost of reduced output voltage. One potential application for the integrated photodiodes is harvesting energy for a subdermal biomedical device.

Index Terms—Diffraction grating, energy-harvesting, implantable biomedical device, integrated storage, low power, photodiode.

I. INTRODUCTION

CMOS technology scaling has continued to reduce the size and active power consumption of electronic devices.

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This trend has opened the door for energy harvesters to power wireless systems through extracting mechanical, thermal, or solar energy from the environment. Increased system integration has allowed solar energy harvesters, in the form of passive photodiodes, to be implemented on the same silicon die as active circuitry, which can be powered by the harvested energy. These integrated photodiodes [1], [2] are modeled after a passive pixel architecture [3], which can form the basis for CMOS imagers. Previous works have outlined the use of environmental energy-harvesting for powering wireless systems [4]–[23]. For many wireless systems, photovoltaics (PVs) are a viable source for energy-harvesting [5]–[16]. Integrating the solar energy-harvesting on the same die as other parts of the system enables reduced system cost and size. The concept of a system, which consists of a photodiode array, a DC–DC converter with optional maximum power point tracking (MPPT) (included depending on power budget and power available) which supplies power to the sensor, analog-to-digital converter (ADC), digital signal processing (DSP), and communication blocks, all on the same die, is proposed in Fig. 1(a). However, side effects such as lateral photocurrent may become problematic [24]–[26] if the parasitic diode formed between the p-substrate and the n-well is utilized in the photodiode array. Fig. 1(b) shows the area of the concept IC dominated by the photodiode array, whose output voltage is then conditioned before supplying power to the other blocks. When solar energy alone is not enough, multiple energy-harvesting transducers can be combined to increase the total generated energy and can be supplemented with a battery or ultracapacitor to sustain peak loads [19]. Efficiently combining the multiple sources can prove to be difficult, especially with power budgets in the microwatts. We are presently developing a prototype that implements this concept and will report our results in future work.

In this paper, we explore several aspects of integrated PVs in energy-harvesting applications through the design, experimental characterization, and circuit modeling of several prototype photodiodes with diffractive storage capacitance fabricated in a 90-nm CMOS logic process. In Section II, we describe the design of these photodiodes. Section III reports the measured results from the test chip including the impact of photodiode capacitance on switched-capacitor DC/DC converter transients. Section IV describes an equivalent circuit model fit to the measured results suitable for integration in a conventional IC design flow. Section V discusses the implications of integrating photodiodes with logic for system architecture. Their possible application to shallow-implantable
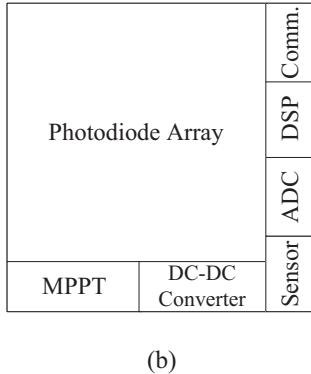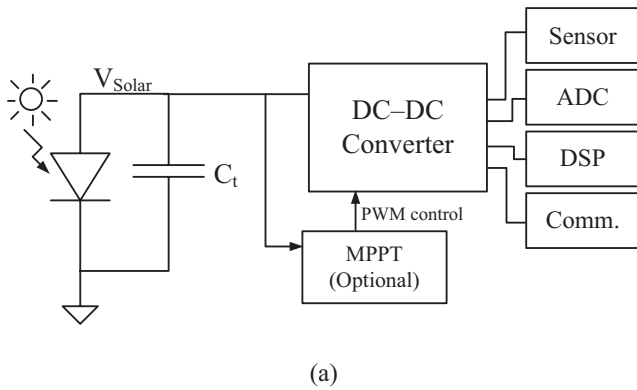
(a)

(b)

Fig. 1. (a) Simplified block diagram of a conceptual PV energy-harvesting system. (b) Conceptual chip architecture of the whole sensor system. A prototype system is currently being developed and will be characterized in future work.
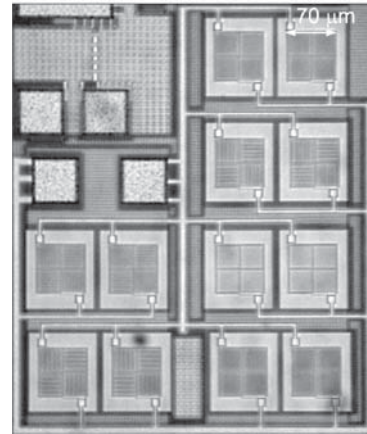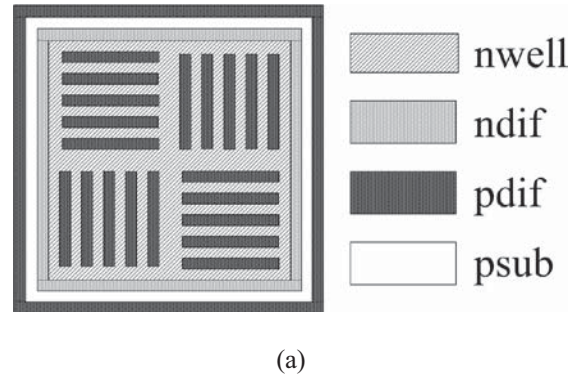

(a)

(b)

Fig. 2. (a) Layout view of 2-D integrated photodiode. Metal diffraction gratings are aligned with the p-diffusions. (b) Die photograph of test chip showing multiple photodiode test structures constructed in the 90-nm CMOS process.

(subdermal) biomedical devices is explored in Section VI. This paper is compared with recent works in Section VII, which also summarizes the conclusion drawn from these results.

II. INTEGRATED PHOTODIODE DESIGN

Fig. 2(a) shows the layout for an integrated photodiode. A 2-D photodiode structure, consisting of p-diffusion fingers implanted in an n-well, was implemented. Vertical parallel plate storage capacitance using metal routing layers can be constructed on top of the fingers, forming an optical diffraction grating [2]. Metal density design rules are becoming stricter as technology continues to scale in modern CMOS processes. Using metal interconnect as storage capacitance can help satisfy these density constraints while providing useful functionality. Since the spacing between these vertical metal strips doubles as the aperture for the incident light, the storage capacitance will have an optical filtering effect. To increase the optical efficiency in order for the photodiode to harvest additional energy from off-axis illumination (large incident angle, ϕ^i) a periodic grating sequence can be implemented by varying the height of the metal fingers. Fig. 2(b) shows a die photo of the fabricated photodiode test structures.

Extensive research has been done on increasing solar cell efficiency by increasing the effective path of mostly longer wavelengths ($\lambda > 600$ nm) through using antireflective coatings, texturing the surface, and incorporating diffraction gratings or reflectors on the backside of the die [27]–[29].

All of these techniques require a specialized solar cell fabrication process. Diffraction can be defined as the bending or spreading of light waves when they interact with an obstacle [30], [31]. Here, since we implement an integrated diffraction grating using the metal interconnects available in a commodity CMOS logic process, the design of the gratings differs in fundamental ways from prior work. First, the grating is placed above the photodiode, in the incoming light path, which means that the grating may block some of the incident photons while guiding others toward the photodiodes. This tradeoff must be carefully considered in the grating design to ensure that the net impact of the grating is an increase in harvested energy. Second, the metal design rules and metal and via thicknesses constrain the dimensions of the grating to be different from what can be achieved in a solar cell-specific process. For example, some of the lateral dimensions of the optimal gratings proposed in [29] can be approximated within the 90-nm CMOS design rules, whereas the vertical dimensions (55–170 nm for the solar cell process, a minimum height of 500–600 nm for the logic process) cannot. Third, in solar cells, gratings are used to scatter light into the silicon and increase the fraction of incident photons which are absorbed. In our case, the goal of the gratings is to increase the power generated from off-axis illumination or from photons scattered by intervening media such as biological tissue. These are
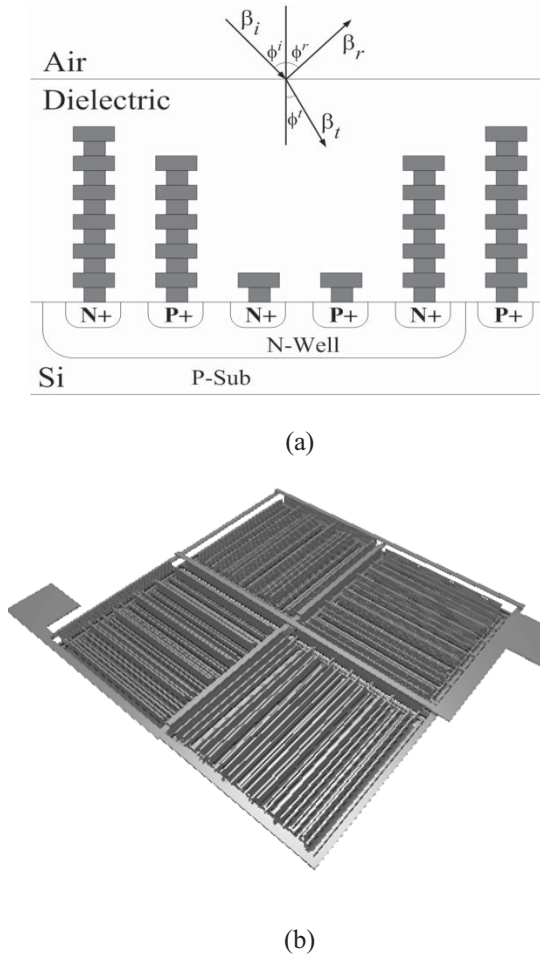
(a)

(b)

Fig. 3. (a) Side view of candidate 1-D photodiode (design D2 from [1]) together with storage capacitance. Metal pattern helps to reduce reflections and guides light to the depletion region. (b) 3-D views of the different metal layers that make up the grating are shown. Each quadrant of the photodiode is rotated 90° from the previous to capture light from all directions.

Fig. 4. Side views of photodiodes' gray metal diffraction gratings show periodicity and heights for various sequences.

not problems for most photo-voltaic applications since it is typically assumed that the angle the solar panel makes with the sun is fixed at an optimum for a particular location.

For medical implants or wireless sensors there is no control over the solar cell's orientation with respect to the illumination source. In these applications, using a grating which increases the scattering of photons into the silicon (rather than concentrating them) would create other problems such as generating lateral photocurrents which might interfere with the operation of adjacent logic circuits.

Our approach to these problems was to adapt diffraction gratings originally designed for acoustic waves. Much of the initial investigation into these types of gratings was done by Schroeder [32], [33]. His goal was to design a surface for enhancing the acoustics in concert halls. Schroeder applied the number theory based on a quadratic residue sequence to determine the geometric periodicity used in the diffraction grating. His original concept was to design a ceiling that would limit the amount of direct reflections heard by the audience. He accomplished this by designing a surface that would limit the amount of reflections into the audience over a wide bandwidth. For audio, the diffraction provided by the periodic grat-
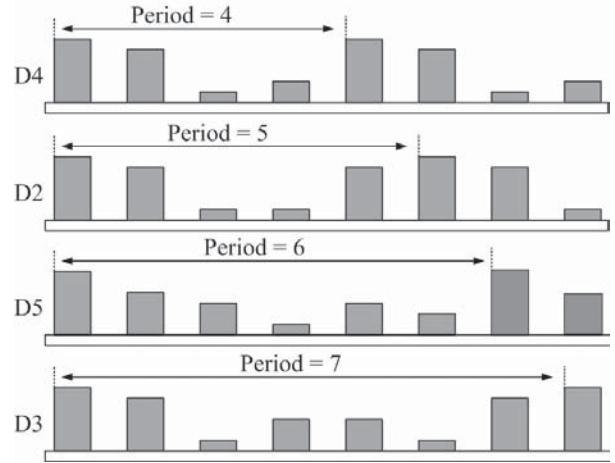
ing reduces the sense of localization for the reflected waves. By reducing the amount of reflected light, the diffraction grating can increase the transmitted energy into the photodiode. Note that this is the opposite goal of the grating design in [29], which was meant to increase the reflection of light into the silicon to improve absorption. Feldman was the first to suggest using a primitive root sequence instead of the quadratic residue sequence for the diffraction gratings [34]. Fig. 3(a) shows the side view of the diffraction structure patterned over the p-sub/n-well energy-harvesting diode with interlaced diffusion fingers similar to the structure D2 from [1]. A 3-D image of a photodiode from this paper can be seen in Fig. 3(b). The gray metal pillars constructed from vias and metal layers reflect and diffract incident light. Section III describes the experimental characterization of these integrated photodiode designs.

III. EXPERIMENTAL RESULTS

In total, six different geometries (D1–D6) for the diffractive storage capacitance were designed and tested. Each diode occupied the same area and had the same diffusion layout in Fig. 2(a), but incorporated a different metal diffraction grating using interconnect layers metal 1 through metal 6 (M1–M6). A goal of this paper is to determine the impact the metal storage capacitance has on the photodiodes' optical efficiency. The first diode D1 is the control, where only M1 was used to connect the p-diffusion fingers together. Diodes D2 and D3 used M1 through M6, and were based on quadratic residue sequence diffusers with periods 5 and 7, respectively. Diodes D4 and D5 also used M1 through M6, but were based on a primitive root sequence with periods 4 and 6, respectively. Diode D6 was also a control, where its diffraction grating occupied all six layers throughout for a maximum metal fill density.

Fig. 4 shows side views of the various diffraction grating sequences [35]. Each diode from D2 to D5 has its own periodicity ranging from four to seven fingers. Gray rectangles indicate metal interconnect. Light passes between the vertical metal plates and then into the substrate, shown as a white rectangle. Table I shows the metal height of the diffraction grating as a function of position for each photodiode. The

TABLE I
DIFFRACTION GRATING SEQUENCE, METAL LAYERS
USED, AND METAL FILL DENSITY

Diode	1	2	3	4	5	6	7	Fill density (%)
D1	1	1	1	1	1	1	1	16
D2	6	5	1	1	5			60
D3	6	5	1	3	3	1	5	57
D4	4	1	5	6				67
D5	4	5	1	3	2	6		53
D6	6	6	6	6	6	6	6	100
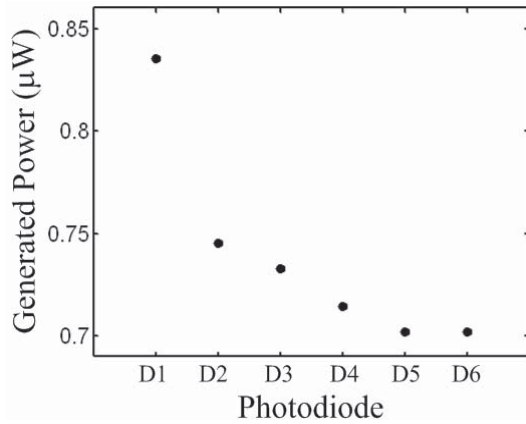
Fig. 5.   Generated electrical power for various photodiodes with an optical illuminance of 5 kLUX.
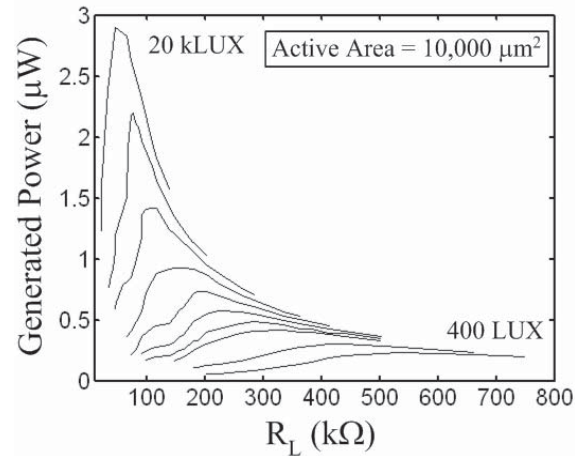

Fig. 6.   Generated electrical power for photodiode D2 (QRD, $p = 5$) for various light intensity levels ranging from 400 to 20 kLUX.
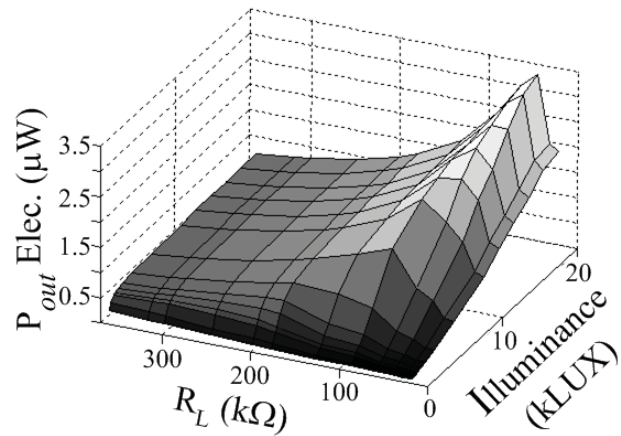

Fig. 7.   Device characterization for photodiode D1 (control). Active area = 10 000 μm^2.

metal fill density is also reported, where 100% corresponds to D6 which has every position filled to M6.

Fig. 5 shows the generated power for each photodiode. Measurements were conducted with incandescent light illumination from a normal tungsten filament of 5 kLUX and an active diode area of 10 000 μm^2 at room temperature. Since each photodiode has the same area and diffusion geometry, the differences between the various photodiodes originate only from optical losses. Each photodiode has an increasing amount of fill density, ranging from the low density of D1 to the maximum density of D6. It can be seen here that there is a direct correlation between metal fill density and optical loss. Therefore, a tradeoff exists between optical efficiency and capacitive energy storage. The duty cycle for the periodicity between the metal width and metal spacing is near 32%. The period for a single aperture–metal pair is approximately 1 μm, and the space between the vertical parallel plates is ∼0.3 μm.

Fig. 6 shows the generated electrical power for photodiode D2, which uses the quadratic residue diffuser (QRD) with period 5, plotted versus load resistance. Each trace is for a different illumination, ranging from 400 LUX to 20 kLUX. It can be seen that the optimal resistance for the photodiode becomes more selective at higher light intensities. MPPT is typically employed to ensure that the photodiode operates near the optimal load condition [36]–[40]. The optimum matching of photodiodes to a fixed resistive load has been previously outlined [36]. Various techniques using switching regulators have also been proposed to tune the photodiode for maximum power generation [37]–[39]. Each of these techniques requires

additional energy overhead to carry out the MPPT algorithm. The curves from Fig. 6 suggest that MPPT could have substantial benefits for the integrated photodiodes, especially at higher power generation. At lower light intensities (<1 kLUX), the energy overhead required for an MPPT algorithm might offset any additional energy-harvesting benefits. A well-designed power management system for solar energy-harvesting would turn on an MPPT algorithm for larger power generation, but then turn it off as illumination decreases. Figs. 7 and 8 show the generated electrical power for photodiodes D1 and D6, respectively. These measurements were taken with a white light source directly on-axis (i.e., normal to the surface of the chip). The characteristic shapes of the power curves are similar since they have identical diffusion patterns. Photodiode D1 generates the most power with on-axis illumination due to a high optical efficiency from a low metal fill density.

Thin metal gratings, similar to the ones discussed here, have previously been used in PV applications as a back reflector, which trap light reflecting off the air to glass interface [28], [41], [42]. When optimized, the diffraction gratings have been shown to increase the efficiency of the photodiode by more than 6.2% [28]. Some rules of thumb have been developed for designing gratings for superior optical performance: the
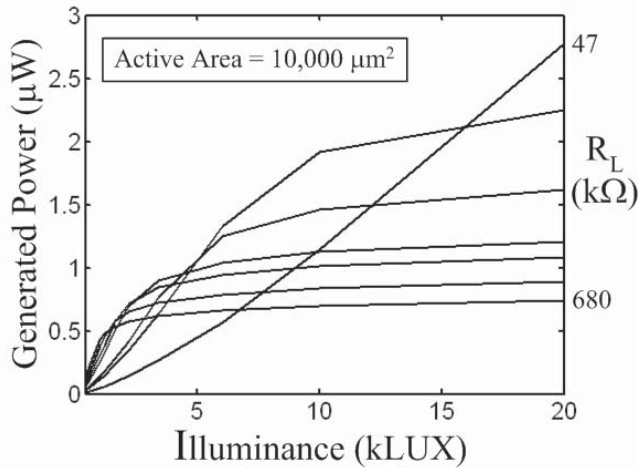
Fig. 8.   Power curves for photodiode D6 (maximum metal fill density). Each trace is for a different load resistance ranging from 47 to 680 kΩ.
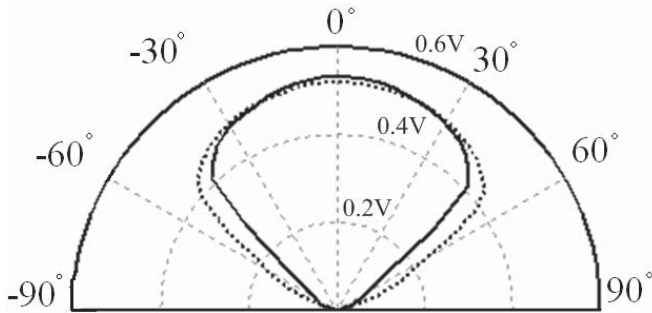

Fig. 9.   Polar plot of open-circuit voltage versus angle of incident light, measuring the photodiodes' off-axis response. Solid line is control D1 (only M1). Dashed line is D4 with periodic diffraction grating (M1–M6). $\lambda = 532$ nm. Peak generated voltage is near 0.5 V.
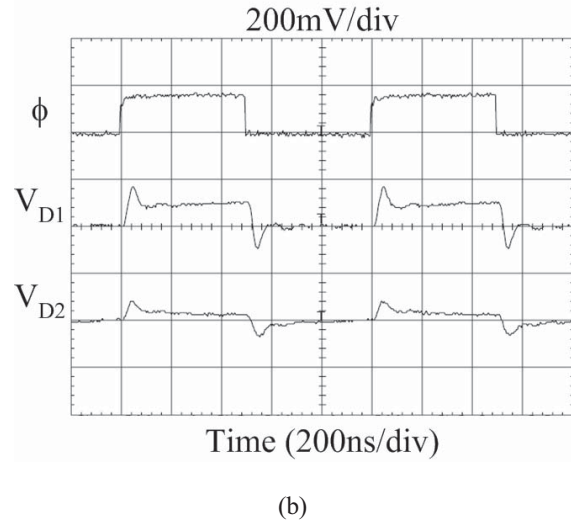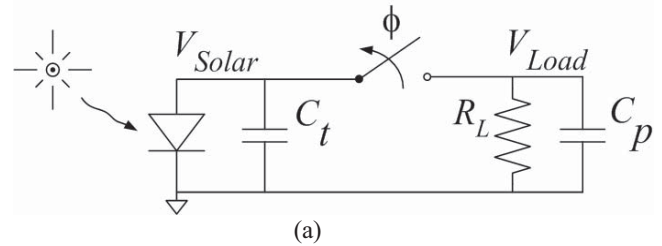

Fig. 10.   (a) Simplified schematic of solar energy-harvesting power supply. A switched RC is used to model a digital load. A larger C_t will function as a filter to smooth current pulses through the switch. (b) Measured waveforms showing clock signal ϕ and V_{solar} voltages for photodiodes D1 and D2. The additional metal capacitance associated with D2 allows for reduced voltage ripple.

grating period should equal $0.7 \times$ the wavelength of light, the optimal grating depth should be $0.18 \times$ the wavelength of light, and, for thicker gratings, a duty cycle near 50% is optimal [42].

Fig. 9 shows the open-circuit voltage of two different photodiodes swept over an incident light angle. These measurements were conducted with a green laser with $\lambda = 532$ nm. When the incident light is normal to the chip surface, the photodiode with the minimal amount of metal capacitance (D1) has the highest generated voltage. There exists an angle, near 45° off-axis, where the photodiode with a diffraction grating (D4) generates the higher voltage. In many scenarios, direct on-axis illumination cannot be guaranteed, therefore, having a photodiode with an improved off-axis response can maximize the harvested energy.

A simplified schematic of the setup testing the transient response of a photodiode is shown in Fig. 10(a). Typically, a switching regulator is used to modulate the current flow from the photodiode to a load. Here the load is modeled as a resistor R_L in parallel with a capacitor C_p. When the clock signal ϕ rises, the switch in Fig. 10(a) closes and charge is shared between the photodiode and the load. This additional loading

will force the photodiode's voltage to decrease, causing a fluctuation in the generated power. This fluctuation on the power supply is highly undesirable for sensitive circuits such as ADCs and may be a limiting factor of resolution or accuracy. A storage capacitance C_t in parallel with the photodiode can be used to mitigate this fluctuation. The additional storage capacitance acts as a filter reducing the voltage ripple caused by the switching.

In Fig. 10(b), the transient response for photodiodes D1 and D2 are compared. For these measurements, an input light intensity of 5 kLUX was used along with $R_L = 100$ kΩ and $C_p = 6$ pF. When ϕ rises, the switch in Fig. 10(a) closes and connects V_{solar} to V_{load}. The additional capacitance associated with D2's metal diffraction grating reduces the transient spike when the switch closes. Photodiode D2 with the additional metal storage capacitance exhibits roughly one half of the peak ripple caused by the switching when compared to photodiode D1, which has no additional metal capacitance, thus there exists a direct tradeoff between optical efficiency and power supply ripple. A minimal diffraction grating provides a good balance between solar energy-harvesting and electrical energy storage.

In order to better understand the effects of technology scaling on integrated photodiodes, experiments were conducted to compare photodiodes implemented in 90-nm and 0.35-μm
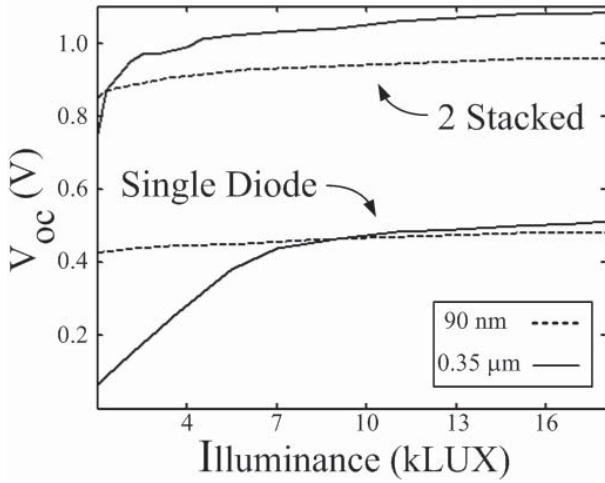
Fig. 11. Open-circuit voltage for a single diode and two diodes stacked in series measured for 90-nm and 0.35-μm CMOS technologies.

	$\lambda = 532$ nm	$\lambda = 633$ nm
P_{max} (μW)	28.8	68.3
Measured η (%)	10	22
Calculated η (%)	27	32

The red laser with $\lambda = 633$ nm has a higher efficiency due to better silicon responsivity at this wavelength. Comparing the photodiodes from this process to the previous design in 0.35 μm, the total efficiency is lower for the newer process due to two contributing factors. The diffraction grating has a higher density with more metal layers used which will block or deflect more photons, and the process may have different n-well and p-diffusion depths, or depletion widths, due to different dopant levels which affect the forward and photogenerated currents.

The theoretical upper bound for efficiency was calculated to be 27 and 32% for the green and red lasers, respectively, using the detailed balance limit. The principle is that the solar cell absorbs long wavelength photons corresponding to the ambient temperature and also emits photons through spontaneous emission resulting in a constant electron concentration at steady state [44]. This limit is based on the temperature of the light source, temperature of the photodiode or solar cell, the band gap, and the likelihood that a photon with energy greater than the band gap will generate an electron–hole pair, and accounts for an ideal case where recombination is only radiative [45]. Especially, in an indirect band gap material, this recombination has little effect on the efficiency and is a function of the bias voltage, here it decreased efficiency by 1%. Discrepancies between the calculated and measured efficiencies are due to the optical grating causing a decrease in optical efficiency as well as resistances within the cell which are assumed to be ideal. Likewise, the discrepancy between the ratios of efficiencies for both lasers may be due to the optical grating as well.

CMOS logic processes. The increased dopant concentrations used in the newer technology resulted in a smaller open-circuit voltage (the dark current density J_0 was measured to be 204 pA/cm^2) when compared to the older technology, for equivalent input illuminance. However, the overall power generation and fill factor were higher for the more advanced 90-nm process. Fig. 11 plots the open-circuit voltages measured for the two technologies versus input illuminance. Data for a single photodiode and two energy-harvesting photodiodes connected in series are shown. It can be seen here that the 90-nm technology has a more consistent open-circuit voltage over a wider range of input illuminance conditions. The fill factor (defined as the ratio of diode output power at a particular load condition to the product of the diode's open-circuit voltage and short-circuit current), is a common figure of merit used in characterizing PV technologies. The photodiode prototypes in this paper have an average fill factor of 0.8.

The total efficiency of photodiode D2 was measured with the same green and red lasers used previously. The total efficiency is the combination of the optical efficiency determined by the diffraction grating and the quantum efficiency determined by the semiconductor properties and its ability to generate electron–hole pairs. To remove the contribution of lateral photocurrent to the output power, a differential measurement was performed by measuring the total power from two photodiodes in parallel, ablating one photodiode, repeating the measurement, and taking the difference between the two. The total optical power in from the laser was measured by the solid-state power meter assuming the top-hat approximation [43]. Since the laser beam is Gaussian shaped, and the diameter of the beam is much larger than the photodiodes, we can use the top-hat approximation to model the laser beam with a uniform intensity and a diameter of $\sqrt{2}\omega$, ω being the radius where the power transmitted is $\approx 86\%$ or the intensity is $1/e^2$ of the peak intensity [43]. The uniform intensity can then be integrated over the area of the photodiode, 70×70 μm. Dividing the generated electrical power by the optical power in, the efficiency is 10 and 22% for the green and red lasers, respectively, as shown in Table II.

IV. PHOTODIODE MODELING

An equivalent circuit model for an idealized PV cell consists of a current source in parallel with an ideal diode. The PV cell is irradiated by solar energy which generates free carriers (and current) and is represented by the current source. To model the nonlinear $I-V$ characteristics of a PV cell, diode D_1 is introduced. The current in the PV cell is constant under the assumption that the irradiance and temperature are constant.

However, this simple model is insufficient in practice because it neglects the nonidealities of fabricated PV cells. Fig. 12 shows a more accurate model of the PV cell with the ideal current source replaced by a voltage-controlled current source (VCCS) and the addition of a second diode, series resistor, and shunt resistor [46]. V_{source} models the solar energy incident on the surface of the photodiode, that is, the irradiance (W/m^2). The VCCS I_L is the product of g_{irrad} and V_{source}, where g_{irrad} is a function of the short-circuit current density given at standard conditions (normalized by 1000 W/m^2 at $T = 25$ °C). The resistor r_{series} accounts for the current flow
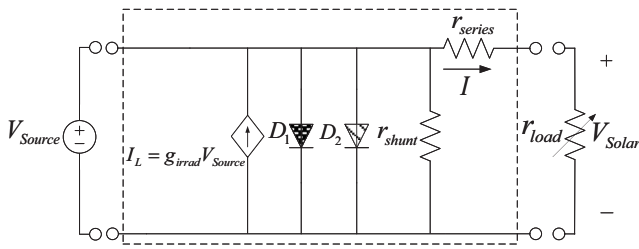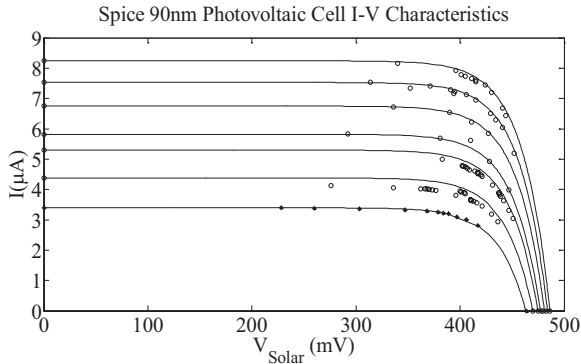
Fig. 12. Generalized PV circuit model.

Fig. 13. Comparison of the modeled $I-V$ curves and measured points of the actual photodiode at different light intensities.

TABLE III
SPICE SIMULATION VERSUS EXPERIMENTAL RESULTS

| $r_{series} \to 0$ $r_{shunt} \to \infty$ | Experimental results 90-nm photodiodes | | | |
| | Simulation | | Measurements | |
Irradiance (kLUX)	I_{sc} (μA)	V_{oc} (mV)	I_{sc} (μA)	V_{oc} (mV)
20	8.24	486	8.24	486
17.5	7.53	483	7.53	483
15	6.75	481	6.75	480
12.5	5.82	477	5.82	478
10	5.30	475	5.30	475
7.5	4.38	470	4.38	470
5	3.40	463	3.40	464

integrated on the same die have many implications and design challenges for the overall system architecture. Several of these are discussed below.

A. PV Array Configuration

One advantage of integrating photodiodes is that arrays of individual cells can be combined in a wide variety of configurations depending on the voltage and current requirements of the load circuits. Subthreshold circuits can operate with an array of several photodiodes connected in parallel. Higher voltages can be achieved by stacking diodes in series (as shown for two diodes in Fig. 11), however, the number of diodes which can be stacked can be limited by the available options for electrical isolation (see below). The stacking also reduces the peak currents which can be generated in exchange for increasing the peak voltage.

B. Isolation

The choice of junctions used to implement the photodiodes can influence the harvested energy and the interaction of the integrated solar cells with adjacent logic. If one would like to utilize the diodes formed between the p-substrate and the n-well, the generated short-circuit current will be four times as great, but further isolation is needed from the rest of the circuits to reduce the interference from lateral photocurrents [8]. Possible layout options utilizing common isolation techniques such as local oxidation of silicon, silicon-on-insulator, shallow trench isolation, deep trench isolation, twin-tub, guard rings, and substrate etching can be considered. The efficacy and compatibility of these techniques with commodity CMOS processes needs further investigation, including their impact on circuit density. Ultimately, the same isolation techniques which are used in CMOS imagers can be applied to integrated solar energy-harvesting systems, however at increased process cost. The impact of high-speed logic circuits on the photodiodes is expected to be minimal because of: 1) supply regulation provided by the integrated DC/DC converter [Fig. 1(a)] and 2) substrate noise isolated by the same structures which limit lateral photocurrents.

C. Mismatch and Noise

Unlike an imaging application, mismatch between the photodiodes themselves is not a problem in this application

through the semiconductor material, interconnect, contacts, and current-collecting bus for a single PV cell. Subsequently, for n series connected PV cells the total value is the product of n and r_{series}. A small increase in r_{series} can lead to a substantial degradation in PV efficiency. Additionally, a parallel resistor r_{shunt} accounts for leakage current pathways parallel to the PV cell due to nonideal semiconductor characteristics. In general, the leakage current is small and the overall effect of r_{shunt} on PV efficiency is insignificant compared to r_{series}. Recombination of carriers in the space-charge region of the PV cell gives rise to the second diode D_2. This results in an additional nonohmic current pathway in parallel with the PV cell [46].

An accurate SPICE model for a practical implementation of 90-nm CMOS-integrated photodiodes has been developed. Diode D_1 in Fig. 12 is replaced by the foundry's 90-nm diode model (p+/n-well, n-well/p-sub). The pertinent model parameters of the generalized circuit model were fit to the measured $I-V$ characteristics of the fabricated 90-nm photodiodes as seen in Fig. 13. Table III summarizes the SPICE simulation results using the 90-nm diode model. A purely resistive external load is varied for several increasing irradiance values to obtain two parameters of interest: the short-circuit current (I_{sc}) and the open-circuit voltage (V_{oc}). Simulation and measurement results for the integrated photodiodes indicate good agreement between the model and the physical device. The small deviation is the result of inherent environmental variations (temperature) and irregularities in irradiance during the experimental measurements.

V. SYSTEM ARCHITECTURE IMPLICATIONS

The design and optimization of the interface (both physical and electrical) between the photodiodes and load circuits

Source	λ (nm)	Method to obtain coefficients	Maximum depth beneath surface tissue to obtain 5 μW (mm)	
			1 cm^2	(0.1 cm)^2
Marchesini 1989	635	Beer's law	6	2.4
van Gemert, 1986 (Epidermis)	540	K–M	1.6	0.79
van Gemert, 1986	540	K–M	2.4	1.0
Anderson, 1981	630	K–M	3.7	1.6
Wan, 1981 (breast and abdominal)	630	K–M	1.9	1.0

since we are only concerned with generating power and not recovering an optical signal with high fidelity. Similarly, photodiode noise such as shot noise does not affect our application directly, but indirectly through the power supply. At low light intensities, shot noise becomes more significant and this may affect sensitive analog circuits with limited power supply rejection ratios.

VI. IMPLANTABLE BIOMEDICAL DEVICE APPLICATIONS

Decreasing the volume of implantable biomedical devices is highly desirable to improve patient comfort (implants can shift and erode through the skin) and decrease the immune response to a foreign object inside the body [47]. Implantable biomedical devices as well as low-power wireless sensor nodes have been demonstrated to function with power consumption in the microwatt range [1], [48], [49]. With the current energy density limits of the lithium-ion battery, a device with 5-μW average power consumption over a 10-year period would require a volume of at least 1 cm^3 [50]. Batteries typically occupy 25 to 60% of the entire device volume [51]. Harvesting energy from vibrations and thermal gradients has been studied extensively for supplying power to help reduce battery volume [48], [49]. However, temperature differences within the body are too small to yield significant power. Integrated photodiodes would require an area of less than 10 000 μm^2 compared to 30.2-mm^3 volume required for vibration energy harvesters to power a simple 16-bit digital finite-impulse response filter operating at 1 MHz [52]. Inductive coupling has been demonstrated with off-chip inductors made of coiled wire with diameters around 5.5–22 mm at low frequencies [53]–[55], operating at a higher frequency would result in smaller devices, but adverse effects with attenuation and heating tissue within the body can arise at frequencies above 1 MHz [53].

Despite their promise to improve device miniaturization, PVs placed under the skin or in the body have yet to be considered for these applications, most likely due to the complicated absorption and scattering that occurs through the different heterogeneous tissue layers that greatly reduce the incident light intensity. At the same time, this attenuation is highly dependent on wavelength. In this paper, 532- and 633-nm high-power lasers were used to illuminate the

photodiodes. Measuring the photodiode output power allows us to more accurately calculate the transmission through certain thicknesses of tissue. Previous works have studied the transmission of collimated lasers at similar wavelengths and reported attenuation and scattering coefficients for a variety of tissues and wavelengths [56]. Two well-known models have been used: Beer's law and Kubelka–Munk (K–M) theory. Beer's law is based on the exponential attenuation due to μ_t, the total attenuation coefficient or the sum of the absorption and scattering coefficients. The percentage of light intensity T transmitted through the tissue of thickness t is

$$T = e^{-\mu_t t}. \tag{1}$$

Neglecting reflections at boundaries, the K–M theory is based on the propagation of a uniform diffuse radiance through a uniform medium, and the percentage of transmission is

$$T = \frac{y}{x \cosh(S_{KM}yt) + y \sinh(S_{KM}yt)} \tag{2}$$

with S_{KM} as the K–M scattering coefficient (m^{-1}), $x = A_{KM}/S_{KM} + 1$, $y = +\sqrt{x^2 + 1}$, and A_{KM} as the K–M absorption coefficient (m^{-1}). Because lasers are collimated and anisotropic, the K–M theory is just an approximation of laser and tissue interaction [56]. Taking these known attenuation and scattering coefficients, the maximum depth beneath the surface of different types of tissue was calculated in order to obtain at least 5-μW output power.

Using high-power lasers, the maximum intensity limit must be known in order to prevent thermal and other adverse effects in tissues. It has been established that tissues can be irradiated by a laser within the visible spectrum for up to 8 h at 0.2 W/cm^2 without undesirable effects [57]. This corresponds to measured powers of 2 and 1.6 mW for the green and red lasers used, respectively. The laser power was measured with a solid-state power meter, and the diameters of the beams were measured using the knife-edge method [58]. At these intensities, the corresponding maximum photodiode output powers are 4.3 and 10.4 μW, assuming an active area of 10 000 μm^2. Since irradiance is expressed in watts per square meter, both the power of the laser and the output power of the photodiodes can be used in the transmission equations above. Assuming a low duty cycle and minimum power budget of 5 μW [1] for the sensor allows us to determine the maximum implantable depth. The implant depth is associated with the thickness t and can be found using the maximum allowable intensity, the power generation density of the photodiode (W/cm^2), and the fixed amount of area allocated for the photodiodes. The green laser requires a maximum attenuation of −39 dB for a 1 × 1 cm photodiode and −19 dB or 1.2% transmission for a photodiode with size 0.1 × 0.1 cm. The red laser ideally should have at most −43 and −23-dB attenuation through the tissue with the same larger and smaller sized photodiodes, respectively. The red laser implant depth is greater because it penetrates the skin more due to its longer wavelength [59].

Table IV shows the calculated depths at which the photodiodes can be placed beneath the various tissue types to harvest 5 μW with photodiodes of areas 1 and 0.01 cm^2 using

TABLE V
COMPARISON OF RECENT WORKS

Parameter	[18]	[17]	[12]	[11]	[1]	This paper
CMOS process	0.35 μm	0.35 μm	0.5 μm	0.35 μm	0.35 μm	90 nm
Incident light intensity	6.37 mW/cm^2 (555 nm)	1–10 kLUX ($\sim$5–50 mW/cm^2)	1–60 kLUX ($\sim$5–300 mW/cm^2)	30 mW/cm^2	20 kLUX ($\sim$100 mW/cm^2)	20 kLUX ($\sim$100 mW/cm^2)
V_{oc} (V)	0.84 (2 stages) 1.3 (3 stages)	0.6–0.83 (2 photodiodes in series)	0.4–0.450	0.480	0.533	0.486
I_{sc} density (mm^{-2})	315 nA* 35 nA*	500 nA–4.2 μA*	-	778 μA*	680 μA	824 μA
Power generated (mm^{-2})	194 nW* 37.3 nW*	164–870 nW*	840 nW – 2.8 μW*	250 μW*	225 μW	325 μW
η (%)	0.3 0.06	2.6	9	17	17 (532 nm)	10 (532 nm) 22 (633 nm)

*Numbers approximated from plots and/or adjusted by given areas.

the radiative transport equation and the calculated coefficients. A photodiode with area 1 cm^2 can be placed at the maximum depth of 6 mm in dermis using the coefficients and a laser with wavelength $\lambda = 635$ nm. Skin thickness not only varies between individuals and with the site of the implant but can also change with age and environmental factors [60], [61]. The skin, made up of the dermis and epidermis layers, typically is 1.5 mm, with the subcutaneous layer, mainly made up of fat, beneath [61], [62]. Therefore, a multilayer model would be more realistic.

An iterative method was used to determine the number of photons or light energy per unit area per time (also known as the fluence rate) that would reach the photodiode by simulating the probable paths that hundreds of thousands of photons will most likely follow. Such rates can be determined using the Monte Carlo method in MATLAB and the probability of scattering and absorption events while calculating directional angles in an iterative process until the photon is either emitted from the tissue or, as in our case, reaches the photodiode [63]. Monte Carlo simulations give a more realistic model and a larger depth beneath the surface of the skin because Beer's law only accounts for the ballistic photons (the photons that travel through the sample without being attenuated or scattered). On the other hand, the Monte Carlo simulations take into account the photons that scatter multiple times but still reach the photodiode. However, the Monte Carlo simulations take longer to perform.

Having control over the light source which supplies power to the implantable device allows the user to have control over the device's performance as well. The light source can be used continuously up to 8 h at a time depending on the optical output power [57], used occasionally to recharge an energy store (taking up more area on the IC or volume in the device), or used only during high power consumption tasks such as communication. The device must be designed to operate at a lower duty cycle and lower performance when the power is insufficient to support full operation. This can be achieved with multiple modes of operation, dynamic frequency and voltage scaling, or any other well-known techniques [12]. On the other hand, one can evaluate the feasibility of periodic optical

recharging to support full operation by considering a specific example. The commercially available neural stimulator in [64] has a volume of 18 cm^3 and has a recharge interval of 121 days in a low-power (estimated average power 300–750 μW) full operation mode. Assuming a battery energy density of 200 mAh/cm^3 [65] and typical battery volumes, the device stores at minimum 3200 J. To accumulate the same amount of energy over the 121-day recharge period would require illuminating an integrated photodiode array 2.7 cm on a side at 630-nm wavelength for 2 h per day (device volume 0.04 cm^3, thickness $\sim$50 μm to store harvested energy for 24 h), when implanted up to 1.6-mm deep. These results indicate that dramatic reductions in volume may someday be enabled by implanted energy-harvesting photodiodes.

VII. CONCLUSION

This paper has been compared to recent works in Table V. Similar to [1], Ferri *et al.* measured analogous parameters such as efficiency; however, at a lower light intensity, and therefore lower and possibly scaled V_{oc} and I_{sc}. They also point out that connecting the p-substrate to the p-diffusions, like in this paper, allows the beneficial use of the parasitic diode formed between the substrate and the n-well, but does not allow for integration with the active circuitry [8]. By measuring both the p-diffusion/n-well and the p-sub/n-well photodiodes separately, it is concluded that the photogenerated current, or I_{sc}, is four times smaller for the floating p-diffusion/n-well photodiode than the two in parallel. Ay utilized the p+/n-well photodiode to harvest energy while shorting the p-sub/n-well photodiode, both of which make up an active pixel sensor of a 54 $\times$ 50 array [9]. Similar systems of energy-harvesting image sensors have been proposed [10]–[12].

Others have come up with interesting solutions to this integration problem. Plesz *et al.* created a model that allows the percentage of current generated by the parasitic diode of the total current to be varied, as well as β of the resulting bipolar junction transistor [13]. This can be realized by implementing a buried $n+$ layer below the n-well to repulse the minority carriers with the electric field it creates, and can

TABLE VI
MEASURED PERFORMANCE (25 °C, 10 000 μm^2)

Parameters	D1	D2	D4	D6
Power generated (μW)	1.32	1.30	1.26	1.20
Energy stored (pJ)	0.86	1.43	1.55	1.98
Capacitance C_t (pF)	7.52	12.74	13.57	17.47
V_{oc} (mV)	479	473	478	477
I_{sc} (μA)	5.96	5.76	5.63	5.43

be enhanced with an $n+$ ring around the p-diffusions. From their simulations, they saw an increase of 58% in I_{sc} with a slight increase in V_{oc} when the parasitic diode contributes only 2%. They were also able to put three photodiodes in series.

Arima and Ehara utilized two photodiodes in series, one formed with the p+/n-well and the other with the p-sub/n+, integrated with a 7-bit counter and a full adder [14]. They demonstrate that the operating frequency scales up with the light intensity incident on the photodiodes. On the other hand, it is unclear how the p-sub/n+ photodiode is isolated from the other circuitry. Law and Bermak compensated for the parasitic photodiode by implementing up to eight photodiodes in parallel in the previous stage(s), and therefore have low efficiencies [15].

Charge pumps were also used with MPPT to generate sufficient voltages for the technology node used [40]. Ciftcioglu *et al.* present a new photodiode structure that has a deep n-well in the p-epi-layer below the p-well that is isolated by n-well on both sides, thus creating two vertical p-n junctions [16]. The upper photodiode is a hybrid vertical and lateral p-i-n that gives a quantum efficiency of 20% at $\lambda = 855$ nm and is used for on-chip optical communication.

In this paper, we outlined both optical and electrical design considerations for integrated energy-harvesting photodiodes. By using a diffraction grating whose period was based on number theory, metal storage capacitors were integrated with the photodiodes while causing minimal optical losses. A tradeoff between optical efficiency and transient response was realized with a moderately dense metal capacitance constructed on top of the photodiode. By using a numerical pattern for the metal capacitance such as a quadratic residue sequence, an increase in off-axis photodiode response can be obtained, at the expense of a slightly diminished on-axis response. Table VI summarizes the measured results for a few select photodiodes. These measurements were conducted with an input light intensity of 10 kLUX. At 20 kLUX, the output power for diode D1 was 325 μW/mm^2, a 44% increase over [1]. Photodiode D2 appeared to have the best overall performance, showing a good balance between power generation, storage, and transient response. This paper leaves room for investigating the effect of noise, such as the effect shot noise might have on the power supply voltage and the power supply rejection ratio of analog circuits.

Tissue optics was considered in a subdermal solar energy-harvesting application to power biomedical devices.

A photodiode with an area of 1 cm^2 was placed 3.7–6 mm under the surface of dermis tissue to meet a 5-μW power budget when illuminated by a laser with $\lambda = 633$ nm. The power budget of course depended on the irradiance of the light source and the duty cycle of the circuit. The measured efficiency of the photodiode matched well with the calculations for the red laser. The photodiode exhibited a 22% efficiency with the red laser which corresponded to the 32% duty cycle of the optical grading and the 37% efficiency determined by the detailed balance limit. The discrepancy between efficiencies given by the detailed balance limit matched well to silicon's responsivity at the respective wavelengths. The discrepancy with the green laser measured efficiency might be due to the optical grating. Finally, an equivalent circuit model was presented that accurately reproduced the measured $I-V$ curves.

REFERENCES

[1] N. J. Guilar, A. Chen, T. Kleeburg, and R. Amirtharajah, "Integrated solar energy harvesting and storage," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design*, 2006, pp. 20–24.

[2] N. J. Guilar, E. G. Fong, T. Kleeburg, D. R. Yankelevich, and R. Amirtharahah, "Energy harvesting photodiodes with integrated 2-D diffractive storage capacitance," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design*, Aug. 2008, pp. 63–68.

[3] I. Fujimori, C. Wang, and C. Sodini, "A 256 × 256 CMOS differential passive pixel imager with FPN reduction techniques," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 2031–2037, Dec. 2000.

[4] A. Kansal and M. Srivastava, "An environmental energy harvesting framework for sensor networks," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design*, Aug. 2003, pp. 481–486.

[5] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems," in *Proc. Int. Symp. Inform. Process. Sens. Netw.*, Apr. 2005, pp. 457–462

[6] X. Jiang, J. Polastre, and D. Culler, "Perpetual environmentally powered sensor networks," in *Proc. 4th Int. Symp. Inform. Process. Sens. Netw.*, Apr. 2005, pp. 463–468.

[7] F. Simjee and P. H. Chou, "Everlast: Long-life, supercapacitor-operated wireless sensor node," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design*, Oct. 2006, pp. 197–202.

[8] M. Ferri, D. Pinna, E. Dallago, and P. Malcovati, "Integrated micro-solar cell structures for harvesting supplied microsystems in 0.35-μm CMOS technology," in *Proc. IEEE Sens. Conf.*, Oct. 2009, pp. 542–545.

[9] S. U. Ay, "A 1.32 pW/frame·pixel 1.2 V CMOS energy-harvesting and imaging (EHI) APS imager," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2011, pp. 116–117.

[10] A. Fish, S. Hamami, and O. Yadid-Pecht, "Self-powered active sensors for ultralow power applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 5310–5313.

[11] C. Shi, M. K. Law, and A. Berkmak, "A novel asynchronous pixel for an energy harvesting CMOS image sensor," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 1, pp. 118–129, Jan. 2011.

[12] M. K. Law, A. Bermak, and C. Shi, "A low-power energy-harvesting logarithmic CMOS image sensor with reconfigurable resolution using two level quantization scheme," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 2, pp. 80–84, Feb. 2011.

[13] B. Plesz, L. Juhász, and J. Mizsei, "Feasibility study of a CMOS-compatible integrated solar photovoltaic cell array," in *Proc. Symp. Design Test Integ. Packag. MEMS/MOEMS*, May 2010, pp. 403–406.

[14] Y. Arima and M. Ehara, "On-chip solar battery structure for CMOS LSI," *IEICE Electron. Exp.*, vol. 3, no. 13, pp. 287–291, 2006.

[15] M. K. Law and A. Bermak, "High-voltage generation with stacked photodiodes in standard CMOS process," *IEEE Electron. Device Lett.*, vol. 31, no. 12, pp. 1425–1427, Dec. 2010.

[16] B. Ciftcioglu, L. Zhang, J. Zhang, J. R. Marciante, J. Zuegel, R. Sobolewski, and H. Wu, "Integrated silicon PIN photodiodes using deep n-well in a standard 0.18-μm CMOS technology," *J. Lightw. Technol.*, vol. 27, no. 15, pp. 3303–3313, Aug. 2009.

[17] R. Amirtharajah, J. Wenck, J. Collier, J. Siebert, and B. Zhou, "Circuits for energy harvesting sensor signal processing," in *Proc. ACM/IEEE Design Autom. Conf.*, San Francisco, CA, 2006, pp. 639–644.

[18] A. Kansal, J. Hsu, M. Srivastava, and V. Raghunathan, "Harvesting aware power management for sensor networks," in *Proc. ACM/IEEE Design Autom. Conf.*, San Francisco, CA, 2006, pp. 651–656.

[19] V. Raghunathan and P. H. Chou, "Design and power management of energy harvesting embedded systems," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design*, Oct. 2006, pp. 369–374.

[20] J. Hsu, S. Zahedi, A. Kansal, M. Srivastava, and V. Raghunathan, "Adaptive duty cycling for energy harvesting systems," in *Proc. ACM/IEEE Int. Symp. Low Power Electron. Design*, Oct. 2006, pp. 180–185.

[21] P. Stanley-Marbell and D. Marculescu, "An 0.9 × 1.2 low power, energy-harvesting system with custom multi-channel communication interface," in *Proc. Design Autom. Test Eur. Conf.*, Apr. 2007, pp. 1–6.

[22] J. Elmes, V. Gaydarzhiev, A. Mensah, K. Rustom, J. Shen, and I. Batarseh, "Maximum energy harvesting control for oscillating energy harvesting systems," in *Proc. IEEE Power Electron. Special. Conf.*, Jun. 2007, pp. 2792–2798.

[23] H. Shao, C.-Y. Tsui, and W.-H. Ki, "An inductor-less micro solar power management system design for energy harvesting applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2007, pp. 1353–1356.

[24] J. S. Lee, R. I. Hornsey, and D. Renshaw, "Analysis of CMOS photodiodes-part I: Quantum efficiency," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1239–1245, May 2003.

[25] J. S. Lee, R. I. Hornsey, and D. Renshaw, "Analysis of CMOS photodiodes-part II: Lateral photoresponse," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1239–1245, May 2003.

[26] P. B. Catrysse and B. A. Wandell, "Optical efficiency of image sensor pixels," *J. Opt. Soc. Amer.*, vol. 19, no. 8, pp. 1610–1620, Aug. 2002.

[27] M. Peters, M. Rüdiger, H. Hermle, and B. Blaesi, "Photonic crystals in solar cells a simulation approach," *Proc. SPIE*, vol. 7725, pp. 772514-1-772514-10, Apr. 2010.

[28] N.-N. Feng, J. Michel, L. Zeng, J. Liu, C.-Y. Hong, L. C. Kimerling, and X. Duan, "Design of highly efficient light-trapping structures for thin-film crystalline silicon solar cells," *IEEE Trans. Electron. Devices*, vol. 54, no. 8, pp. 1926–1933, Aug. 2007.

[29] C. Heine and R. H. Morf, "Submicrometer gratings for solar energy applications," *Appl. Opt.*, vol. 34, no. 14, pp. 2476–24782, 1995.

[30] P. Beckmann and A. Spizzichino, *The Scattering of Electromagnetic Waves from Rough Surfaces*. New York: Pergamon, 1963.

[31] E. G. Loewen and E. Popov, *Diffraction Gratings and Applications*. New York: Marcel Dekker, 1997.

[32] M. R. Schroeder, "Diffuse sound reflection by maximum-length sequence," *J. Acoust. Soc. Amer.*, vol. 57, no. 1, pp. 149–150, 1979.

[33] M. R. Schroeder, "Binaural dissimilarity and optimum ceilings for concert halls: More lateral sound diffusion," *J. Acoust. Soc. Amer.*, vol. 65, no. 4, pp. 958–963, 1975.

[34] E. Feldman, "A reflection grating that nullifies the specular reflection: A cone of silence," *J. Acoust. Soc. Amer.*, vol. 98, no. 623, pp. 623–634, 1995.

[35] G. Ballou, *Handbook for Sound Engineers: New Audio Cyclopedia*. Focal Press, 1998.

[36] K. Y. Khouzam, "Optimum load matching in direct-coupled photovoltaic power systems-application to resistive loads," *IEEE Trans. Energy Convers.*, vol. 5, no. 2, pp. 265–271, Jun. 1990.

[37] C. R. Sullivan and M. J. Powers, "A high-efficiency maximum power point tracker for photovoltaic arrays in a solar-powered race vehicle," in *Proc. IEEE Power Electron. Special. Conf.*, Jun. 1993, pp. 574–580.

[38] C. Hua and C. Shen, "Study of maximum power tracking techniques and control of DC/DC converters for photovoltaic power system," in *Proc. IEEE Power Electron. Special. Conf.*, Fukuoka, Japan, May 1998, pp. 86–93.

[39] K. K. Tse, M. T. Ho, H. S.-H. Chung, and S. Y. Hui, "A novel maximum power point tracker for PV panels using switching frequency modulation," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 980–989, Nov. 2002.

[40] E. Méndez-Delgado, G. Serrano, and E. I. Ortiz-Rivera, "Monolithic integrated solar energy harvesting system," in *Proc. IEEE 35th Photovoltaic Special. Conf.*, Honolulu, HI, Jun. 2010, pp. 1–8.

[41] C. Heine and R. H. Morf, "Submicrometer gratings for solar energy applications," *Appl. Opt.*, vol. 34, no. 14, pp. 2476–2482, May 1995.

[42] C. Eisele, C. E. Nebel, and M. Stutzmann, "Periodic light coupler gratings in amorphous thin film solar cells," *J. Appl. Phys.*, vol. 89, no. 12, pp. 7722–7726, Jun. 2001.

[43] A. E. Siegman, *Lasers*. Mill Valley, CA: Univ. Science Books, 1989.

[44] J. Nelson, *The Physics of Solar Cells*. London, U.K.: Imperial College, 2003.

[45] W. Shockley and H. J. Queisser, "Detailed balance limit of efficiency of p-n junction solar cells," *J. Appl. Phys.*, vol. 32, no. 3, pp. 510–519, Mar. 1961.

[46] L. Castaner and S. Silvestre, *Modelling Photovoltaic Systems Using Pspice*. New York: Wiley, 2002.

[47] S. Upson, "Tiny implants combat chronic pain," *IEEE Spectr.*, vol. 45, no. 12, p. 18, Dec. 2008.

[48] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow power electronics for biomedical applications," *Annu. Rev. Biomed. Eng.*, vol. 10, pp. 247–74, Aug. 2008.

[49] B.-S. Lee, P.-J. Shih, J.-J. He, W.-P. Shih, and W.-J. Wu, "A study of implantable harvesting transducers," *Proc. SPIE*, vol. 6530, pp. 653001-1–653001-8, Mar. 2007.

[50] M. Nathan, "Microbattery technologies for miniaturized implantable medical devices," *Current Pharmaceutical Biotehnol.*, vol. 11, no. 4, pp. 404–410, 2010.

[51] C. Schmidt and P. Skarstad, "The future of lithium and lithium-ion batteries in implantable medical devices," *J. Power Source*, vols. 97–98, pp. 742–746, Jul. 2001.

[52] R. Amirtharajah, J. Wenck, and N. Guilar, "Energy harvesting and limits of low power mixed-signal circuit design," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 1425–1428.

[53] A. K. RamRakhyani, S. Mirabbasi, and M. Chiao, "Design and optimization of resonance-based efficient wireless power delivery systems for biomedical implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 48–63, Feb. 2011.

[54] F. Zhang, X. L. Hackworth, S. A. Sclabassi, and R. J. M. Sun, "In vitro and in vivo studies on wireless powering of medical sensors and implantable devices," in *Proc. Life Sci. Syst. Appl. Workshop*, Bethesda, MD, Apr. 2009, pp. 84–87.

[55] S. Kim, R. R. Harrison, and F. Solzbacher, "Influence of system integration and packaging on its inductive power link for an integrated wireless neural interface," *IEEE Trans. Biomed. Eng.*, vol. 56, no. 12, pp. 2927–2936, Dec. 2009.

[56] W.-F. Cheong, S. A. Prahl, and A. J. Welch, "A review of the optical properties of biological tissues," *IEEE J. Quantum Electron.*, vol. 26, no. 12, pp. 2166–2185, Dec. 1990.

[57] R. L. Harris, *Patty's Industrial Hygiene*, 5th ed. New York: Wiley, 2000.

[58] O. Solgaard, *Photonic Microsystems*. New York: Springer-Verlag, 2009.

[59] R. R. Anderson and J. A. Parrish, "The optics of human skin," *J. Invest. Dermatol.*, vol. 77, no. 1, pp. 13–19, 1981.

[60] L. K. Smalls, R. R. Wickett, and M. O. Visscher, "Effect of dermal thickness, tissue composition, and body site on skin biomechanical properties," *Skin Res. Technol.*, vol. 12, no. 1, pp. 43–49, 2006.

[61] S. Shuster, M. M. Black, and E. McVitite, "The influence of age and sex on skin thickness, skin collagen and density," *British J. Dermatol.*, vol. 93, no. 6, pp. 639–643, Dec. 1975.

[62] S. E. Whitmore and J. G. Sago, "Caliper-measured skin thickness is similar in white and black women," *J. Amer. Academy Dermatol.*, vol. 42, no. 1, pp. 76–79, Jan. 2000.

[63] S. A. Prahl, M. Keijzer, S. L. Jacques, and A. J. Welch, "A Monte Carlo model of light propagation in tissue," *Proc. SPIE Dosimetry Laser Radiat. Med. Biol.*, vol. IS5, pp. 102–111, 1989.

[64] *St. Jude Medical, Eon Mini Rechargeable IPG Competitive Data Sheet* [Online]. Available: http://www.sjmneuropro.com/Products/US/Eon-Mini-Rechargeable-IPG-System.aspx

[65] O. Soykan, "Power sources for implantable medical devices," in *Proc. Business Briefing: Med. Device Manufact. Technol.*, 2002, pp. 76–79.

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