Energy Harvesting and Limits of Low Power Mixed-Signal Circuit Design

Rajeevan Amirtharajah, Justin Wenck
ECE Dept., Univ. of California, Davis
Davis, CA
ramirtha@ece.ucdavis.edu, jawenck@ucdavis.edu

Nathaniel Guilar
Agilent Technologies
Santa Clara, CA
njguilar@ece.ucdavis.edu

***Abstract*—Wireless sensors and implantable medical devices have driven IC design to extremes of low power consumption to maximize system operating lifetimes from fixed energy stores or from energy harvested from the environment. Reaching the limits of miniaturization will require approaching the limits of power dissipation. We describe three key sensor subsystems: integrated diodes for solar energy harvesting, efficient microwatt power conversion circuits, and supply-voltage-ripple-tolerant digital circuits. We then extrapolate from these examples to find the minimum surface area and volume required for energy harvesting sensors.**

I. Introduction

Fifteen years ago, Vittoz presented a remarkably prescient paper on low-power design [1]. He predicted much of the direction of research in low-power electronics that has occurred in the last decade and a half, including dynamic voltage and frequency scaling, aggressive power-down and clock gating of idle subsystems, on-die voltage conversion and power management, renewed interest in ultra-low-V_{DD} and subthreshold circuit design, dynamic biasing of analog circuits, and substrate biasing to minimize leakage currents in low-V_{th} and mixed-threshold designs. He described certain limits to low power design for both digital and analog circuits based on theoretical considerations. In particular, he determined the minimum power to implement an analog pole $P_{Amin} = 8fkT(\frac{S}{N})$, where f is the signal frequency bandwidth, T is absolute temperature, k is Boltzmann's constant, and $\frac{S}{N}$ is the required signal-to-noise ratio. Similar considerations for digital circuits set the minimum power supply voltage near $8kT/q = 200$mV, where q is the electron charge. For a digital system, the minimum energy for a bit transition is $E_{Dmin} = 8kT$. Thus, for a digital circuit with a supply voltage of 0.2V, the corresponding capacitance for $E_{Dmin} = CV_{DD}^2$ at the theoretical minimum is 0.83aF. The inverter input capacitance for a cutting-edge 45nm CMOS process [2] is estimated to be 258aF. There is clearly room for further progress in transistor miniaturization.

Energy harvesting systems offer an interesting context to explore the implications of the theoretical limits mentioned above. For example, the limits determine the minimum volume requirements for a system that powers itself, since both vibration energy harvesting and solar energy harvesting scale poorly as volume shrinks [3]. An energy harvesting system can have potentially unlimited operating lifetime while occupying a finite volume, so it presents an interesting limit study on how small an electronic system can be made. Wireless sensor nodes, which combine sensing and actuation, analog and digital processing, and RF communication, typically require low performance from each of their components and therefore can be made very low power with aggressive application of the techniques listed above. Figure 1 shows an energy harvesting and power delivery system which creates multiple power supplies from multiple energy sources (vibration and solar) and delivers them to the heterogeneous loads in a sensor platform [4]. A detailed discussion of every block in Figure 1 is beyond the scope of this paper. Therefore, in the remaining sections we will focus on design examples of three of the subsystems shown in Figure 1: the solar energy harvesting transducer (photodiode), the power management circuits, and a highly supply-voltage-ripple-tolerant low power digital processor. The combined power characteristics of these modules will set a lower bound on the volume of an energy harvesting system, which we estimate in Section V.

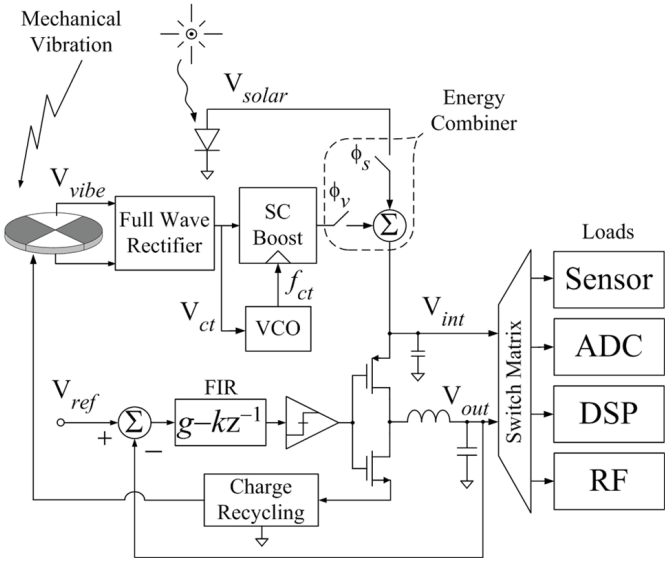

Fig. 1. Multiple modality energy harvesting system for a wireless sensor.

II. Integrated Solar Energy Harvesting

Integration has been a driving force in reducing cost and system power consumption in electronics for decades. Because the average power of circuits for sensor applications can be made very low due to low duty cycle and aggressive application of clock gating, power-down modes, and leakage reduction, it is possible to devote a fraction of die area to energy harvesting - thus integrating the power source into the chip itself. The simplest way to do this is to use CMOS passive pixels (similar to imager pixels) as photovoltaic cells to harvest solar energy [5], [6]. The metal interconnect layers on the chip can be exploited as capacitance to store the harvested energy, although at low energy density compared to off-chip ultracapacitors. Because on-chip wiring can be fabricated at

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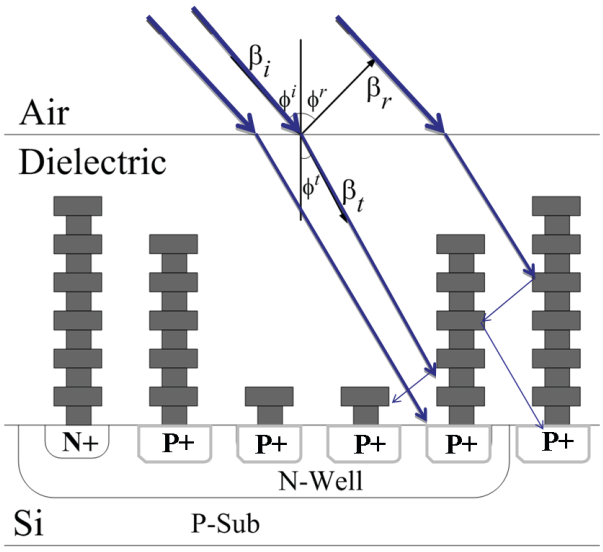

Fig. 2. Diffraction around metal fingers.

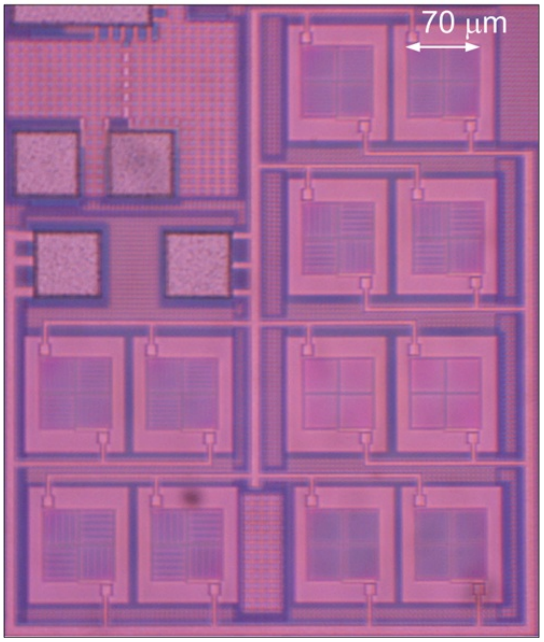

Fig. 3. Integrated solar energy harvesting photodiodes test chip.

pitches comparable to the wavelength of light, it is further possible to use metal on-chip interconnect as diffractive optics to improve solar energy harvesting with integrated photodiodes. Figure 2 illustrates the concept. Incident photons encounter the dielectric at the top of the chip and are guided to the depletion regions in the substrate by metal fingers implemented using stacks of interconnect and vias. The fingers provide the on-chip storage capacitance for the harvested energy. By varying the heights of the fingers, an optical diffuser is created which can harvest energy from a wider range of incident light angles than if all the fingers had the same height, at the expense of a decrease in the energy storage density. Figure 3 shows a test chip fabricated to explore this idea using a number of test structures with different diffuser patterns. The optimal diffuser increases the range of incident angles which could generate 200mV from 0°-45° to 0°-60° [6]. For 20kLux incident light intensity, photodiodes in 0.35μm digital CMOS and 90nm digital CMOS have been shown to deliver output power of 225μW/mm^2 and 325μW/mm^2, respectively. For comparison, vibration energy scavenging can generate power densities from 0.4-80nW/mm^3 depending on the vibration frequency and amplitude [3].

III. Power Electronics

Energy harvesting systems that rely on a diverse set of energy sources require a highly flexible power supply to deal with large variation in environmental conditions. This section describes an integrated power management system for use with multiple energy harvesters, which employs energy awareness and charge recycling. Multiple energy harvesters (e.g., a multi-phase piezoelectric disk for vibration harvesting [7] and integrated photovoltaic cells for solar energy shown in Figure 1) present opportunities for energy combining using switched capacitor networks. Piezoelectrics produce high AC voltages and low output currents while photovoltaics produce low DC voltages. Switched capacitors can filter and down-convert the piezoelectric output and combine it in parallel with the photovoltaic output to increase current to the load, or can combine outputs in series to boost the load voltage. This flexibility can optimize power conversion based on load characteristics: high power/high voltage/low ripple supplies are required by RF transmitters while digital circuits tolerate low power/low voltage/high ripple supplies. The main design considerations for these circuits are the size of the capacitors and switches. The capacitors must be large enough to deliver big enough charge packets to supply the load. The switch sizing must balance the conduction loss through the series switch resistance with the dynamic power of charging and discharging the gate. Sizes can be adjusted dynamically by using multiple parallel FETs to implement each switch, thus allowing wider switches to be used only under high loads [8].

Multiple regulation approaches which trade efficiency for output voltage quality are enabled by combining switching converters and linear regulators with fully digital or mixed-signal feedback control. Regulator loops can be closed around voltage for analog circuits, or performance (critical path delay) for digital circuits. In Figure 1, the rectified and filtered output of the piezoelectric disk transducer provides the input voltage V_{int} to a switching DC/DC (buck) converter. V_{int} can also be used directly by any load which can tolerate its characteristics. The output of the switching converter V_{out} is determined by sliding-mode control using a single comparator. The FIR filter $g-kz^{-1}$ can be adjusted to control the switching frequency of the converter, increasing the frequency (and the corresponding power consumption) when low output ripple is required and decreasing the frequency to produce a high output ripple but at high efficiency. The filter is implemented using a time-interleaved passive switched-capacitor network, trading off degraded noise performance (lower SNR) and increased offset for low power consumption by eliminating opamps [4].

Harvesting transducers can also serve as energy storage. The charge recycling block in Figure 1 recovers charge from

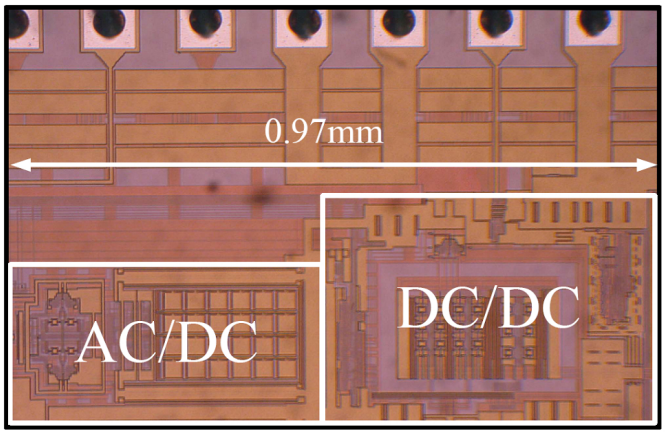

Fig. 4. Integrated circuit realization AC/DC and DC/DC converters from Figure 1.

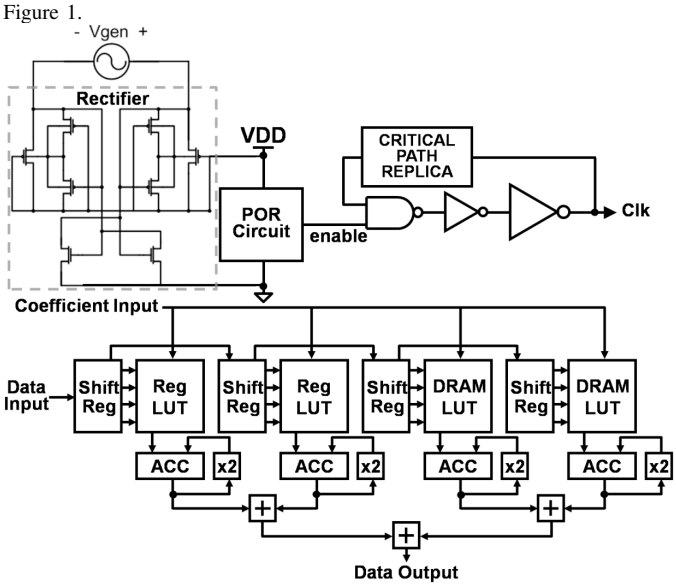

Fig. 5. AC power supply test chip block diagram.

highly capacitive circuit nodes (e.g., the buck converter output), and stores it in the piezoelectric disk. The recovered energy is stored mechanically to be used again, improving overall system efficiency. Energy recovery techniques can help reduce power consumption below the $CV_{DD}^2 f$ limit, but their overhead must be minimized to obtain a net benefit. These techniques can be implemented using switched capacitors with the same design considerations described above. Figure 4 shows a chip realization in 0.25μm CMOS of the AC/DC and DC/DC converters proposed in Figure 1. The AC/DC and DC/DC converters have maximum power efficiencies of 84.1% and 74.5% when the controllers consume 13.5μW and 16μW, respectively. Charge recycling reduces power by approximately 10%. These values are comparable to the 78% peak efficiency of the DC/DC converter in [8].

IV. Digital Circuits and Microarchitecture

One approach to avoiding the efficiency penalty of AC/DC conversion described above is to recognize that the period of the AC supply waveform is long compared to the clock frequencies demanded even in sensor applications (typical

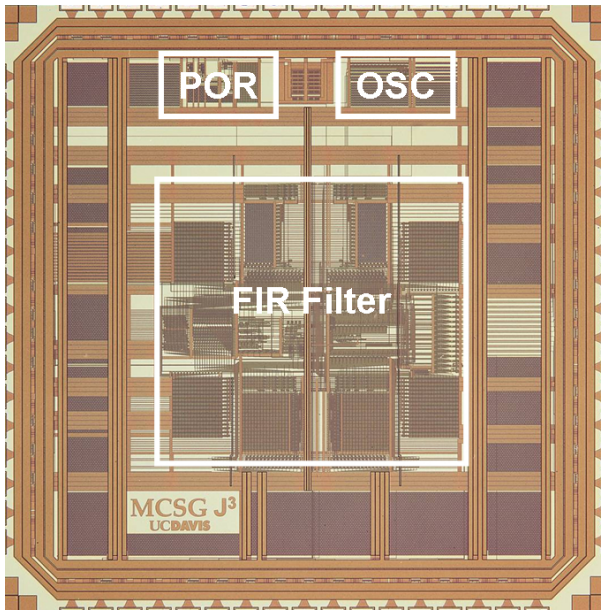

Fig. 6. AC power supply test chip die photo.

vibration-based energy harvesters produce outputs between 60Hz and 1kHz), consequently a digital circuit with good tolerance to wide supply variations can use the AC supply directly if initialization and memory can be handled correctly. Figure 5 shows the block diagram of a test chip developed to explore circuit design for energy harvesting AC power supplies [9]. The chip combines a novel power-on-reset (POR) circuit, self-timed circuit design, and dynamic memory to implement an energy-scalable programmable digital FIR filter based on Distributed Arithmetic [10]. Self-timing is accomplished using a ring oscillator based on a replica of the critical path of the digital filter. It also integrates a static CMOS full-wave rectifier [11]. The rectifier filter capacitance due to parasitics and on-chip bypass is too small to smooth low frequency AC ripple to DC. The POR initializes the state elements with a fast time constant to maximize operation time. The dynamic memory is based on a 3T cell with non-destructive reads [12]. The storage node capacitance is chosen to maintain state between power supply cycles (on the order of several ms) at the limiting voltage and temperature corner. Distributed Arithmetic is used, rather than the conventional multiply-accumulate (MAC) architecture, because it has been shown to offer lower total power consumption when leakage dominates at low clock frequencies for filters with large numbers of taps [13]. Because Distributed Arithmetic is based on storing precomputed results in lookup-tables, all of the techniques for low power memory design can be exploited to reduce its power consumption. In addition, since it relies on serial shifting of the input sample bits, the filter computation can be made *energy scalable*, i.e. the accuracy of the final result can be traded off linearly for reduced power consumption by shifting in fewer bits.

A die photo of the test chip, implemented in 0.18μm CMOS, is shown in Figure 6. The chip was verified over input supply frequencies from 60Hz to 1kHz with a peak self-timed

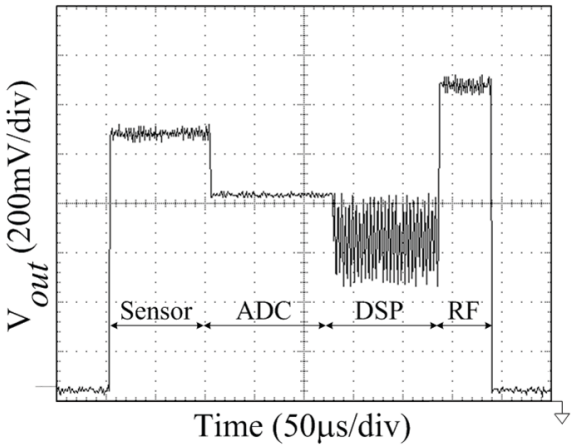

Fig. 7. Measured power supply waveforms with emulated loads.

clock frequency of 75.6MHz at peak $V_{DD} = 1.8$V. Power consumption varies between 127μW and 113μW with supply frequency. Higher power occurs at low frequency since the circuit is active for a higher proportion of the cycle period. Computing a 16 bit 4-tap filter result consumes 2.68nJ. Scaling the energy to a 200mV V_{DD} and 65nm CMOS, results in an energy/bit of 151fJ. For comparison, completing an instruction consumes a scaled energy/bit of 272fJ in [8] and 71fJ in [14].

V. Conclusion

Figure 7 shows the measured output voltage from the power converter chip of Figure 4 with each load emulated by a variable resistor. Each load has a different requirement based on voltage and ripple or noise, with the digital load able to tolerate the lowest supply voltage and lowest quality supply. Therefore we will use the digital energy/bit from Section IV, the power conversion efficiencies from Section III, and the 90nm CMOS integrated solar power generation from Section II, to estimate the minimum surface area and volume of an energy harvesting sensor system. Assuming we want to compute 16 bit results at 1MHz using the microarchitecture of [9], and 76.3% DC/DC conversion efficiency, the system would require 9763 μm^2 of solar diode area. Using vibration energy scavenging, assuming the maximum energy density, and 100% efficiency with an AC supply-tolerant digital circuit, the system would require 30.2mm^3. For comparison, a human red blood cell has a surface area of 150μm^2 and a volume of 115μm^3. Using the $8kT$ digital switching energy limit, assuming 100 switching events per bit, and the same 16 bit results at 1MHz, yields a required solar diode area of 0.21μm^2 and a volume of 7.88×10^{-4}mm^3, including the nonideal AC/DC switching efficiency. This limit corresponds to a power consumption of 53pW. This power level is comparable to the 22pW ideal limit of a passive analog filter with 10kHz bandwidth and SNR equivalent to 16 bit dynamic range, such as one might use as an antialiasing filter at the ADC input of a wireless sensor node. Clearly, we still have many orders of magnitude remaining to scale digital power consumption.

By following the principles of low power mixed-signal design such as simple circuit forms (e.g., passive switched-capacitor analog filters), high density microarchitectures which minimize signal routing capacitance and leakage (e.g., Distributed Arithmetic), self-timed circuits, and energy recovery, designers can continue to push the limits of low power design to create ever smaller and increasingly sophisticated energy harvesting systems. Implementing microbe-sized systems requires approaching the minimum switching energy of $8kT$.

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