Switched-Capacitor Boost Converter Design and Modeling for Indoor Optical Energy Harvesting with Integrated Photodiodes

Stanley W. Hsu, Erin Fong, Vipul Jain, Travis Kleeburg, and Rajeevan Amirtharajah
Micropower Circuits and System Group, Department of Electrical and Computer Engineering
University of California, Davis
Davis, CA 95616
Email: swhsu@ucdavis.edu

***Abstract*—Integrated photovoltaic energy harvesting from indoor lighting is appropriate for ultra-low duty cycle applications. Indoor illumination may flicker due to AC mains rectification or pulse-width-modulated dimming, causing ripple on the output voltage. Switched-capacitor DC/DC conversion can increase harvester output voltage and reduce this ripple. We present a switched-capacitor boost converter design, a model that matches measured output voltage within 10% for 500 Hz to 5 MHz switching frequencies, and compare the converter to a series photodiode configuration. The distortion caused by supply ripple on a passive filter delta-sigma modulator is modeled and verified with measurements from a 180nm test chip.**

***Keywords*—Switched capacitor circuits, Delta-sigma modulation, Photodiodes, Energy harvesting, Analog-digital integrated circuits, wireless sensor networks**

I. Introduction

Wireless and implantable sensors that harvest energy from indoor ambient lighting using discrete solar cells [1] and integrated photodiodes [2], [3] have been proposed. Some systems [3] simply use the photodiode output voltage as the supply rail while others use a switched-capacitor boost converter (SCBC) to regulate the photodiode output [4].

Consider an integrated temperature sensor that harvests indoor ambient lighting for power. Assuming constant illumination and no energy storage/regulation circuits, the required photodiode area is determined by the peak load power and the minimum supply voltage. In such a configuration a flickering light source, e.g. an LED light fixture with pulse-width modulated (PWM) for dimming control [5], causes the photodiode output to become modulated, which translates directly into supply voltage ripple. If multiple photodiodes (PD) are configured to meet the system requirements, and assuming a bypass capacitor C_b is used to smooth the output, the ripple $V_r = V_{max} - V_{min}$ can be derived as

$$V_r = V_{PD}\left(1 - e^{\frac{-(1-D)T_f}{R_{PD}C_b}}\right) \quad (1)$$

, where D and T_f are the flicker duty cycle and period respectively, $V_{PD} = V_{max}$ is the PD output voltage under constant illumination, and assuming the PD output resistance R_{PD} dominates the load resistance R_L. For 50% duty cycle, flicker frequency of 120 Hz, and $R_{PD} = 700$ kΩ, C_b needs to be 56.5 nF to limit supply ripple to 10% of V_{PD}, requiring an off-chip capacitance that increases system cost and volume.

Trade-offs between supply voltage ripple, area, and design complexity are inherent in optically powered integrated systems [6]. Stacking photodiodes to increase the supply voltage requires a multi-well process and increases the system's absolute power supply rejection requirement (due to direct coupling of supply ripple). If an integrated SCBC is used to create the supply voltage from a single photodiode, the converter must be carefully designed such that system requirements are met while operating from a flickering optical source.

In this work, a boost converter model that accounts for various losses while predicting the output voltage is developed. The model performance is verified using simulation and measured results from a 180nm test chip. Additionally, effects of supply ripple on sensitive circuits such as a passive delta-sigma modulator are analyzed and compared to measured results. Understanding the interaction between modulated illumination, switched-capacitor boost conversion, and supply ripple effects on load circuits is critical to minimizing the photodiode bypass capacitance C_b, cost, and volume.

The remainder of the paper is organized as follows: Section II discusses the integrated photodiode design and presents the switched-capacitor boost converter circuit design and model. Section III presents the delta-sigma modulator and discusses the effects of supply ripple and technology selection for low leakage. Section IV presents measurement and simulation results and Section V concludes the paper.

II. Integrated Photovoltaic Power Supply

The on-chip energy harvesting power supply consists of an array of integrated photodiodes followed by a switched-capacitor charge pump voltage converter.

A. Photodiode Design

Two types of integrated solar cells were fabricated. The first photodiodes are fabricated using p-diffusion fingers implanted in n-well [2], [3]. The second design is shown in Fig. 1 and uses a deep n-well (DNW) to capture incident photons before they are absorbed in the substrate. In this design, the efficiency is expected to decrease due to the increase in the distance between p+ diffusion and n-well, causing more carriers to

be recombined. Stacking solar cells in series makes the open circuit voltage scale linearly. However, integrating multiple cells in series on chip presents a challenge if the parasitic diode formed between the substrate and n-well is utilized. This junction generates up to four times as much photocurrent than p+/n-well photodiodes. Likewise when the substrate is utilized, the lateral photogenerated current can negatively affect the adjacent active circuitry. These issues can be circumvented with the use of SOI, which increases cost.

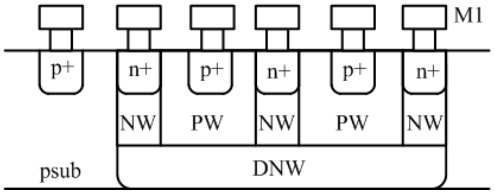


Fig. 1. Cross section of the deep n-well photodiode.

B. Switched-Capacitor Boost Converter Model

Fig. 2 shows a one to four (1:4) SCBC schematic. The circuit operates by first charging flying capacitors C_{ST} in parallel to V_{in} during clock phase ϕ_2. During the next clock phase ϕ_1, the capacitors are placed in series, with V_{in} at the bottom of the first capacitor to achieve a boosted output of $4V_{in}$. However, due to various loss mechanisms that will be discussed and modeled later, the actual output is usually $< 4V_{in}$. NMOS switches at the top of each flying capacitor increase isolation between the boosted internal nodes and the input terminal when low-swing clocks are used. PMOS switches or full transmission gates may be used in other circumstances. In an optically powered system, the boost converter can be started up inefficiently by first using an inaccurate clock generator such as a free-running ring oscillator powered directly from a single photodiode, then switching to a more precise clock source once the boost converter output reaches steady-state.

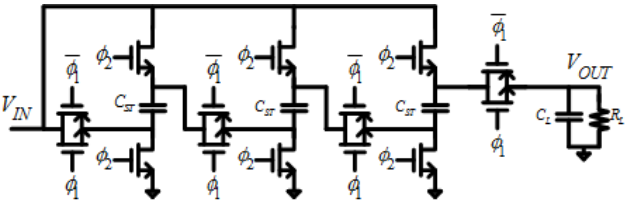


Fig. 2. 1:4 switched-capacitor boost converter schematic (C_{ST} =126pF, C_L =383pF and R_L = 10MΩ).

The SCBC can be modeled using an ideal transformer and an output impedance $R_o(f_{sw})$ dependant on switching frequency f_{sw}, as shown in Fig. 3 [7].

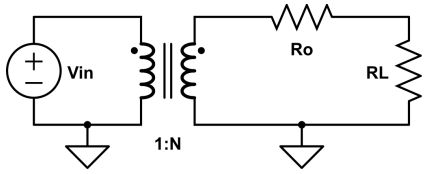


Fig. 3. Simplified model of switched-capacitor boost converter.

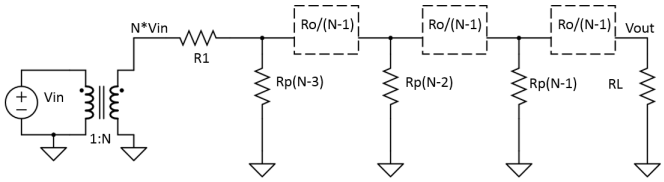


Fig. 4. Proposed cascaded model of the 1:4 ($N = 4$) SCBC includes shunt loss R_p due to flying capacitor bottom plate parasitic capacitance.

$R_o(f_{sw})$ models losses at the slow switching limit (R_{SSL}) and fast switching limit (R_{FSL}) using Equations 2 and 3 [8].

$$R_{SSL} = \frac{\sum_i (a_{c,i})^2}{(C_i f_{sw})} \tag{2}$$

$$R_{FSL} = 2 \sum_i R_i (a_{r,i})^2 \tag{3}$$

R_{SSL} is the loss due to flying capacitor $C_i = C_{ST}$ charging and discharging and R_{FSL} is the loss due to the finite on-resistance of the switches R_i. $a_{c,i}$ and $a_{r,i}$ are charge multiplier vectors that represent the charge flow through each flying capacitor in R_{SSL}, and switches in R_{FSL}, respectively [8]. The transition from the slow to fast switching limit occurs when the settling time of the flying capacitors becomes comparable to the switching period. The total R_o can be estimated by adding R_{SSL} and R_{FSL} in quadrature, $R_o = \sqrt{R_{SSL}^2 + R_{FSL}^2}$ [7].

Previous work [7] mentions, but does not model the the bottom plate parasitic capacitance C_p of the flying capacitors, and does not provide a method to directly compute the converter output voltage. Furthermore, the simple model cannot be applied to converters with boost ratio greater than 2 due to the different loss magnitudes at each cascaded stage. A distributed cascaded model shown in Fig. 4 correctly accounts for the shunt losses due to C_p at each stage and allows the output voltage to be easily calculated. The model has $N - 1$ stages for an 1:N boost converter and the shunt loss at each stage is modeled by $R_p(k)$, $1 \leq k \leq N - 1$. As shown in Fig. 4, the loss due to the bottom plate parasitic is different for each stage since the voltage across the parasitic capacitance is different at each stage. R_1 is added in the model to account for both the effective switch resistance associated with the first stage bottom plate capacitance and the output resistance of the input source V_{in}. $R_p(k)$ can be calculated using Equation 4, where k is the stage number and P_C is the dynamic power dissipated in the parasitic capacitances C_p:

$$R_p(k) = \frac{V_{out}^2}{P_C} = \frac{V_{out}^2}{f_{sw} C_p (kV_{in})^2} \tag{4}$$

In the proposed model, the shunt loss due to the bottom plate parasitic capacitance C_p, and series loss of flying capacitors and switch resistances are the only losses considered. Loss mechanisms at even higher frequencies (where C_p is effectively a short) are not modeled here.

III. Delta-Sigma Modulator

A low voltage and ultra-low power delta-sigma modulator (DSM) can be implemented by replacing the active integrator with a passive switched-capacitor low pass filter (LPF) [9], [10] as shown in Fig. 5. The comparator does not utilize

a pre-amplifier and is a purely dynamic circuit, therefore it does not reject power supply noise in the conventional sense. The only static current in the DSM is due to leakage. The sampling frequency of the integrator can be adjusted to scale the dynamic power consumption, enabling a power-resolution tradeoff. A DSM-based ADC was selected here instead of a successive approximation register (SAR) ADC since the DSM does not require a capacitive DAC, resulting in a small layout area, which frees more area for implementing energy harvesting photodiodes.

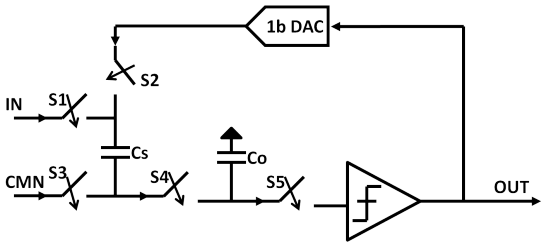


Fig. 5. Passive integrator delta-sigma modulator block diagram. Single-ended channel shown and clock phases omitted for clarity.

A. Ripple Analysis

Flourescent lighting may suffer from flicker due to rectifying the AC power line input voltage. This flicker is converted by integrated photodiodes into power supply ripple at 120 Hz.

Supply ripple degrades the signal to noise and distortion ratio (SNDR) by introducing in-band distortion through three mechanisms. First, because the switched-capacitor LPF clocks are rail-to-rail digital signals, their amplitude is modulated at the supply ripple frequency. Consequently the LPF acts as a passive mixer between the input and the power supply and the effective conversion gain G is $2/\pi$ [11] for clocks with 50% duty cycle. The gain rolls off with increasing clock frequency. Equation 5 shows the conversion gain as a function of duty cycle, D, and harmonic order, n, for odd n.

$$G = \frac{\sin n\pi D}{n\pi D} \tag{5}$$

The distortion due to the passive mixer action primarily results from three sources: the ripple itself, intermodulation (IM) between the ripple and the input signal, and IM between the frequency components within the ripple. Assuming the ripple resembles a square wave, the distortion tones due to the ripple on the supply voltage V_{DD} can be computed using Fourier series,

$$V_{DD}(t) = V_{DC} + \frac{V_{PP}}{2}\sum_{k=1}^{\infty} A_k \sin\left((2k-1)2\pi f_r t\right) \tag{6}$$

$$V_{clk}(t) = V_{DD}(t)\left(\frac{1}{2} + \frac{1}{2}\sum_{j=1}^{\infty} A_j \sin\left((2j-1)2\pi f_s t\right)\right) \tag{7}$$

, where V_{PP} is the peak-to-peak ripple voltage, f_s is the DSM clock frequency, f_r is the ripple frequency, $A_k = \frac{4}{(2k-1)\pi}$, and $A_j = \frac{4}{(2j-1)\pi}$. Assuming the DSM input is $V_{in}(t) = V_{CM} + A_{in}\sin(2\pi f_{in} t)$, where V_{CM} is the average (common-mode) input voltage, and the clock signal is $V_{clk}(t)$ as shown in Equation 7 above, the output of the passive LPF will contain IM distortion tones at $(2k-1)f_r$ with amplitude proportional to A_k due to mixing between the supply ripple (transferred through the sampling clock) and the average input signal. This distortion depends strongly on the ripple's shape and frequency; the more sinusoidal the ripple, the lower the distortion since higher order harmonics are less significant. Additionally, if the ripple frequency is large enough such that the higher order components fall outside of the bandwidth, SNDR degradation can be minimized.

The second source of distortion is second order IM (IM2) between the ripple and the input. This IM2 distortion occurs due to the switch S1 in Fig. 5 in the LPF that samples the input. The ripple is present at the switch control terminal while the input frequency is present at the switch input terminal. IM2 causes frequency tones at the sum and difference between the signal frequency and each of the frequency components in the supply ripple to appear. In general, the tones are at $f_{in} \pm (2k-1)f_r$. The magnitude of these IM2 tones is proportional to $GA_{in}\frac{V_{PP}}{(2k-1)\pi}$.

The third source of distortion is IM2 between the frequency components of the ripple itself. This IM2 is injected into the LPF through the 1 bit feedback DAC. The DAC output is added into the LPF through sampling switch S2 in Fig. 5. Here, the ripple is once again present at the switch control terminal, but the switch input terminal is now connected to the supply voltage, which contains the same ripple. Let $f_1 = f_r, f_2 = 3f_r, f_3 = 5f_r, ...$ and $f_k = (2k-1)f_r$, the IM2 tones appear at $f_2 \pm f_1, f_3 \pm f_2, ...$ and $f_k \pm f_{k-1}$, where $k = 2, 3, ...$ Since all distortion tones are proportional to V_{PP} in amplitude, minimizing ripple to maintain adequate SNDR is critically important.

B. Technology Selection

The 180nm technology is suitable for optical energy harvesting systems due to its low leakage characteristics. Leakage current is not only important in large digital circuits, but also in ultra-low duty cycle, data-rate, and low voltage/power applications; leakage causes state information stored as charge to leak away during the long idle time, introducing errors into the system. Switched-capacitor circuits that operate on charge sharing principles are especially sensitive to leakage. High leakage technology results in leaky capacitors and low off-resistance of MOS transistors, resulting in poor analog switch isolation and charge retention.

For a sample and hold circuit that consists of a MOS switch connected to a capacitor C and assuming the average (common-mode) input is V_{CM}, the voltage during the hold mode is $V_{hold} = V_{CM}e^{(\frac{-T_S}{2R_{off}C})}$, where R_{off} is the off resistance of the switch and $\frac{T_S}{2}$ is the hold duration. We define the error due to leakage as $\epsilon_{lk} = \frac{V_{hold}}{V_{CM}} = e^{(\frac{-T_S}{2R_{off}C})}$. If we further define an off-to-on resistance ratio $K = \frac{R_{off}}{R_{on}}$, let $K = 10000$ for 180nm technology, $K = 1000$ for 90nm technology, $T_S = 20\mu$s (50 kHz sampling rate), $R_{on} = 5\text{k}\Omega$, and $C = 10$ pF, the average voltage across C suffers from 1.9% droop at 180nm and 18% droop at 90nm due to leakage. The drooping due to leakage becomes important in circuits operating from low supply voltages and at low sampling

rates, such as the passive filter-based DSM in this work. The technology appropriate for ultra-low duty cycle applications must have low leakage characteristics to minimize error.

IV. Results

A test chip, shown in Fig. 6, containing the photodiodes, boost converter, and the delta-sigma modulator was fabricated in 180nm CMOS to prototype the system and to verify the boost converter model.

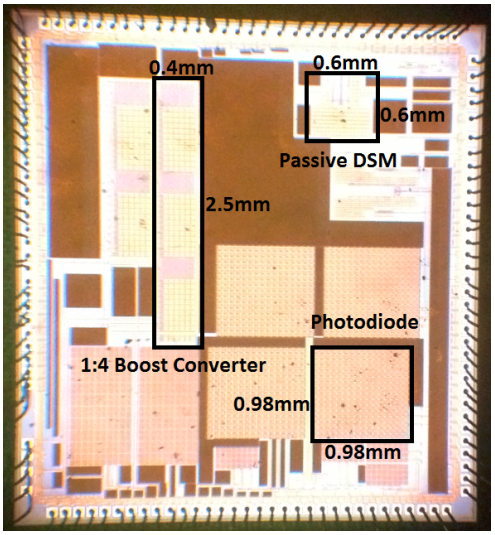


Fig. 6. Die photo of the 180nm test chip with parts labeled.

A. Integrated Photodiodes

Under 400 Lux of white LED illumination, the open circuit voltage and short circuit current produced by the integrated photodiodes are approximately 0.41V and 1.5 μA, respectively. The measured open circuit voltage ranges from 0.45-0.52V under LED and incandescent lighting from 400 Lux to 20 kLux (approximating direct sunlight) of intensity. Under 20 kLux of incandescent illumination, the p+/n-well photodiodes produce 557 μW/mm^2 while the DNW photodiodes generate 20.75 μW/mm^2; the DNW photodiodes performs worse than the p+/n-well photodiodes as expected.

A stack of three integrated DNW photodiodes without explicit bypass capacitance produces output voltages as shown in Fig. 7, when illuminated with white LED light flickering completely on and off at 120 Hz with 20% and 50% duty cycles, corresponding to measured ripple of 1.19V and 1.15V, respectively. Higher duty cycles reduce ripple since the output voltage has less time to discharge. The output of the photodiode when the LED is turned off is non-zero due to the background room lighting.

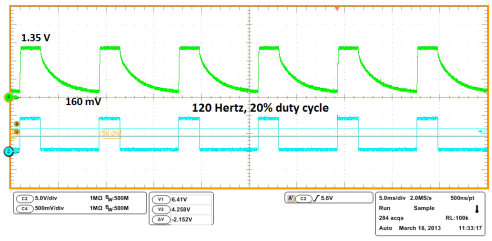
To understand how ripple effects the operation of switched-capacitor boost converter, transistor-level simulations of Fig. 2 across a range of switching frequencies at 50% illumination duty cycle were performed. Two schemes were simulated: 1) complete and 2) partial light flickering, both at 120 Hz and with no photodiode bypass capacitance C_b (maximum photodiode output voltage ripple). The assumed maximum illumination for both schemes is the same. The minimum illumination for the partial scheme is higher since the LED is assumed to be partially off. The ratio of ripple to desired output voltage (1.6V) versus switching frequencies is plotted in Fig. 8. The plot on the left in Fig. 8 was obtained by assuming constant illumination (no flickering). The ripple at low frequencies comes from the periodic charge/discharge of the flying capacitors. As frequency increases, the flying capacitors do not have enough time to completely discharge, resulting in small ($< 1\%$) ripple.

When there is ripple on the input voltage due to light flickering, this ripple is translated to the output and dominates any ripple due to flying capacitor charging/discharging for switching frequency $f_{sw} > 1$ kHz as seen in the plot on the right in Fig. 8. When the switching frequency is much greater than the flicker frequency for no C_b, the converter output is fully charged and discharged within each flicker cycle due to the large number of switching cycles in each flicker period T_f; consequently the ripple expressed as a percentage of the desired output voltage is 100%. As the flickering amplitude decreases, the curve shifts down at high frequency since the ratio of ripple to desired output voltage decreases. However, below 1 kHz switching frequency, the phase of the switching can affect the output voltage greatly. In Fig. 8 the light flicker and the switching frequency are in phase.

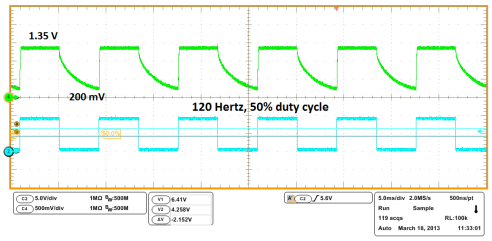
A balance exists between charging the flying capacitors to the boost converter input voltage (the photodiode output voltage) during one clock phase and having the input voltage appear at the bottom plate of the first flying capacitor on the next clock phase. The boost converter output voltage reaches a maximum at $f_{sw} = 60$ Hz because during both phases ϕ_2 and ϕ_1, the light flickers on and off once. Likewise, there is a minimum at 40 Hz when the boost converter clock and the light flicker are in phase because when the flying capacitors are in parallel, the photodiodes are illuminated twice, and on the next clock phase when capacitors are stacked in series, the photodiodes are only illuminated once and experience no light for twice as long. In general, it is desirable to operate the boost converter at frequencies higher than the flicker frequency when C_b is sufficiently large. Operating the boost converter at low frequencies causes extra photogenerated carriers in the photodiode in each flicker cycle to be wasted.

B. Switched-Capacitor Boost Converter

The 1:4 boost converter (labeled in the die photo in Fig. 6) was tested using a DC power supply. The calculated, simulated, and measured converter output voltage V_{out} versus switching frequency f_{sw} is plotted in Fig. 9, for V_{in} =0.3V, N =4, C_{ST} =126pF, R_i =187Ω, C_L =384pF, R_L =10$M\Omega$ and C_p =28pF. The simulated circuit includes transistor implementations for the switches and the bottom plate parasitic capacitnaces. Note that the bottom plate parasitics are predicted by the model to reduce the boost ratio from the ideal of 4 to approximately 3. The model matches measurement results to within 10% for switching frequencies from 500 Hz to 5 MHz. The deviations of the model in this frequency range are likely due to the assumed uniform distribution of the output impedance to each stage (Figure 4). At frequencies beyond 5 MHz, an ideal transformer model cannot be used and additional parasitics must be included. Although not modeled here, V_{out} is expected to converge to V_{in} at frequencies well beyond 5 MHz (as indicated in the simulated result) since



(a) 20% duty cycle.



(b) 50% duty cycle.

Fig. 7. Output of three stacked DNW photodiodes under PWM white LED illumination at 120 Hertz and (a) 20% and (b) 50% duty cycle.

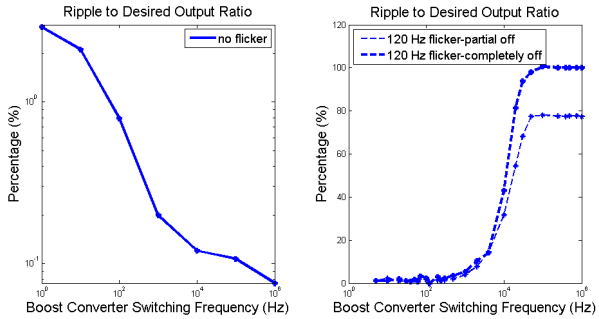


Fig. 8. Output ripple versus boost converter switching frequency f_{sw}. Left: no flicker. Right: 120 Hz flicker at two different flicker amplitudes.

the voltage across the flying capacitor approaches zero at $f_{sw} > 100$ MHz.

In the test chip, the flying capacitors were built using double polysilicon capacitors. The dominant parasitic capacitance is formed by the bottom polysilicon layer and the substrate. Fabricating the flying capacitors using higher metal layers should reduce the parasitic capacitances. In the model, parasitic capacitances at the source and drain of the transistors implementing the switches were ignored since the transistors are small compared to the flying capacitors.

C. Delta-Sigma Modulator

Fig. 10 shows a close-up view of the DSM with various blocks labeled. Fig. 11 shows the measured DSM output spectrum with an input sinusoid applied at 981 Hz and a clean power supply. With the Nyquist rate $f_N = 4$ kHz and a sampling rate of 1.6 MHz, the SNDR is approximately 50 dB, achieving an ENOB of approximately 8 bits at $V_{DD} = 1.8$V. Fig. 12 shows the measured DSM power consumption with respect to supply voltage and sampling frequency. At 50 kHz sampling rate and 1.6V supply voltage, the modulator achieves sub-microwatt operation. The extrapolated leakage

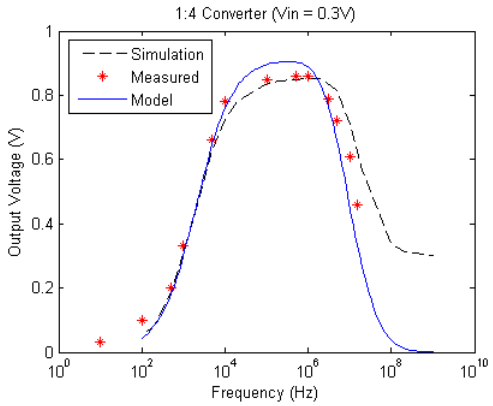


Fig. 9. V_{out} versus switching frequency for 1:4 boost converter.

power at 1.8V supply is approximately 1.6 μW.

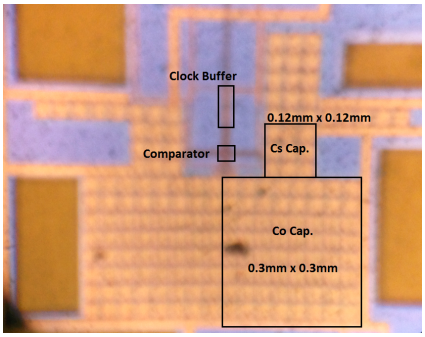


Fig. 10. Die photo of the passive delta-sigma modulator.

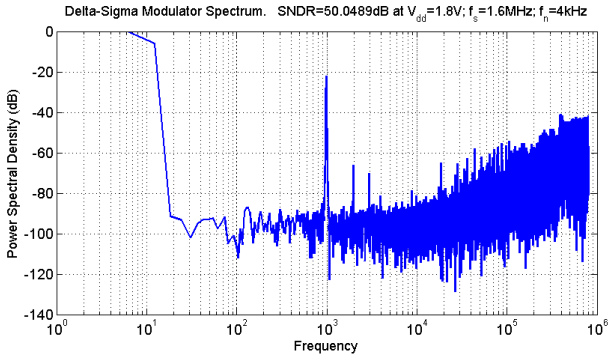


Fig. 11. Measured DSM output spectrum with no power supply ripple.

D. Supply Ripple Effects

As discussed previously, distortion at the DSM output due to supply ripple is primarily caused by amplitude modulation (AM) of the switched-capacitor filter clock mixing with the input. Figure 13 show the measured DSM output spectrum when experiencing a worst-case square wave supply ripple of 0.8V peak-to-peak (largest amplitude that does not overload the DSM) at 120 Hz on a DC supply V_{DC} of 1.4V, at bands below and above the input tone at 980 Hz, respectively. Distortion tones are labeled in Figure 13, which shows the lower sideband of the DSM output spectrum.The ripple frequency

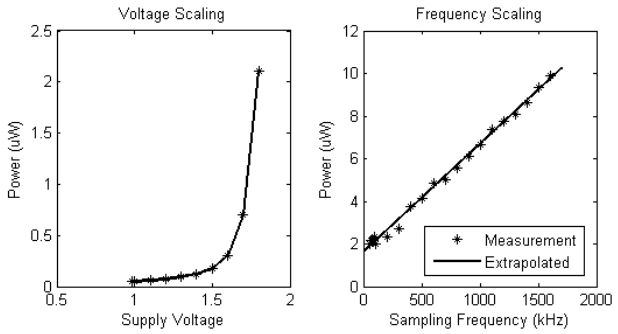


Fig. 12. Measured DSM power versus supply voltage at 50 kHz sampling rate (left) and versus sampling frequency at $V_{DD} = 1.8$V (right).

and its odd harmonics can be clearly seen and are labeled accordingly. Second order intermodulation (IM2) between the input signal and the frequency tones in the ripple itself are labeled as "IM2,$\pm N$", where N is the order of the harmonic of the ripple frequency. The sum-product terms labeled in Fig. 13 are a result from IM2 between the frequency tones within the ripple itself. Note that the distortion can be reduced significantly if the high frequency components in the ripple are attenuated. With increasing supply ripple amplitude, the DSM output SNDR is reduced by almost 16 dB compared to the output without supply ripple. Fig. 14 shows the measured SNDR degradation with ripple amplitude. If 20dB of SNDR is tolerable, the supply ripple can be 21% of V_{PD}, which implies a required bypass capacitance of only $C_b = 3.86$ nF.

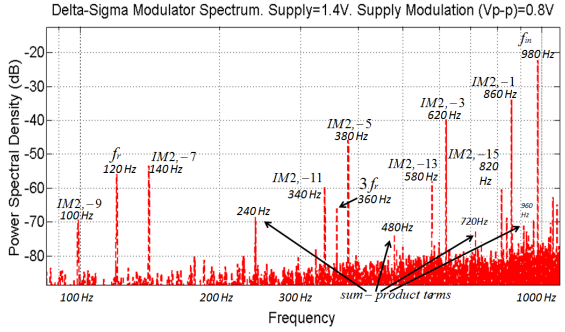


Fig. 13. Measured DSM output spectrum with lower sideband distortion tones labeled.

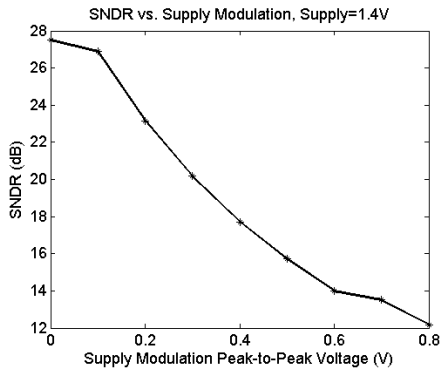


Fig. 14. Measured DSM output SNDR versus supply ripple.

V. Conclusion

This paper studied the effects of light flicker on optically powered systems, in particular, effects of flicker on integrated photodiodes, switched-capacitor boost converter, and a passive filter-based DSM. A boost converter circuit model was presented that includes losses due to the flying capacitors and switches, and also to the parasitic capacitance at the bottom plate of the flying capacitors. The proposed boost converter model was validated using simulations and measurements on a 180nm CMOS test chip, confirming that the model predicts the measured output voltage to within 10% over practical switching frequencies. The effect of light flicker-induced supply ripple on the DSM output through amplitude modulation of clocks is also investigated using the test chip. The models and analysis presented in this work can be used to select the minimum bypass capacitance that satisfies load requirements, leading to cheaper and smaller wireless sensors.

VI. Acknowledgements

The authors thank W. McIntyre, A. Rao, K. Schoendoerfer, and G. Winter of Texas Instruments for technical insights and support. E. Fong and S. Hsu are supported by a gift from Texas Instruments. Chip fabrication support was provided by B. Chatterjee and Texas Instruments.

References

[1] Y. Tan and S. Panda, "Energy harvesting from hybrid indoor ambient light and thermal energy sources for enhanced performance of wireless sensor nodes," *Industrial Electronics, IEEE Transactions on*, vol. 58, no. 9, pp. 4424–4435, 2011.

[2] N. Guilar *et al.*, "Integrated solar energy harvesting and storage," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 17, no. 5, pp. 627 –637, may 2009.

[3] S. Ayazian *et al.*, "A photovoltaic-driven and energy-autonomous cmos implantable sensor," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 6, no. 4, pp. 336–343, 2012.

[4] B. Sarioglu *et al.*, "An optically powered cmos receiver system for intravascular magnetic resonance applications," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol. 2, no. 4, pp. 683–691, 2012.

[5] R. Rosen, "Dimming techniques for switched-mode LED drivers," Application Note Lit. No. SNVA605, Texas Instruments, Dallas, Texas, USA, 2011.

[6] E. Fong *et al.*, "Integrated energy-harvesting photodiodes with diffractive storage capacitance," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 21, no. 3, pp. 486 –497, march 2013.

[7] H.-P. Le, S. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc-dc converters," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 9, pp. 2120–2131, Sept.

[8] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *Computers in Power Electronics, 2006. COMPEL '06. IEEE Workshops on*, pp. 216–224, July.

[9] F. Chen, S. Ramaswamy, and B. Bakkaloglu, "A 1.5v 1ma 80db passive sigma; delta; adc in 0.13 mu;m digital cmos process," in *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, 2003, pp. 54–477 vol.1.

[10] T. Kleeburg *et al.*, "Ultra-low-voltage circuits for sensor applications powered by free-space optics," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, feb. 2010, pp. 502 –503.

[11] B. Cook *et al.*, "Low-power 2.4-ghz transceiver with passive rx front-end and 400-mv supply," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 12, pp. 2757–2766, 2006.