Analysis of DC-DC Conversion for Energy Harvesting Systems Using a Mixed-Signal Sliding-Mode Controller

Nathaniel J. Guilar[1, 2], Rajeevan Amirtharajah[1], and Paul Hurst[2]

[1]Micropower Circuits and Systems Group
Department of Electrical and Computer Engineering
University of California, Davis, CA 95616

[2]Solid-State Research Laboratory
Department of Electrical and Computer Engineering
University of California, Davis, CA 95616

***Abstract*-Increasing efficiencies in electronic devices have opened the door for energy harvesters to power wireless systems by scavenging energy from solar, thermal, or mechanical sources. The design of an efficient power supply that can regulate scavenged energy to produce stable voltages for multiple loads is presented here. To limit energy dissipation and increase the flexibility of the regulator, a discrete-time sliding-mode controller is presented. The performance of sliding-mode controllers is hard to predict because their switching frequency and output voltage ripple are dependent on duty cycle and load conditions. An analytical approach for the closed-loop steady-state behavior of a discrete-time sliding-mode controller is presented here. The proposed analytical solution matches measured results to within 4% for duty cycles ranging between 0.1 and 0.9.**

I. INTRODUCTION

Today's circuit designers can choose from an array of analog, digital, and mixed-signal voltage regulators. Each class of regulator has its own benefits and drawbacks. Figure 1 illustrates the design tradeoffs for different regulators. There is an inherent tradeoff between performance (voltage ripple, rise time, offset, and overshoot) and efficiency. For instance, pulse width modulation (PWM) regulators, which are commonly used for digital circuits, can achieve very high efficiencies, but at the cost of significant output ripple. Low dropout (LDO) linear regulators, which are commonly used for sensitive RF and analog circuits, can achieve high tracking speeds without switching noise but with relatively poor efficiencies due to the static currents used to bias the analog circuits and the voltage drop across the power transistor.

In many systems, analog and digital circuits must work together, as in the energy harvesting wireless sensor node [1,2] shown in Fig. 2. Using separate regulators for the analog and digital subsystems can substantially increase area and cost. It is desirable to have a single regulator for the entire system which is highly flexible so that it can meet the requirements for analog and digital load circuits. A mixed-signal sliding-mode (SM) regulator is highly flexible [3] and has the ability to trade off efficiency for performance.

This work analyzes the power supply needs for an energy harvesting wireless sensor node, and explores the tradeoffs between various power regulators for this application. A regulator that satisfies the flexibility, efficiency and performance requirements for energy harvesting is analyzed.

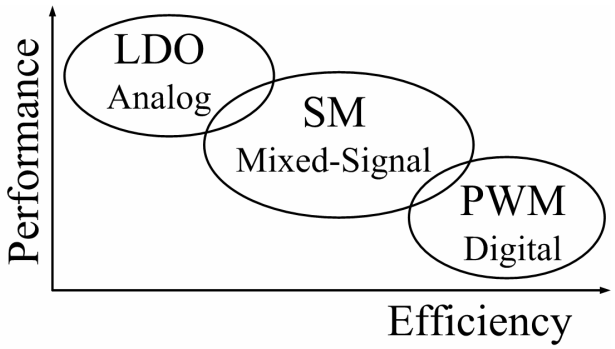

Figure 1.Design tradeoffs for different regulator topologies

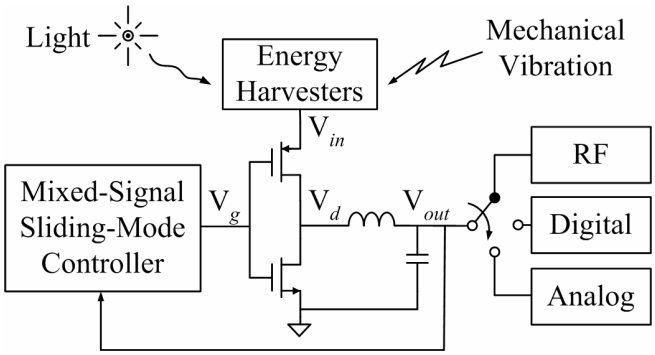

Figure 2. Block diagram of an energy harvesting regulator with light and mechanical vibration energy sources. A discrete-time mixed-signal SM controller operates a buck converter, which supplies power for RF, digital, and analog circuitry. V_g is the control signal, which is used to modulate the state of the output transistors, switching V_d between the energy harvesting voltage V_{in} and ground.

II. APPROACH

A. Mixed-Signal Sliding-Mode

Figure 3 shows a block diagram of a discrete-time mixed-signal SM controller operating a buck converter, with a low-pass output filter G(jω). The simple model for G(jω) consists of a series inductor, shunt capacitor and load, as shown in Fig. 2. At first, ignore the filter H(z) in Fig. 3. The controller first samples the error signal, determines its polarity, and then drives the output as hard as it can in the opposite direction of the error. In steady-state, the SM controller signal (V_d) ideally converges to a limit-cycle with a constant oscillation frequency and pulse width. An approximate expression for the switching at the output of the power transistors is

$$V_d(t) = \begin{cases} V_{in} & TD \le t < T \\ 0 & 0 \le t < TD \end{cases} \quad (1)$$

where D is the duty cycle and T is the limit-cycle oscillation period. G(jω) will attenuate the higher harmonics of the periodic signal in (1), leaving only the desired DC value and a residual ripple from the fundamental at the output of the regulator.

To improve the closed loop performance (higher switching frequency and smaller output ripple), the error signal V_e in Fig. 3 can be passed through a signal filter H(z) before reaching the comparator input V_x. To allow for the use of low-power passive switched-capacitor filter circuits, it is desirable to implement a discrete-time FIR signal filter H(z).

$$H(z) = \frac{V_x}{V_{ref} - V_{out}} = \left(1 - kz^{-1}\right)z^{-2} \quad (2)$$

where z^{-1} equals the delay of the sampling interval, $T_s = 1/f_s$. The last term in (2) is z^{-2}, which models a two-sample-period parasitic delay in the signal path from V_e to the comparator input but does not affect the zero of the filter. If the two coefficients in the filter are equal (k=1), the signal filter approximates a differentiator by computing an output that is the first difference between two consecutive input samples. When 0<k<1, the signal filter approximates a continuous time proportional plus derivative (PD) filter with the proportional term = 1-k and the derivative term = k.

Figure 4 shows a graphical representation of an example course for the locus of a discrete-time SM controller in the phase plane [4]. If H(z) is tuned accurately, it can provide a zero in the closed loop transfer function, which can be adjusted to cancel a pole from G(jω). Complete cancellation can depend on loading characteristics, which may be unknown in practice. It has been shown that a buck converter under SM control can be described by the error amplitude and its rate of change instead of the capacitor voltage and inductor current in G(jω) [5]. The resulting single-time-constant response of the system can then be modeled with a first-order differential equation in terms of the error signal. The sliding surface is defined as

$$\sigma = \dot{V}_e + \lambda V_e \quad (3)$$

where λ is the resulting eigenvalue of the simplified first-order response.

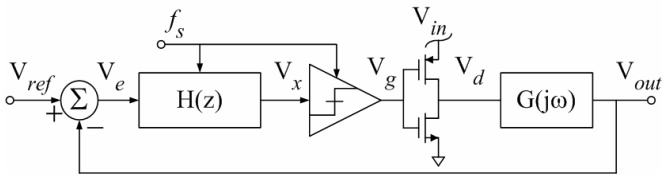

Figure 3. Block diagram of discrete-time mixed-signal SM controller with output stage. V_{in} is the unregulated power source, and V_e is the difference between the desired output voltage (V_{ref}) and the actual output voltage (V_{out}). G(jω) is a passive low pass output filter, which is used to smooth the output of the buck converter. Both the discrete time filter H(z) and comparator operate at a sampling rate of f_s.

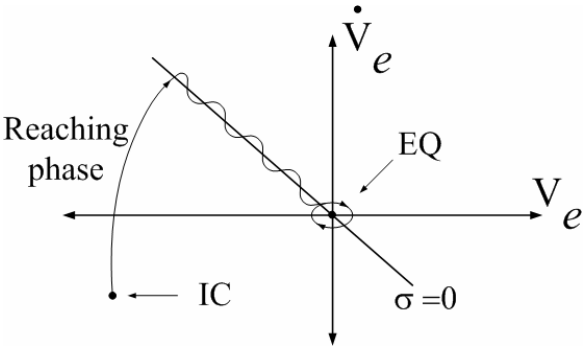

Figure 4. Graphical representation of the sliding condition in a phase plane. The origin of the phase plane represents a system that has V_{out}=V_{ref} for both error position and trajectory. The locus starts at initial condition and eventually stabilizes into a limit-cycle around an equilibrium point.

An initial condition (IC) starts the system with a finite position and velocity error. The trajectory in time of the error will progress exponentially towards the sliding surface σ = 0. This movement of the locus from the initial condition to the sliding surface is known as the reaching phase. Ideally, once the locus of the system has reached the sliding surface it would slide smoothly along the surface until reaching the equilibrium point (EQ), where V_{out}=V_{ref}.

Due to imperfect control switching, loop delay and other nonidealities, the trajectory of the tracking error vector will oscillate around the sliding surface creating a limit-cycle. A limit-cycle is defined as a closed-loop orbital trajectory in a phase space. The type of limit-cycles discussed here are stable which implies a self-sustained isolated oscillation. In many feedback controllers, a large loop gain at low frequencies is required to minimize the steady state error. For the proposed discrete-time SM controller, the gain is provided by the comparator.

In order to explore the design tradeoffs associated with different controller techniques, a comparison was conducted between different voltage regulators. Figure 5 shows the block diagram of the test bench for the three additional voltage regulators, which were simulated and compared to the proposed discrete-time SM regulator. Here, we compare the SM controller against a LDO and two varieties of PWM control.

B. Design Space Comparison

Numerous analog and digital circuit implementations of PWM controllers have been published [6-9]. Analog PWM controllers are able to provide a very fine tuning granularity for the average output value, but require wasteful static power. Digital PWM controllers can only tune the output to discrete values, and increasing the tuning precision will generally require additional circuitry and power consumption. Similar to the poly-phase sigma-delta modulator described in [10], the discrete time SM controller can only make switching transitions at intervals of T_s. In practice, this may limit the overall tunable step size of the regulator. If the discrete time SM controller in Fig. 3 is asked to produce a duty cycle D that corresponds to a pulse width which is not an integer multiple of T_s, the controller will alternate between two or more separate pulse widths and limit-cycles, eventually averaging near the desired D.

Table I compares the simulated performance of SM, analog PWM, digital 1-bit PWM, and LDO voltage regulators, which are shown in Fig. 3 and 5. All regulators were simulated with the same V_{in}, load resistance and output capacitance. The target output power for the comparison was 1 mW at 1 V. The size of the CMOS output drivers were selected to give a conduction efficiency of 90% at the target power and voltage. To meet the target conduction efficiency in a 0.35 µm technology with a 2 V supply, the resulting symmetrical power transistors require widths of 135 µm and 45 µm for the PMOS and NMOS devices, respectively. The switching losses of the power transistors will also impact the total efficiency of the regulator. A procedure to maximize the efficiency of a buck converter can be found in [11].

From H(z), the 50 ns delay in the SM controller corresponds to a two-sample-period delay, which places the sampling rate for H(z) at 40 MHz. The PWM controllers operate at 1 MHz (f_{switch} in Fig. 5), while SM controller has a limit-cycle frequency of f_{switch}. The SM and digital PWM controllers offer the most power efficient regulation techniques since they require no static currents. For k=0, the mixed-signal SM controller in Fig. 3 consists only of analog circuitry to generate the error signal and a comparator. A 1-bit digital PWM controller [8] will require the same analog error signal and comparator as the SM controller plus additional circuitry to generate the PWM waveform. The SM controller needs a higher clock rate than the 1-bit digital PWM, but requires less circuitry. The question then becomes which controller consumes less energy, and the answer depends on the resolution of the digital PWM regulator. From [8], each output voltage level (corresponding to a discrete duty cycle) requires 136 nW of power at 1 MHz in a 0.35 µm CMOS technology. Transistor-level simulations from layouts including extracted parasitics suggest that the entire SM controller will consume 26 µW of power with a sampling rate of 40 MHz in the same technology. We can then estimate a consumption of 650 nW to generate the 1-bit error-signal for the PWM generator at 1 MHz. Therefore, if more than 186 distinct output levels (7.5-bit resolution) are required, the SM controller will result in a more efficient control technique.

Mechanical vibration energy harvesters can potentially generate open-circuit voltages greater than 30V [12]. Assuming the analog subsystem requires a supply voltage of 0.9-1.1V (1V±10%), the regulator for the mechanical energy harvester described in [12] will require more than 300 distinct output levels (8.2-bit resolution). For this dynamic range and resolution, an SM controller is the most efficient technique for regulating the harvested mechanical energy.

The digital SM controller in [13] targets adaptive power supply regulation for digital systems based on critical path delays. It consumes as little as 400 µW with 40 distinct output levels in 0.25 µm CMOS. The discrete-time mixed-signal SM controller described above can provide much higher output resolution (ultimately limited by comparator offset and the sampling rate) while consuming less power, and is suitable for analog and digital loads. Many of the performance requirements for the voltage regulator in the energy harvesting wireless sensor node will be determined by the subsystem with the highest supply voltage sensitivity, which is often an analog-to-digital converter (ADC). A possible ADC for this application is an energy efficient 8-bit successive approximation ADC operating at 200 kS/s [14]. If this ADC has a full scale voltage of 1V and a power supply rejection ratio (PSRR) of 0 dB to 30 dB, it will require less than 2 to 60 mV of supply noise, respectively.

Figure 6 shows MATLAB simulations for a 1V 35µs pulse at V_{ref} for the SM controller in Fig. 3 and the analog PWM (APWM) controller in Fig. 5. The SM controller was modeled with a parasitic loop delay, which was chosen to set the limit-cycle frequency close to 1 MHz, with k=0. The analog PWM controller has a gain that was chosen to set the overshoot to 1% (close to the overshoot for the SM). For these simulations, V_{in} and G(jω) were the same for all switching regulators. It is important for a regulator which handles multiple loads to have a fast transient response. Otherwise, considerable time and energy are spent switching between subsystems with different voltage and ripple requirements. The ADC in [13] requires 40 µs to process a single input sample at 200 kHz. The rise and fall times of the voltage regulator will increase the total power-on time of the ADC subsystem operating on a single sample to 108 µs for the 1-bit digital PWM controller. The SM controller with an identical voltage ripple can accomplish the same task in 46 µs, an improvement of 2.3x. Furthermore, for the SM controller, very little dynamic power is dissipated during large voltage steps since the output transistors will not be continuously switching on and off.

TABLE I
REGULATOR COMPARISON RESULTS (Vin = 2 V, $Pout$ = 1 mW, 0.35 µm)

Parameter	SM	LDO	1b PWM	APWM
f switch	980 kHz	N/A	1 MHz	1 MHz
f (-3dB)	167 kHz	209 kHz	167 kHz	167 kHz
Ripple	51 mV	N/A	50 mV	50 mV
Overshoot	8 mV	10 mV	30 mV	10 mV
Delay (T_d)	50 ns	N/A	0.5 µs	N/A
Offset	17 mV	1 mV	5 mV	5 mV
Rise Time	3 µs	2.6 µs	34 µs	14 µs
Gain (A)	N/A	1 V/µs *	15.6 k **	85.5 k
Efficiency	86%	70%	89%	73%

** Gain = Switching Frequency / Number of Steps (64 step PWM)
* Slew rate at gate of PMOS power transistor

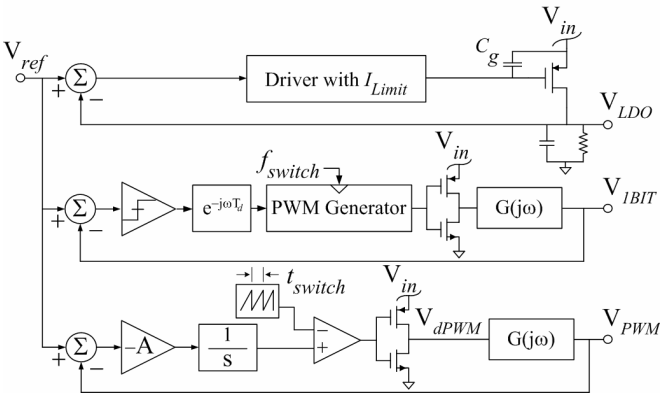

Figure 5. Block diagram of test bench for comparing various regulators. V_{LDO}, V_{1BIT} and V_{PWM} are the regulated output voltages for the linear regulator, digital 1-bit PWM and analog PWM regulators, respectively.

III. ANALYSIS OF SM CONTROLLER

A. Free Running Frequency

In many wireless applications, a highly efficient regulator will need to supply power for a communication system [15]. Due to poor power supply rejection, which is common in low power transceivers, the transmitted signal is susceptible to the switching noise from the power supply. Furthermore, a mixer could modulate the switching noise to an undesired region of the transmitted spectrum where it could further corrupt the integrity of the signal. When the switching frequency is known (as is the case with PWM), it is possible to devise a system-level approach that will place the switching noise of the regulator in a benign spectral location, enabling looser ripple requirements. In practice, the limit-cycle frequency of an SM voltage regulator is not well controlled, and this unknown switching frequency can complicate integrating the controller with other circuitry. It is therefore desirable to have an understanding of the limit-cycle frequency and its dependencies on controller and load parameters. This section analyzes the steady state operation of an SM controller, and outlines an estimation technique for the limit-cycle frequency as a function of multiple circuit parameters.

Previous works have pioneered the understanding of SM controllers [16-20]. To analyze the closed-loop behavior of the SM controller, we will start with the assumption that the limit-cycle oscillation frequency ω is the product of a free running frequency ω_o and a nonlinear function of the duty cycle *f*(D),

$$\omega = f(D)\omega_o \tag{4}$$

Since the phase shift around the loop depends on the period of oscillation, determining the free running frequency requires solving a transcendental equation. The free running limit-cycle period T_o is equal to twice the loop delay when D=1/2 [16]. Summing the phase shifts from H(z) and G(jω) yields an equation that can be used to find the free running period for the discrete-time mixed-signal SM controller:

$$T_o = 4T_s + \frac{T_o}{\pi}\left[\begin{array}{l}\tan^{-1}\left(\frac{2\pi}{p_1 T_o}\right)+\tan^{-1}\left(\frac{2\pi}{p_2 T_o}\right)\\ -\tan^{-1}\left(\frac{k\sin\left(\frac{2\pi T_s}{T_o}\right)}{1-k\cos\left(\frac{2\pi T_s}{T_o}\right)}\right)\end{array}\right] \tag{5}$$

here we assume the output filter G(jω) can be modeled as a second-order filter with real pole magnitudes p_1 and p_2. Note that (5) is only accurate when a single frequency is present in the comparator input voltage V_x, which is a good assumption when D=1/2. In order to incorporate hysteresis into this analysis, an additional positive phase shift of $sin^{-1}(\delta/M)$ could be added within the brackets of (5), where δ is the width of the hysteresis and M is the amplitude of the limit-cycle frequency at the input of the comparator [21].

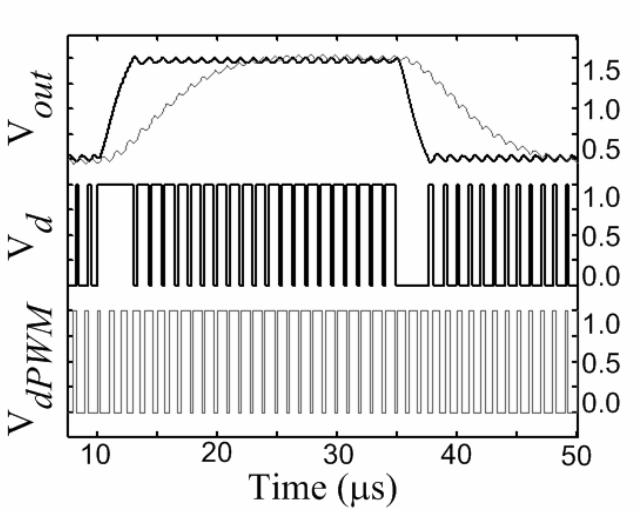

Figure 6. Simulated results comparing SM and analog PWM regulators. SM and PWM are the darker and lighter V_{out} traces, respectively. The two lower traces V_d and V_{dPWM} are the control signals for the SM and analog PWM regulators from Fig. 3 and 5, respectively.

B. Two-Sinusoid-Input Describing Function

Describing Function (DF) analysis can be used to analyze a system which has a strongly nonlinear element, such as a comparator [4]. The DF is based on a quasi-linearization technique that replaces the nonlinear element under consideration with an element that is linear except for a dependence on the amplitude of the input waveform. For the proposed SM controller, traditional DF analysis will only account for the effects from the fundamental component of the square wave in (1).

Bulga [22] pioneered the Two-Sinusoid-Input Describing Function (TSIDF), which is generated from extending the DF to include a second term from the Fourier series created by the nonlinearity. From [21], the TSIDF for an ideal comparator that considers input frequencies from a fundamental and its n^{th} harmonic is an elliptic integral of the first kind. The TSIDF for a comparator whose output switches between 0 and V_{in} and whose input has an amplitude of M is

$$N_m = \frac{4Vin}{\pi^2 M}\int_0^{\pi/2}\sqrt{1-m^2\sin^2(\psi)}\,d\psi \tag{6}$$

where m is the ratio of amplitudes between the n^{th} harmonic and the fundamental at the input of the comparator, and ψ is a term relating the relative phase between the two tones at V_x. By expanding the TSIDF into a power series, the following expression may be obtained [23]:

$$N_m = \frac{2Vin}{\pi M}\left(1-\frac{1}{4}m^2-\frac{3}{64}m^4-\frac{5}{256}m^6\cdots\right) \tag{7}$$

Since the comparator is assumed to be memoryless the equivalent transfer function in (7) has no phase shift, hence the TSIDF is purely real. It can also be seen that the TSIDF is independent of frequency, depending instead on amplitude. Assuming that the error signal is small, (7) may be approximated for the case when n = 2 and k = 0 by truncating to the first two terms [24]. Eq. (7) can be written in terms of duty cycle D by assuming a linear mapping between the

range of D (0 < D < 1) and the range of m (-1 < m < 1) [10], yielding:

$$D=\frac{1}{2}(m+1) \tag{8}$$

The resulting pseudo-linear equivalent gain for the comparator with a duty-cycle dependency is

$$N_D=\frac{2Vin}{\pi M}\left(\frac{3}{4}+D-D^2\right) \tag{9}$$

The resulting ripple amplitude can be computed with the knowledge of the magnitude response of G(jω) and the limit-cycle frequency.

Johnson [25] outlines an approach to determine *f*(D) from the TSIDF, which results in the following power series [22]:

$$\omega=\left(1-\frac{\lambda_2}{2!}m^2-\frac{\lambda_3}{3!}m^3-\frac{\lambda_4}{4!}m^4\cdots\right)\omega_o \tag{10}$$

where λ_n are frequency correction terms. By factoring the second-order term from the parenthesis in (10) we arrive at:

$$\omega=\left(1-m^2\left[\sum_{n=2}^{\infty}\frac{\lambda_n}{n!}m^{(n-2)}\right]\right)\omega_o \tag{11}$$

Assuming m=0.5 (average value for $\sin^2\omega t$) within the summation, the power series converges to a constant value that can be found using a best fit to simulation results. This value corresponds to the frequency correction terms (λ_n's) being approximately 1. By applying (8), the resulting estimation for the limit-cycle frequency as a function of duty cycle is obtained:

$$\omega=\left(1-0.59(2D-1)^2\right)\frac{2\pi}{T_o} \tag{12}$$

where T_o may be determined from (5).

Fig. 7 shows an example plot of the limit-cycle frequency normalized to 5 MHz vs. load resistance and duty cycle. The oscillation frequency increases with a shrinking load resistance due to the phase shift in G(jω). In order to explore the validity of the model derived for *f*(D), an SM controller was built from discrete components. Figure 8 shows a schematic of the prototype built from discrete components using a breadboard. The signal filter H(z) was omitted for these experiments since the goal was to observe only the effects due to the changes in D. Figure 9 shows the measured waveforms from the discrete prototype.

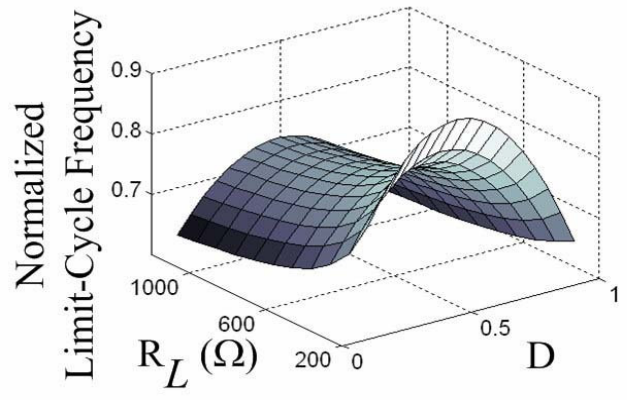

Figure 7. Analytical model of the normalized limit-cycle frequency plotted vs. load resistance and duty cycle.

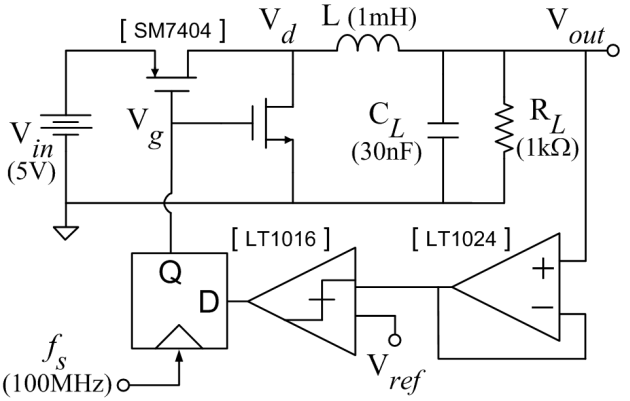

Figure 8. Schematic of test setup with discrete components, biasing circuitry omitted.

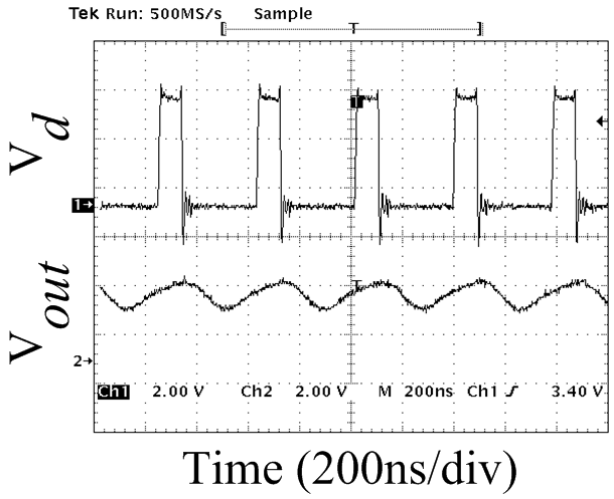

Figure 9. Measured steady-state output and gate voltages.

V. RESULTS AND CONCLUSION

Figure 10 shows a comparison between measured, analytical, and simulated limit-cycle oscillation frequencies vs. duty cycle for the circuit in Fig. 8. The model-to-error ratio, defined as the power in the analytical results divided by the power in the difference between the measured and analytical results, is 28dB and 43dB for conversion-ratio ranges of 80% and 20% percent, respectively. The slight asymmetry of the plots in Fig. 10 is largely caused by unequal charge and discharge time constants for the buck converter. If the on-resistances of the power transistors are made to be equal and much smaller than the load resistance, this asymmetry can be minimized.

For the configuration in Fig. 8, measurements show a 2x peak variation in switching frequency due to changes in D. Simulations suggest that by adaptively changing k in (2) to compensate for the limit-cycle dependence on D, a decrease in limit-cycle sensitivity can be obtained. Altering k will also allow controller flexibility and enable a tradeoff between efficiency (small k, low ω, high ripple) and performance (large k, high ω, low ripple).

Figure 11 shows a plot of the simulated limit-cycle frequency vs. duty-cycle for various signal filters. The solid line is the SM controller with k=0, the dashed line has k

equal to a continuous function of D, and the dotted line has k equal to a discrete function of D. The discrete function of k is equivalent to digitally trimming the ratio of capacitor values in a switched-capacitor circuit. Here, a 2b digital trim varies the amount of k symmetrically around D=1/2 with equally spaced thresholds.

For a 5% variance in the limit-cycle frequency from the free running frequency, an SM controller with k=0 can only achieve a conversion-ratio range of 30%, while the continuously variable k controller achieves a conversion-ratio range of 60%. When allowing for a 10% variance in switching frequency the conversion-ratio range for the continuously tunable and discrete signal filter with 2b trim is near 70% and 60%, respectively. Increasing the resolution of the digital trim to 3b expands its conversion range to 65%.

By dynamically changing the value of k as a function of D, the variance in the switching frequency of the discrete-time SM controller has been shown to be reduced by as much as a factor of 2x. A continuously variable k will yield the best results, but a programmable k using a 2b or 3b digital trim may also be sufficient for certain applications.

ACKNOWLEDGMENTS

The authors are grateful for technical discussions with S. Lewis and Z. Sabato. N. Guilar is supported by a U.S. Dept. of Education GAANN fellowship.

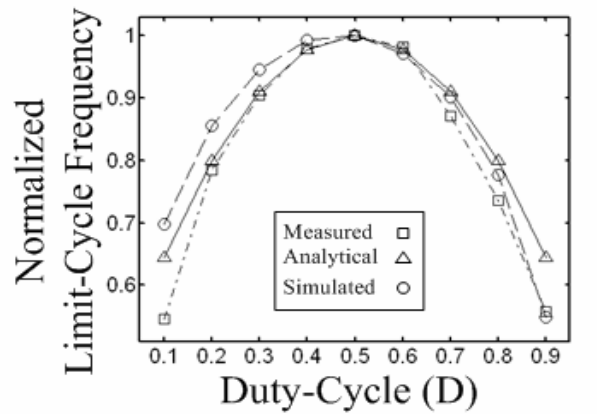

Figure 10. Limit-cycle frequency (normalized to 5 MHz) vs. duty cycle for measured, analytical and simulated data points with k=0.

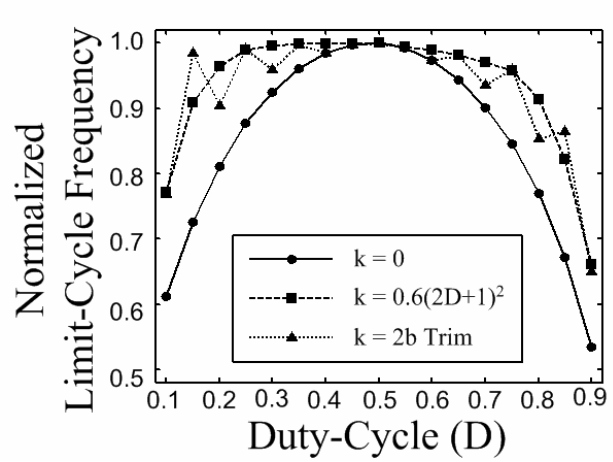

Figure 11. Simulated limit-cycle frequency vs. duty cycle for various signal filters adapting k. Continuous and discrete values of k are compared.

REFERENCES

[1] A. Kansal and M. Srivastava, "An environmental energy harvesting framework for sensor networks," *ISLPED*, pp. 481-6, Aug. 2003.

[2] R. Amirtharajah, J. Wenck, J. Collier, J. Siebert, B. Zhou, "Circuits for Energy Harvesting Sensor Signal Processing," *AMC/IEEE Design Automation Conference*, pp. 639 - 644 , July 2006.

[3] S.-C. Tan, Y. Lai, C. Tse, "An Evaluation of the Practicality of Sliding Mode Controllers in DC-DC Converters and Their General Design Issues," IEEE PESC Conference, pp. 1-7, 2006.

[4] C. L. Phillips and R. D. Harbor Feedback Control Systems, Prentice-Hall, New Jersey, 1996.

[5] R. Vankataramanan, A. Sabanovi´c, and S. Cu´k, "Sliding Mode Control of DC-DC Converters," *IEEE IECON*, vol. 1, pp. 251-258, 1985.

[6] M. Y.-K. Chui, W.-H. Ki, and C.-Y. Tsui, "A Programmable Integrated Digital Controller for Switching Converters With Dual-Band Switching and Complex Pole-Zero Compensation," *IEEE JSSC*, Vol. 40, No. 3, pp. 772-780, March 2005.

[7] V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, " Low-Voltage-Swing Monolithic dc-dc Conversion," *IEEE Trans. on Ckts. and Sys. II*, vol. 51, no. 5, pp. 241-248, May 2004.

[8] A. Dancy, R. Amirtharajah, and A. Chandrakasan, ``High-Efficiency Multiple-Output DC-DC Conversion for Low-Voltage Systems," *IEEE Trans. on VLSI Sys.*, vol. 8, no. 3, pp. 252-63, June 2000.

[9] A. J. Stratakos, S. R. Sanders, and R. W. Brodersen, "A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System," in *IEEE PESC* , pp.619-629, 1994.

[10] E. Roza, "Poly-Phase Sigma-Delta Modulation," *IEEE Circuits and Systems* II, vol. 44, no. 11, pp. 915-923, Nov. 1997.

[11] M. Mulligan, B. Broach, and T. Lee, "A Constant-Frequency Method for Improving Light-Load Efficiency in Synchronous Buck Converters" *IEEE Power Electronics Letters*, vol. 3, no. 1, March 2005.

[12] G. K. Ottman, H. F. Hofmann, G. A. Lesieutre, "Optimized Piezoelectric Energy Harvesting Circuit using Step-Down Converter in Discontinuous Conduction Mode," *IEEE PESC*, pp. 1988-1994, 2002.

[13] J. Kim and M. A. Horowitz, "An Efficient Digital Sliding Controller for Adaptive Power-Supply Regulation," *IEEE JSSC*, vol. 37, no. 5, pp. 639-647, May 2002.

[14] N. Verma, A. Chandrakasan, "A 25mW 100kS/s 12b ADC for Wireless Micro-Sensor Applications," *IEEE ISSCC*, pp. 222-223 & 650, 2006.

[15] B. Otis, Y. Chee, and J. Rabey, "A 400 µW-Rx, 1.6mW-Tx super-regenerative transceiver for wireless sensor networks, *ISSCC 05*, pp. 396-7, 606, Feb. 2005.

[16] Z. J. Palmor, Y. Halevi, and T. Efrati, "A general and exact method for determining limit cycles in decentralized relay systems," *Automatica*, vol. 31, no. 9, pp. 1333-1339, 1995.

[17] A. S. Kislovski, R. Redl and N. O. Sokal, Dynamic Analysis of Switching-Mode DC/DC Converters, Van Nostrand Reinhold, New York, 1991.

[18] G. Wester, "Describing-Function Analysis of a Ripple Regulator with Slew-Rate Limits and Time Delays," *IEEE PESC*, pp. 341-6, 1990.

[19] F. F. Judd and C. T. Chen, "Analysis and Optimal Design of Self-Oscillating DC-to-DC Converters," *IEEE Transactions on Circuit Theory*, vol. CT-18, pp. 651-658, Nov. 1971.

[20] I. M. B´aba´a, T. G. Wilson, and Y.Yu, "Analytic Solutions of Limit Cycles in a Feedback-Regulated Converter System with Hysteresis," *IEEE Trans. Automat. Contr.*, vol. AC-13, pp. 524-531 Oct. 1968.

[21] A. Gelb, and W. E. Vander Velde, Multiple-Input Describing Functions and Nonlinear System Design, McGraw Hill, 1968.

[22] B. V. Bulgakov, Periodic Processes in Free Pseudo-linear Oscillatory Systems*, J. Franklin Inst.*, vol. 235, pp. 591-616, June 1943.

[23] V. Mangulis, Handbook of Series for Scientists and Engineers, Academic Press, New York, 1965.

[24] B. Amsler, R. Gorozdos, "On the analysis of bi-stable control systems" *IRE Automatic Control*, vol. 4, no. 3, pp. 46-58, Dec. 1959.

[25] C. E. Johnson, Sinusoidal Analysis of Feedback-control Systems Containing Nonlinear Elements, *Trans. AIEE, pt.* II, vol. 71, pp.169-181, July, 1952.